Linear Integrated Circuits

Second Edition

D. Roy Choudhury
Shail B. Jain

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Contents

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1

Integrated Circuit Fabrication

1.1 INTRODUCTION

We are going through a period of micro-electronic revolution. For a common person, the role of electronics is limited to audio-visual gadgets like radio and television, but the truth is, today the growth of any industry like communication, control, instrumentation or computer, is dependent upon electronics to a great extent. And integrated circuits are electronics.

The integrated circuit or IC is a miniature, low cost electronic circuit consisting of active and passive components that are irreparably joined together on a single crystal chip of silicon. Most of the components used in ICs are not similar to conventional components in appearance although they perform similar electrical functions. In this chapter, we describe the basic processes used in the fabrication of integrated circuits. Both bipolar and MOS fabrication are treated. These circuits naturally offer a number of distinct advantages over those made by interconnecting discrete components. These may be listed as follows:

1. Miniaturization and hence increased equipment density
2. Cost reduction due to batch processing
3. Increased system reliability due to elimination of soldered joints
4. Improved functional performance (as it is possible to fabricate even complex circuits for better characteristics)
5. Matched devices
6. Increased operating speeds (due to the absence of parasitic capacitance effect)
7. Reduction in power consumption.

1.2 CLASSIFICATION

Integrated circuits offer a wide range of applications and could be broadly classified as:

Digital ICs

Linear ICs

Based upon the above requirements, two distinctly different IC technology namely, Monolithic technology and Hybrid technology have been developed.

In monolithic integrated circuits, all circuit components, both active and passive elements and their interconnections are manufactured into or on top of a single chip of silicon. The monolithic circuit is ideal for applications where identical circuits are required in very large quantities and hence provides lowest per-unit cost and highest order of reliability. In hybrid circuits, separate component parts are attached to a ceramic substrate and interconnected by means of either metallization pattern or wire bonds. This technology is more adaptable to small quantity custom circuits. Based upon the active devices used, ICs can be classified as bipolar (using BJT) and unipolar (using FET). Bipolar and unipolar ICs may further be classified depending upon the isolation technique or type of FET used as in Fig. 1.1.

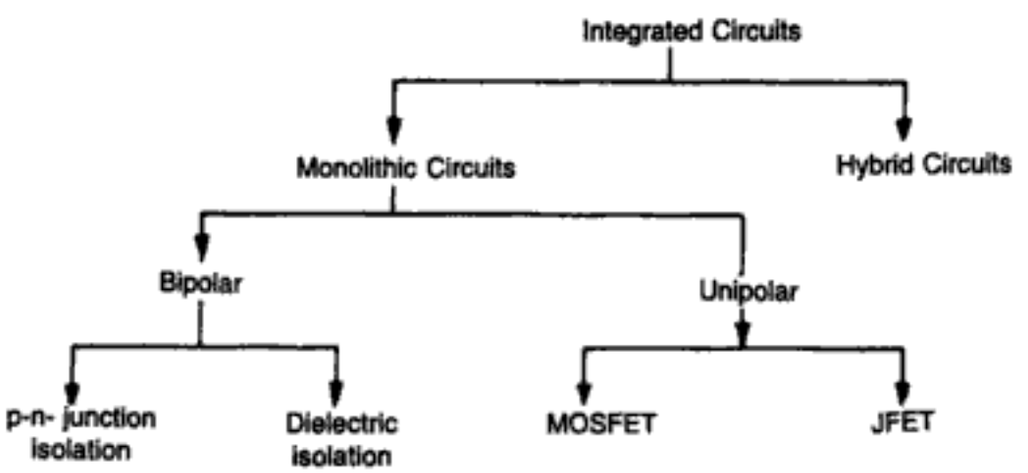


Fig. 1.1 Classification of ICs

1.3 IC CHIP SIZE AND CIRCUIT COMPLEXITY

UP until the 1950s, the electronic device technology was dominated by the vacuum tube. The present day electronics is the result of the invention of the transistor in 1947. The invention of the transistor by William B. Shockley, Walter H. brattain and John Bardeen of Bell Telephone Laboratories was followed by the development of the Integrated circuit (IC). The concept of IC was introduced at the beginning of 1960 by both Texas Instruments and Fairchild Semiconductors. Since that time, the size and complexity of ICs have increased rapidly as shown by the brief chronology.

Invention of transistor (Ge)		1947
Development of Silicon transistor		1955–1959
Silicon Planar Technology	Junction transistor diode	1959
First ICs, Small Scale Integration (SSI)	3 to 30 gates/chip approx. or 100 transistors/chip (Logic gates, Flip-flops)	1960–65
Medium Scale Integration (MSI)	30 to 300 gates/chip or 100 to 1000 transistors/chip (Counters, Multiplexers, Adders)	1965–1970
Large Scale Integration (LSI)	300 to 3000 gates/chip or 1000–20,000 transistors/chip (8 bit microprocessors, ROM, RAM)	1970–1980
Very Large Scale Integration (VLSI)	More than 3000 gates/chip or 20,000–1,00,00,00 transistors/chip (16 and 32 bit microprocessors)	1980–1990
Ultra Large Scale Integration (ULSI)	$10^6 - 10^7$ transistors/chip (Special processors, Virtual reality) machines, Smart sensors	1990–2000
Giant-Scale Integration (GSI)	> 10^7 transistors/chip	

Over the years, the device density has increased together with some increase in the chip area. Figure 1.2 (a, b, c) show small (SSI), medium (MSI) and large (LSI or VLSI) IC chip size. The chip areas range from 1 mm^2 (1600 mil^2)* for the SSI chip to 1 cm^2 (160,000 mil^2) for the LSI chip.

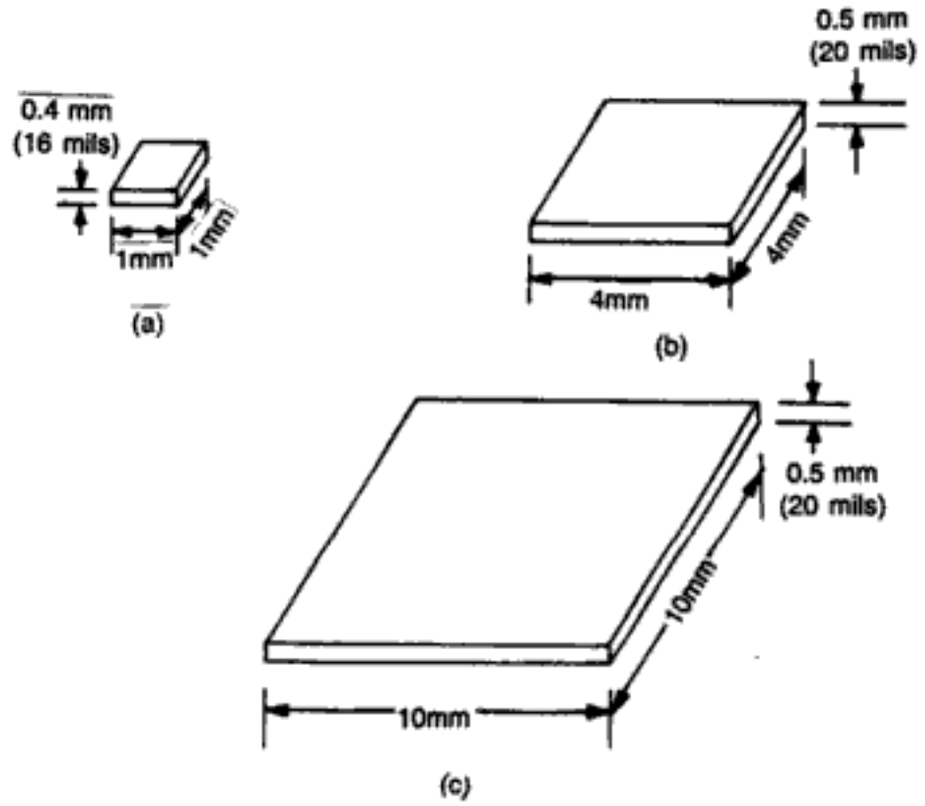


Fig. 1.2 Integrated circuit chips (a) SSI chip (b) MSI chip (c) LSI or VLSI chip

* mil = 0.001 in = 25.4 μm = 0.0254 mm

1.4 FUNDAMENTALS OF MONOLITHIC IC TECHNOLOGY

A monolithic circuit, literally speaking, means a circuit fabricated from a single stone or a single crystal. The origin of the word 'monolithic' is from the Greek word *monos* meaning 'single' and *lithos* meaning 'stone'. So monolithic integrated circuits are, in fact, made in a single piece of single crystal silicon.

The most significant advantage of integrated circuit of reducing the cost of production of electronic circuits due to batch production can be easily visualized by a simple example. A standard 10 cm diameter wafer can be divided into approximately 8000 rectangular chips of sides 1 mm. Each IC chip may contain as few as tens of components to several thousand components. And if 10 such wafers are processed in one batch, we can make 80,000 ICs simultaneously. Many chips so produced will be faulty due to imperfection in the manufacturing process. Even if the yield (percentage of fault free chips/wafer) is only 20 percent, it can be seen that 16,000 good chips are produced in a single batch.

The fabrication of discrete devices such as transistor, diode or an integrated circuit in general can be done by the same technology. The various processes usually take place through a single plane and therefore, the technology is referred to as planar technology. A simple circuit of Fig. 1.3 when fabricated by silicon planar technology will have the cross-sectional view shown in Fig. 1.4.

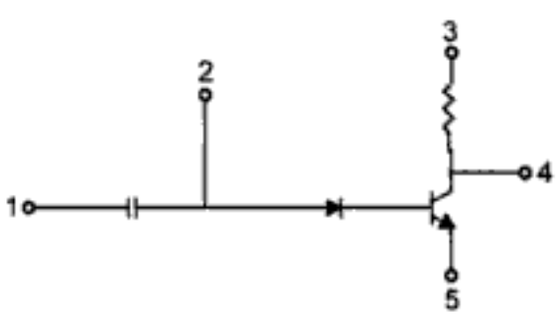


Fig. 1.3 A typical circuit

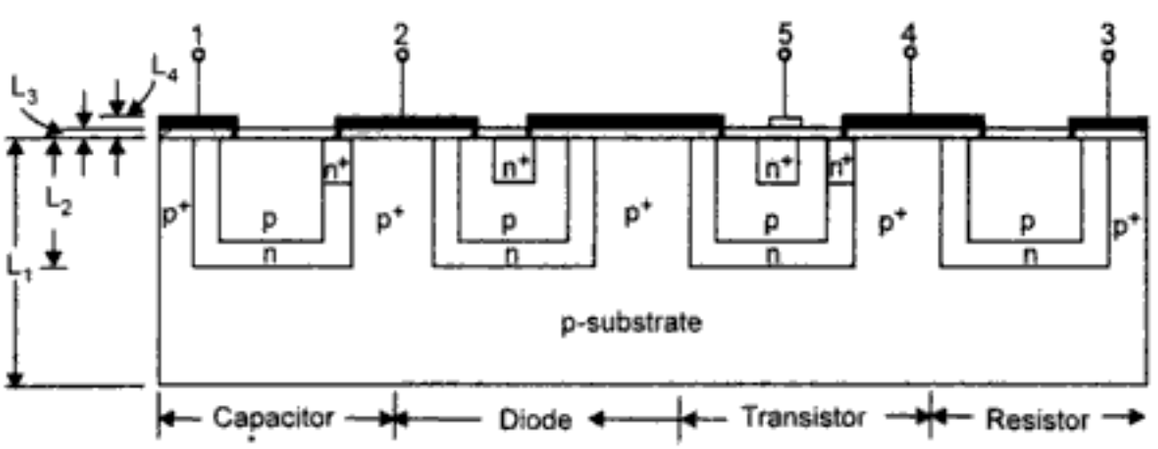


Fig. 1.4 Complete cross-sectional view of the circuit in Fig. 1.3 when transformed into monolithic form

An IC in general, consists of four distinct layers, as follows:

Layer No. 1 (~ 400 μm)	is a *p*-type silicon substrate upon which the integrated circuit is fabricated.
Layer No. 2 (~ 5–25 μm)	is a thin *n*-type material grown as a single crystal extension of the substrate using epitaxial deposition technique. All active and passive components are fabricated within this layer using selective diffusion of impurities.
Layer No. 3 (0.02–2μm)	is a very thin SiO_2 layer for preventing diffusion of impurities wherever not required using photolithographic technique.
Layer No. 4 (~ 1μm)	is an aluminium-layer used for obtaining interconnection between components.

It may be pointed out that the drawings showing the cross-sectional view in this chapter are never scale drawings, but are distorted for the particular emphasis required.

1.5 BASIC PLANAR PROCESSES

The basic processes used to fabricate ICs using silicon planar technology can be categorised as follows:

1. Silicon wafer (substrate) preparation
2. Epitaxial growth
3. Oxidation
4. Photolithography
5. Diffusion
6. Ion implantation
7. Isolation technique
8. Metallization
9. Assembly processing and packaging

We shall now describe these processes in detail

1.5.1 Silicon Wafer Preparation

The following steps are used in the preparation of Si-wafers

1. Crystal growth and doping
2. Ingot trimming and grinding
3. Ingot slicing
4. Wafer polishing and etching
5. Wafer cleaning

The starting material for crystal growth is highly purified (99.99999) polycrystalline silicon. The Czochralski crystal growth process is the most often used for producing single crystal silicon ingots. The polycrystalline silicon together with an appropriate amount of dopant

is put in a quartz crucible and is then placed in a furnace. The material is then heated to a temperature in excess of the silicon melting point of 1420°C. A small single crystal rod of silicon called a seed crystal is then dipped into the silicon-melt and slowly pulled out as shown in Fig. 1.5. As the seed crystal is pulled out of the melt, it brings with it a solidified mass of silicon with the same crystalline structure as that of seed crystal. During the crystal pulling process, the seed crystal and the crucible are rotated in opposite directions in order to produce ingots of circular cross-section. The diameter of the ingot is controlled by the pulling rate and the melt temperature. Ingot diameter of about 10 to 15 cm is common and ingot length is generally of the order of 100 cm.

Next the top and bottom portions of the ingot are cut off and the ingot surface is ground to produce an exact diameter (D = 10, 12.5, 15 cm). The ingot is also ground flat slightly along the length to get a reference plane. The ingot is then sliced using a stainless

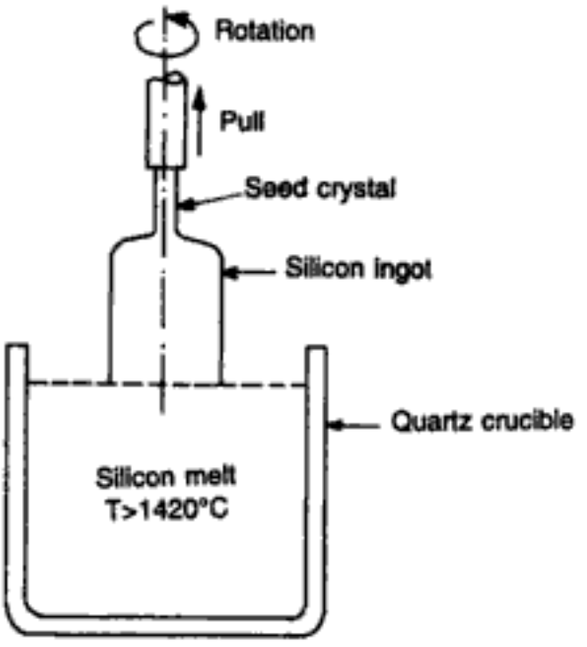


Fig. 1.5 Czochralski crystal growth

steel saw blade with industrial diamonds embedded into the inner diameter cutting edge. This produces circular wafers or slices as shown in Fig. 1.6. The orientation flat portion serves as a useful reference plane for the various processes described later. The silicon wafers so obtained have very rough surface due to slicing operation. These wafers undergo a number of polishing steps to produce a flat surface. Then one side of the wafer is given a final mirror-smooth highly polished finish, whereas the other side is simply lapped on an abrasive lapping machine to obtain an acceptable degree of flatness. Finally, the wafers are thoroughly rinsed and dried. A raw cut slice of thickness 23–40 mils produces wafers of 16–32 mils thickness after all the polishing steps.

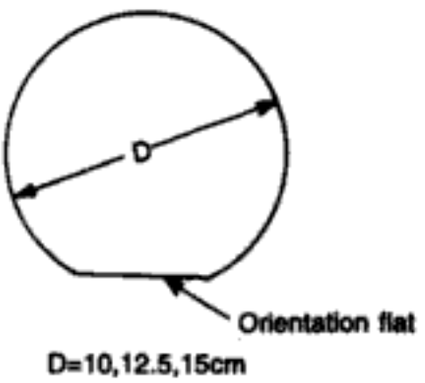


Fig. 1.6 Silicon wafer, D = 10, 12.5, 15 cm showing flat orientation

These silicon wafers will contain several hundred rectangular chips, each one containing a complete integrated circuit. After all the IC fabrication processes are complete, these wafers are sawed into 100 to 8000 rectangular chips having side of 10 to 1 mm. Each chip is a single IC and may contain hundreds of components. The wafer thickness therefore is so chosen that it is possible to separate chips without breaking and at the same time, it gives sufficient mechanical strength to the IC chip.

1.5.2 Epitaxial Growth

The word epitaxy is derived from Greek word *epi* meaning 'upon' and the past tense of the word *teinon* meaning 'arranged'. So, one could describe epitaxy as, arranging atoms in single crystal fashion upon a single crystal substrate, so that the resulting layer is an extension of the substrate crystal structure.

The basic chemical reaction used for the epitaxial growth of pure silicon is the hydrogen reduction of silicon tetrachloride.

$$SiC_4 + 2H_2 \underset{}{\overset{1200°C}{\rightleftharpoons}} Si + 4HCl$$

Mostly, epitaxial films with specific impurity concentration are required. This is accomplished by introducing phosphine (PH_3) for the n-type and bi-borane (B_2H_6) for p-type doping into the silicon-tetrachloride hydrogen gas stream.

The process is carried out in a reaction chamber consisting of a long cylindrical quartz tube encircled by an RF induction coil. Figure 1.7 shows the diagrammatic representation of the system used. The silicon wafers are placed on a rectangular graphite rod called a boat. This boat is then placed in the reaction chamber where the graphite is heated inductively to a temperature 1200°C. The various gases required for the growth of desired epitaxial layers are introduced into the system through a control console.

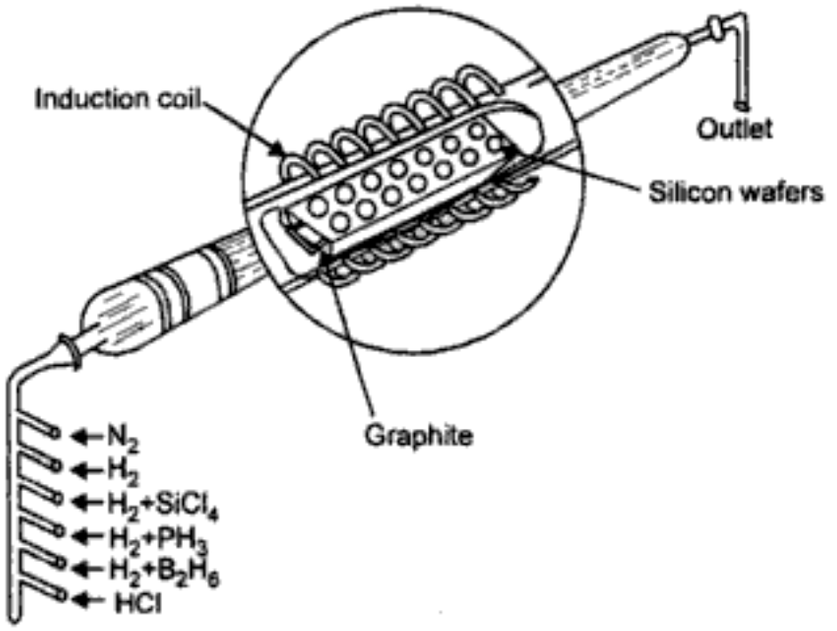


Fig. 1.7 A diagrammatic representation of a system for growing silicon epitaxial films

1.5.3 Oxidation

SiO_2 has the property of preventing the diffusion of almost all impurities through it. It serves two very important purposes.

1. SiO_2 is an extremely hard protective coating and is unaffected by almost all reagents except hydrofluoric acid. Thus it stands against any contamination.
2. By selective etching of SiO_2, diffusion of impurities through carefully defined windows in the SiO_2 can be accomplished to fabricate various components.

The silicon wafers are stacked up in a quartz boat and then inserted into quartz furnace tube. The Si-wafers are raised to a high temperature in the range of 950 to 1115°C and at the same time, exposed to a gas containing O_2 or H_2O or both. The chemical reaction is

$$Si + 2H_2O \longrightarrow SiO_2 + 2H_2$$

This oxidation process is called thermal oxidation because high temperature is used to grow the oxide layer. The thickness of the film is governed by time, temperature and the moisture content. The thickness of oxide layer is usually in the order of 0.02 to 2 μm.

1.5.4 Photolithography

With the help of photolithography, it has become possible to produce microscopically small circuit and device patterns on Si-wafers. As many as 10,000 transistors can be fabricated on a 1 cm × 1 cm chip. The

conventional photolithographic process uses ultraviolet light exposure and device dimension or line width as small as 2 μm can be obtained. However, with the advent of latest technology using X-ray or electron beam lithographic techniques, it has become possible to produce device dimension down to submicron range (< 1 μm).

Photolithography involves two processes, namely:
Making of a photographic mask
Photo etching

The making of a photographic mask involves the following sequence of operations—first the preparation of initial artwork and secondly, its reduction. The initial layout or artwork of an IC is normally done at a scale several hundred times larger than the final dimensions of the finished monolithic circuit. This is because, for a tiny chip, larger the artwork, more accurate is the final mask. For example, it is often required to make an opening of width about 1 mil (25 μm). Obviously, this cannot be managed by any draftsman even with his thinnest of sketch pens. So the drawings are made magnified and often by a factor of 500. With this magnification, it is easy to see that a width of one mil is magnified to a width of 500 mils, that is, about 1.2 cm. Therefore, for a finished monolithic chip of area 50 mil × 50 mil, the artwork will be made on an area of about 60 cm × 60 cm.

This initial layout is then decomposed into several mask layers, each corresponding to a process step in the fabrication schedule, e.g., a mask for base diffusion, another for collector diffusion, another for metallization and so on.

For photographic purpose, artwork should not contain any line drawings but must be of alternate clear and opaque regions. This is accomplished by the use of clear Mylar coated with a sheet of red photographically opaque mylar (trade name-Rubylith). The red layer can be easily peeled off thus exposing clear areas with a knife edge from the regions where impurities have to be diffused. The artwork is usually produced on a precision drafting machine, known as coordinatograph. The coordinatograph has a cutting head that can be positioned accurately and moved along two perpendicular axes. The coordinatograph outlines the pattern cutting through the red mylar without damaging the clear layer underneath.

This rubylith pattern of individual mask is photographed and then reduced in steps by a factor of 5 or 10 several times to finally obtain the exact image size. The final image also must be repeated many times in a matrix array, so that many ICs will be produced in one process. The photo repeating is done with a step and repeat camera. This is an imaging device with a photographic plate on a movable platform. Between exposure, the plate is moved in equal steps so that successive images form in an array. When the exposed plate is developed, it becomes a master mask. The masks, actually used in IC processing are made by contact printing from the master. These working masks wear out with use and are replaced as required.

Photo-etching is used for the removal of SiO_2 from desired regions so that the desired impurities can be diffused. The wafer is coated with a film of photosensitive emulsion (Kodak Photoresist KPR). The thickness of the film is in the range of 5000–10000 Å as shown in Fig. 1.8 (a). The mask negative of the desired pattern) as prepared by steps described earlier is placed over the photoresist coated wafer as shown in Fig. 1.8 (b). This is now exposed to ultraviolet light, so that KPR becomes polymerized beneath the transparent regions of the mask. The mask is then removed and the wafer is developed using a chemical (trichloroethylene) which dissolves the unexposed/ unpolymerized regions on the photoresist and leaves the pattern as shown in Fig. 1.8 (c). The polymerised photoresist is next fixed or cured, so that it becomes immune to certain chemicals called etchants used in subsequent processing steps. The chip is immersed in the etching solution of hydrofluoric acid, which removes the SiO_2 from the areas which are not protected by KPR as shown in Fig. 1.8 (d) After diffusion of impurities, the photoresist is removed with a chemical solvent (hot H_2SO_4) and mechanical abrasion.

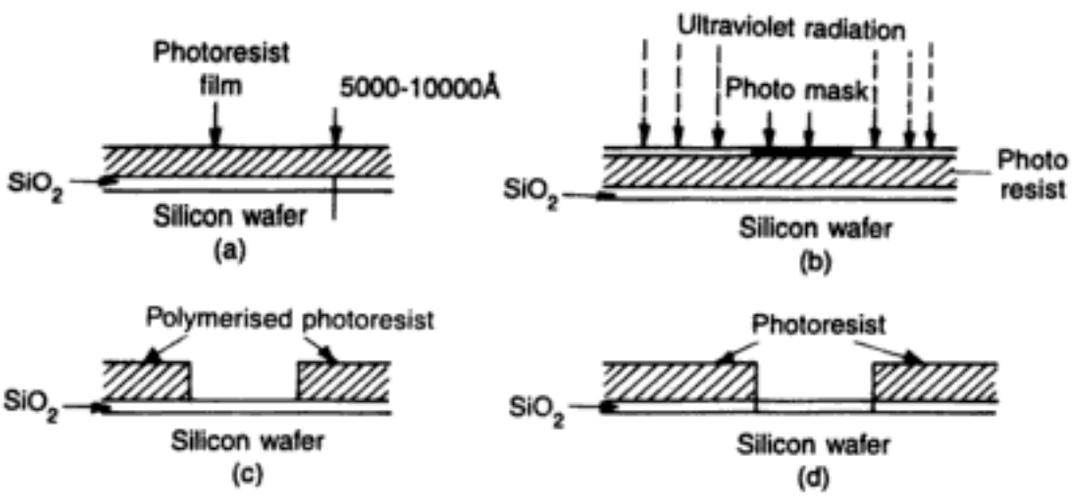


Fig. 1.8 Various steps for photo-etching

The etching process described is a wet etching process and the chemical reagents used are in liquid form. A new process used these days is a dry etching process called plasma etching. A major advantage of the dry etching process is that it is possible to achieve smaller line openings (≤ 1 μm) compared to wet process. Complete description of the plasma etching process is beyond the scope of this book.

X-Ray and Electron Beam Lithography

With conventional ultraviolet (UV) photolithography process in which the UV wavelengths used are in the range 0.3 to 0.4 μm, the minimum device dimensions or line widths are limited by diffraction effects to around five wavelengths or about 2 μm. This is what puts an upper limit on the IC device density using UV photolithography.

With the advent of X-ray and electron beam lithography techniques, it has become possible to produce device dimensions down to submicron range (< 1 μm). This is due to much shorter wavelengths involved. With these techniques, MOSFET with gate length as small as 0.25 μm have been made. The cost of X-ray or electron beam equipment is very high and the exposure times very much longer than with UV photolithography. So this becomes a very expensive process and is used only when very small device dimensions (≤ 1 μm) are needed.

1.5.5 Diffusion

Another important process in the fabrication of monolithic ICs is the diffusion of impurities in the Silicon chip. This uses a high temperature furnace having a flat temperature profile over a useful length (about 20″ length). A quartz boat containing about 20 cleaned wafers is pushed into the hot zone with temperature maintained at about a 1000°C. Impurities to be diffused are rarely used in their elemental forms. Normally, compounds such as B_2O_3 (Boron oxide), BCl_3 (Boron chloride) are used for Boron and P_2O_5 (Phosphorous pentaoxide) and $POCl_3$ (Phosphorous oxychloride) are used as sources of Phosphorous. A carrier gas, such as dry oxygen or nitrogen is normally used for sweeping the impurity to the high temperature zone. The depth of diffusion depends upon the time of diffusion which normally extends to 2 hours.

The diffusion of impurities normally takes place both laterally as well as vertically. Therefore, the actual junction profiles will be curved as shown in Fig. 1.9. However, for the sake of simplicity, lateral diffusion will be omitted in all the drawings.

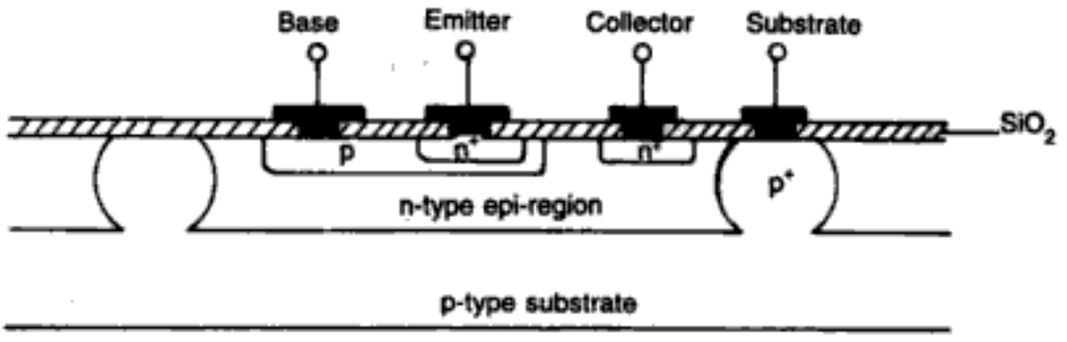


Fig. 1.9 The cross-section of an *npn* transistor showing curved junction profiles as a result of lateral diffusion

1.5.6 Ion Implatation

Ion implantation is the other technique used to introduce impurities into a silicon wafer. In this process, silicon wafers are placed in a vacuum chamber and are scanned by a beam of high-energy dopant ions (borons for *p*-type and phosphorus for *n*-type) as shown in Fig. 1.10. These ions are accelerated by energies between 20 kV to 250 kV.

As the ions strike the silicon wafers, they penetrate some small distance into the wafer. The depth of penetration of any particular type of ion increases with increasing accelerating voltage. Ion implantation technique has two important advantages.

1. It is performed at low temperatures. Therefore, previously diffused regions have a lesser tendency for lateral spreading.
2. In diffusion process, temperature has to be controlled over a large area inside the oven, whereas in ion implantation technique, accelerating potential and the beam current are electrically controlled from outside.

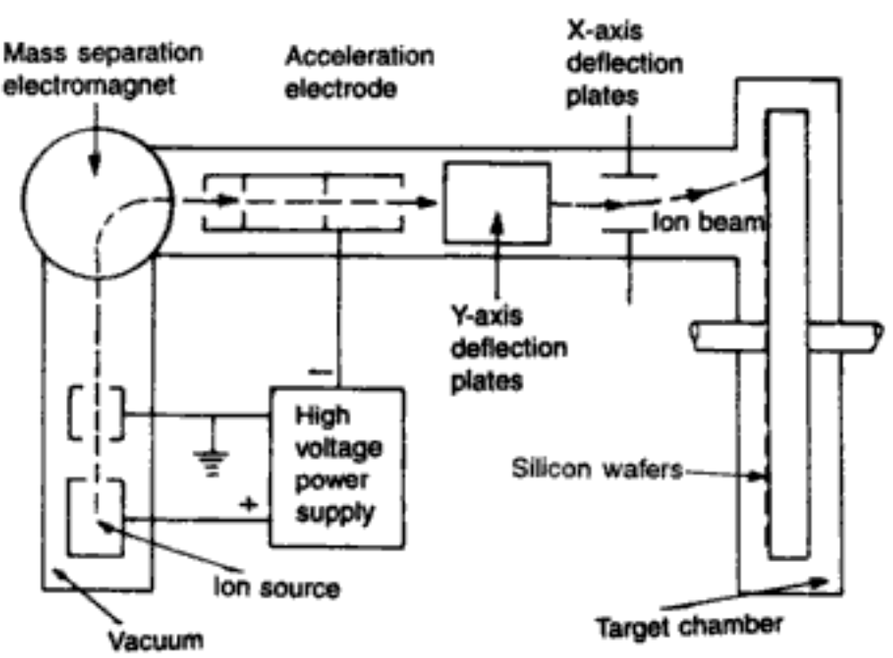


Fig. 1.10 Ion implantation system

1.5.7 Isolation Techniques

Since a number of components are fabricated on the same IC chip, it becomes necessary to provide electrical isolation between different components and interconnections. Various types of isolation techniques have been developed. However, we shall discuss here only two commonly used techniques namely:

pn junction isolation
Dielectric isolation

p-n Junction Isolation

In this isolation technique, p^+ type impurities are selectively diffused into the n-type epitaxial layer so as to reach p-type substrate as shown in Fig. 1.11 (a). This produces islands surrounded by p-type moats. It can be seen that these regions are separated by two back-to-back p-n junction diodes. If the p-type substrate material is held at the most negative potential in the circuit, the diodes will be reverse

biased providing electric isolation between these islands. The different components are fabricated in these isolation islands. The concentration of the acceptor atoms in the region between isolation islands is usually kept much higher (p^+) than the p-type substrate. This prevents the depletion region of the reverse biased diode from penetrating more into p^+ region and possibly connecting the isolation islands.

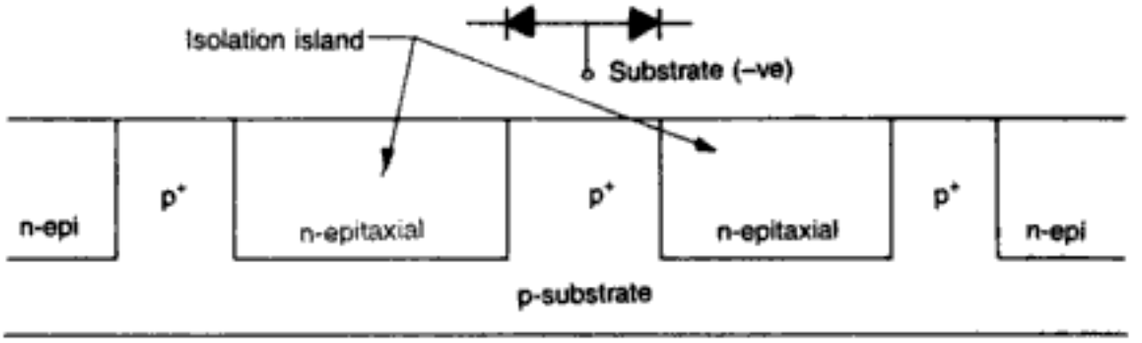


Fig. 1.11 (a) *p-n* junction isolation

There is, however, one undesirable by-product of this isolation process. It is the presence of a transition capacitance at the isolating *pn* junctions, resulting in an inevitable capacitor coupling between the components and the substrate. These parasitic capacitances limit the performance of the circuit at high frequencies. But being economical, this technique is commonly used for general purpose ICs.

Dielectric Isolation

Here a layer of solid dielectric such as silicon dioxide or ruby completely surrounds each component, thereby producing isolation, both electrical and physical. This isolating dielectric layer is thick enough so that its associated capacitance is negligible. Also, it is possible to fabricate both *pnp* and *npn* transistor within the same silicon substrate. Since this method requires additional fabrication steps, it becomes more expensive. The technique is mostly used for fabricating professional grade ICs required for specialised applications viz, aerospace and military, where higher cost is justified by superior performance. Figure 1.11 (b) shows such a structure.

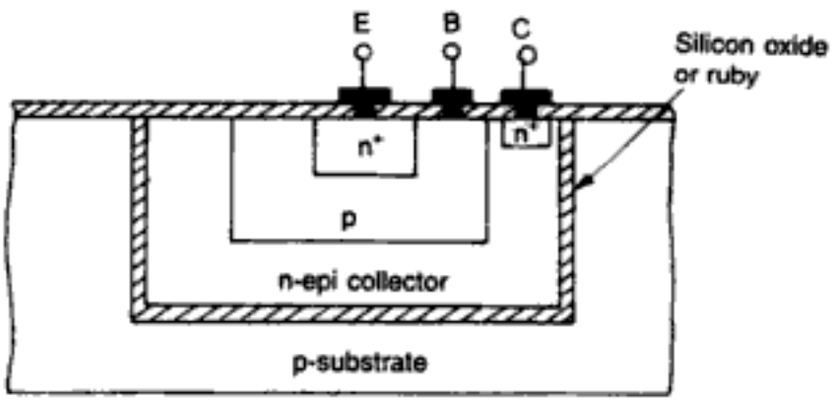


Fig. 1.11 (b) Dielectric isolation

1.5.8 Metallization

The purpose of this process is to produce a thin metal film layer that will serve to make interconnections of the various components on the chip. Aluminium is usually used for the metallization of most ICs as it offers several advantages.

1. It is relatively a good conductor.
2. It is easy to deposit aluminium films using vacuum deposition.
3. Aluminium makes good mechanical bonds with silicon.
4. Aluminium forms low resistance, non-rectifying (i.e. ohmic) contact with *p*-type silicon and the heavily doped *n*-type silicon.

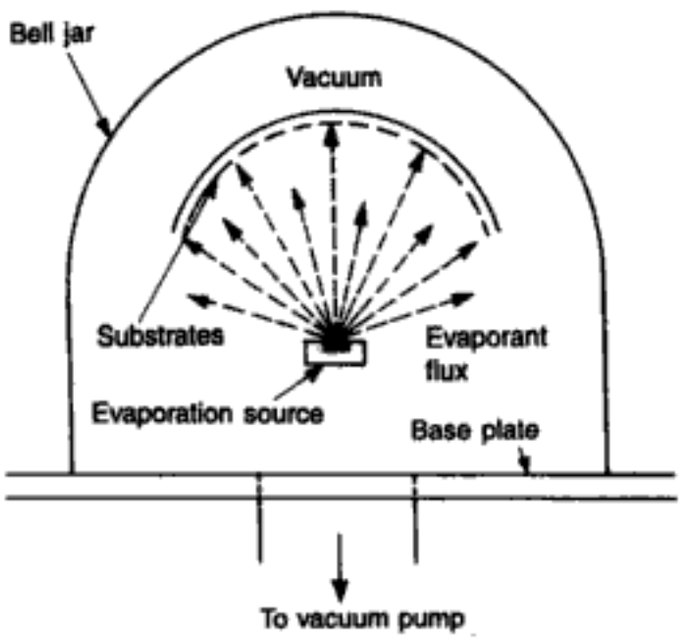


Fig. 1.12 Vacuum evaporation for metallization

The film thickness of about 1 μm and conduction width of about 2 to 25 μm are commonly used. The process takes place in a vacuum evaporation chamber as shown in Fig. 1.12. The pressure in the chamber is reduced to the range of about 10^{-6} to 10^{-7} torr (1 atmosphere = 760 torr = 760 mm Hg). The material to be evaporated is placed in a resistance heated tungsten coil or basket. A very high power density electron beam is focussed at the surface of the material to be evaporated. This heats up the material to very high temperature and it starts vaporizing. These vapors travel in straight line paths. The evaporated molecules hit the substrate and condense there to form a thin film coating.

After the thin film metallization is done, the film is patterned to produce the required interconnections and bonding pad configuration. This is done by photolithographic process and aluminium is etched away from unwanted places by using etchants like phosphoric acid (H_3PO_4).

1.5.9 Assembly Processing and Packaging

Each of the wafer processed contains several hundred chips, each being a complete circuit. So these chips must be separated and individually packaged. A common method called scribing and cleaving used for separation makes use of a diamond tipped tool to cut lines into the surface of the wafer along the rectangular grid separating the individual chips. Then the wafer is fractured along the scribe lines and the individual chips are physically separated. Each chip is then mounted on a ceramic wafer and attached to a suitable package.

There are three different package configurations available.

1. TO-5 glass metal package
2. Ceramic flat package
3. Dual-in-line (ceramic or plastic type)

TO-5 packages are available in 8, 10 or 12 leads, whereas the flat or dual-in-line package is commonly available in 8, 14 or 16 leads, but

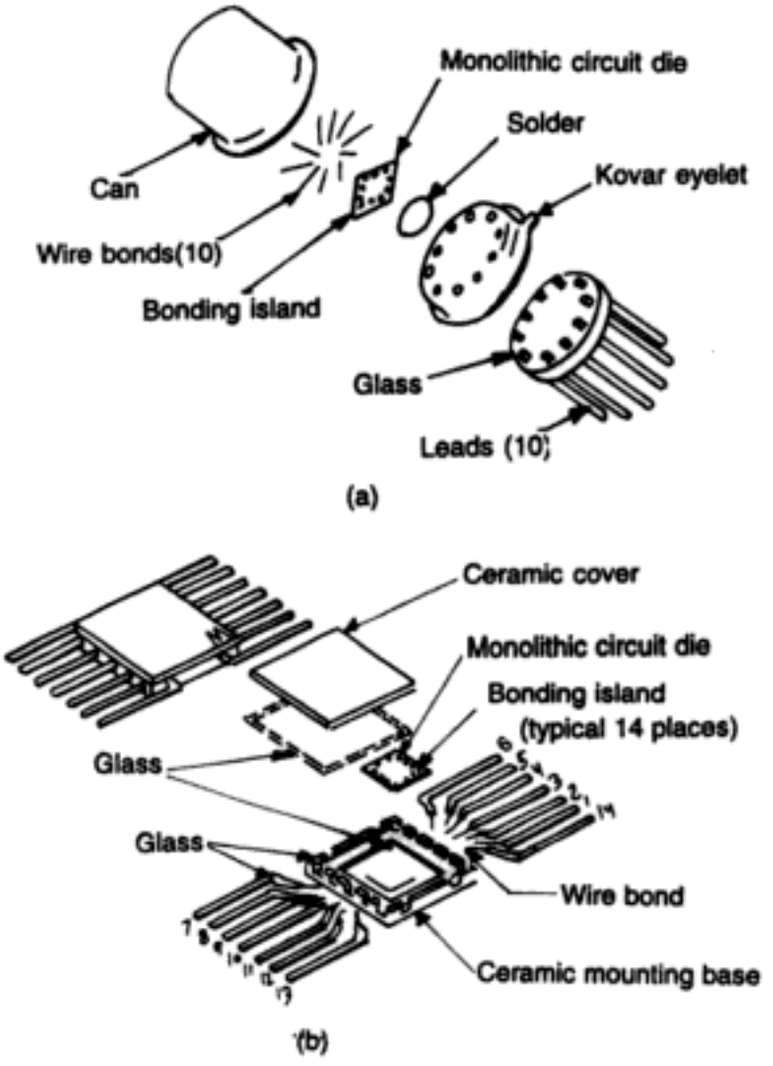


Fig. 1.13 Exploded view of (a) lead TO-5 package (b) 14-lead version of the flat package, showing the various components as well as the completed flat package

even 24 or 36 or 42 leads are also available for special circuits. Ceramic packages, whether of flat type or dual-in-line are costly due to fabrication process, but have the advantage of best hermetic sealing. Most of the general purpose ICs are dual-in-line plastic packages due to economy. Figure 1.13 (a, b) shows the exploded view of TO-5 and flat package.

1.6 FABRICATION OF A TYPICAL CIRCUIT

We shall here show the various steps utilized in converting the circuit of Fig. 1.3 into the monolithic IC of Fig. 1.4.

Step-1: Wafer Preparation

Refer Fig. 1.14 (a). The starting material called the substrate is a *p*-type silicon wafer prepared as discussed in Sec. 1.5.1. The wafers are usually of 10 cm diameter and 0.4 mm(~ 400 μm) thickness. The resistivity is approximately 10 Ω-cm corresponding to concentration of acceptor atom, $N_A = 1.4 \times 10^{15}$ atoms/cm^3.

Step-2: Epitaxial Growth

An *n*-type epitaxial film (5–25 μm) is grown on the *p*-type substrate as shown in Fig. 1.14 (b). The ultimately becomes the collector region of the transistor, or an element of the diode and diffused capacitor associated with the circuit. So in general it can be said that all active and passive components are fabricated within this layer. The resistivity of *n*-epitaxial layer is of the order of 0.1 to 0.5 Ω-cm.

Step 3: Oxidation

Refer Fig. 1.14 (c) A SiO_2 layer of thickness of the order of 0.02 to 2 μm is grown on the *n*-epitaxial layer.

Step 4: Isolation Diffusion

In the circuit of Fig. 1.3 four components have to be fabricated, so we require four islands which are isolated. For this, SiO_2 is removed from five different places using photolithographic technique. Refer Fig. 1.14 (d). The wafer is next subjected to heavy *p*-type diffusion for a long time interval so that *p*-type impurities penetrate the *n*-type epitaxial layer and reach the *p*-type substrate. The area under the SiO_2 are *n*-type islands that are completely surrounded by *p*-type moats. As long as the *pn* junctions between the isolation islands are held at reverse bias, that is, the *p*-type substrate is held at a negative potential with respect to the *n*-type isolation islands, these regions are electrically isolated from each other by two back-to-back diodes, providing the desired isolation.

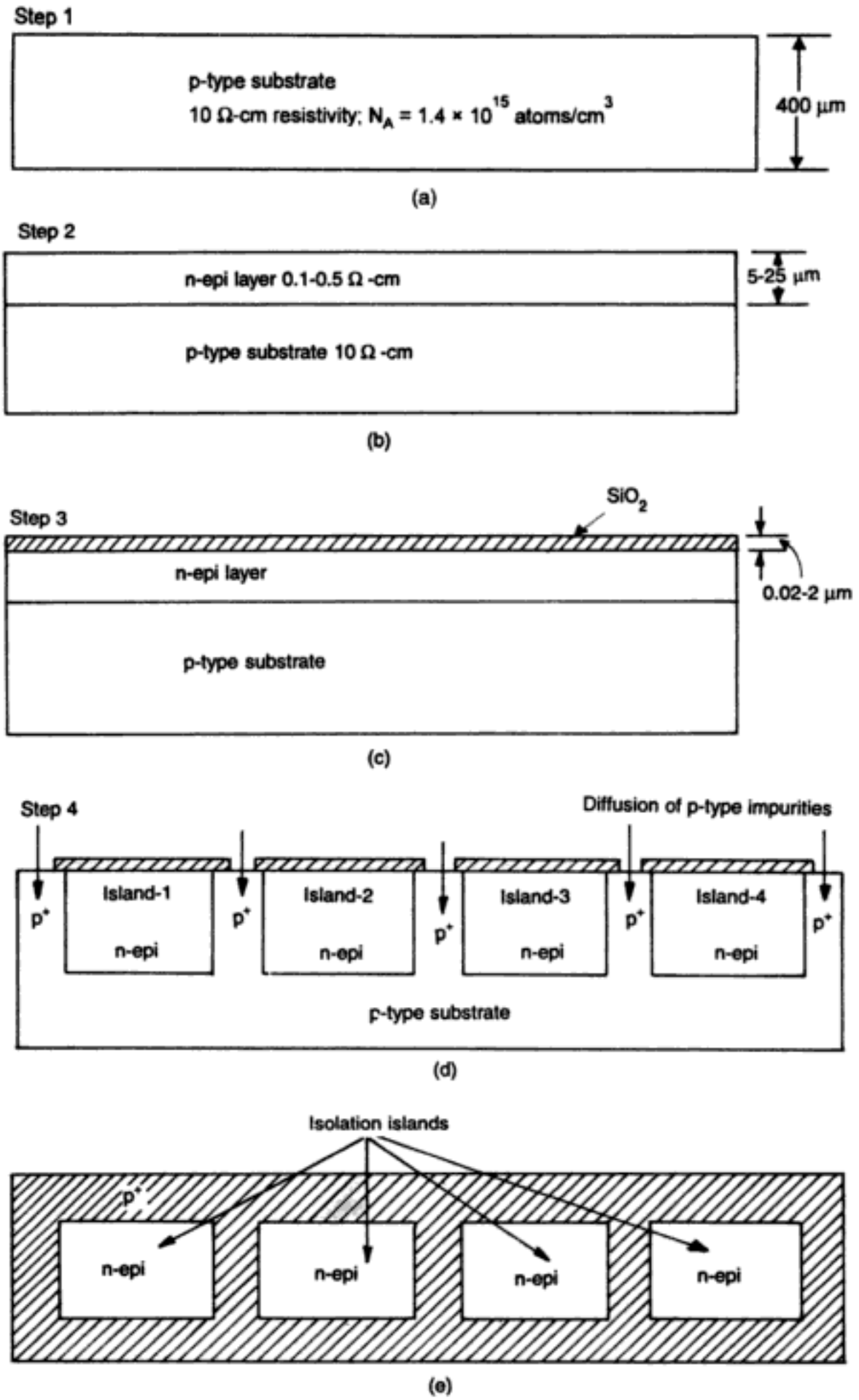


Fig. 1.14 (a-e) Steps in the fabrication of the circuit shown in Fig. 1.3

The concentration of acceptor atoms ($N_A \simeq 5 \times 10^{20}$ cm^{-3}) in the region between isolation islands is generally kept higher than p-type substrate for which $N_A = 1.4 \times 10^{15}$ atoms/cm^3. This ensures that the depletion region of the reverse biased diode will not extend into p^+ region to the extent of electrically connecting the two isolation islands. There will, however, be a significant amount of barrier or transition capacitance present as a by product of the isolation diffusion. The top view of the isolation islands is depicted in Fig. 1.14 (e).

Step 5: Base Diffusion

Refer to Fig. 1.14 (f). A new layer of SiO_2 is grown over the entire wafer and a new pattern of openings is formed using photolithographic technique. Now, p-type impurities, such as boron, are diffused through the openings into the islands of n-type epitaxial silicon. The depth of this diffusion must be controlled so that it does not penetrate through n-layer into the substrate. This diffusion is utilized to form base region, of the transistor, resistor, the anode of the diode and junction capacitor.

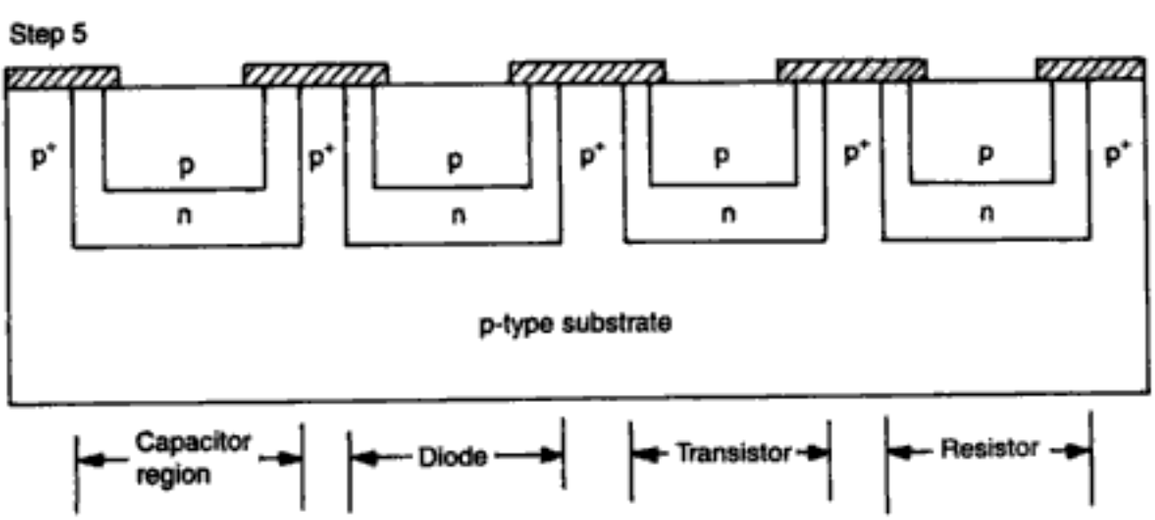


Fig. 1.14 (f)

Step 6: Emitter Diffusion

Refer to Fig. 1.14 (g). A new layer of SiO_2 is again grown over the entire wafer and selectively etched to open a new set of windows and n-type impurity (phosphorus) is diffused through them. This forms transistor emitter and cathode region of diode.

Windows (W_1, W_2 etc.) are also etched into n-region where contact is to be made to the n-type layer. Heavy concentration of phosphorus (n^+) is diffused into these regions simultaneously with the emitter diffusion. The reason for using heavily doped n-regions can be explained as follows:

Aluminium, normally used for making interconnections, is a *p*-type impurity in silicon, and can produce an unwanted rectifying contact with the lightly doped *n*-material. However, heavy concentration of phosphorous (~ 2×10^{20} cm^{-3}) doping causes a high degree of damage to the Si-lattice at the surface, thus effectively making it semi-metallic. This n^+ layer thus makes a good ohmic contact with the Al-layer. The top view corresponding to Fig. 1.14 (g) is shown in Fig. 1.14 (h).

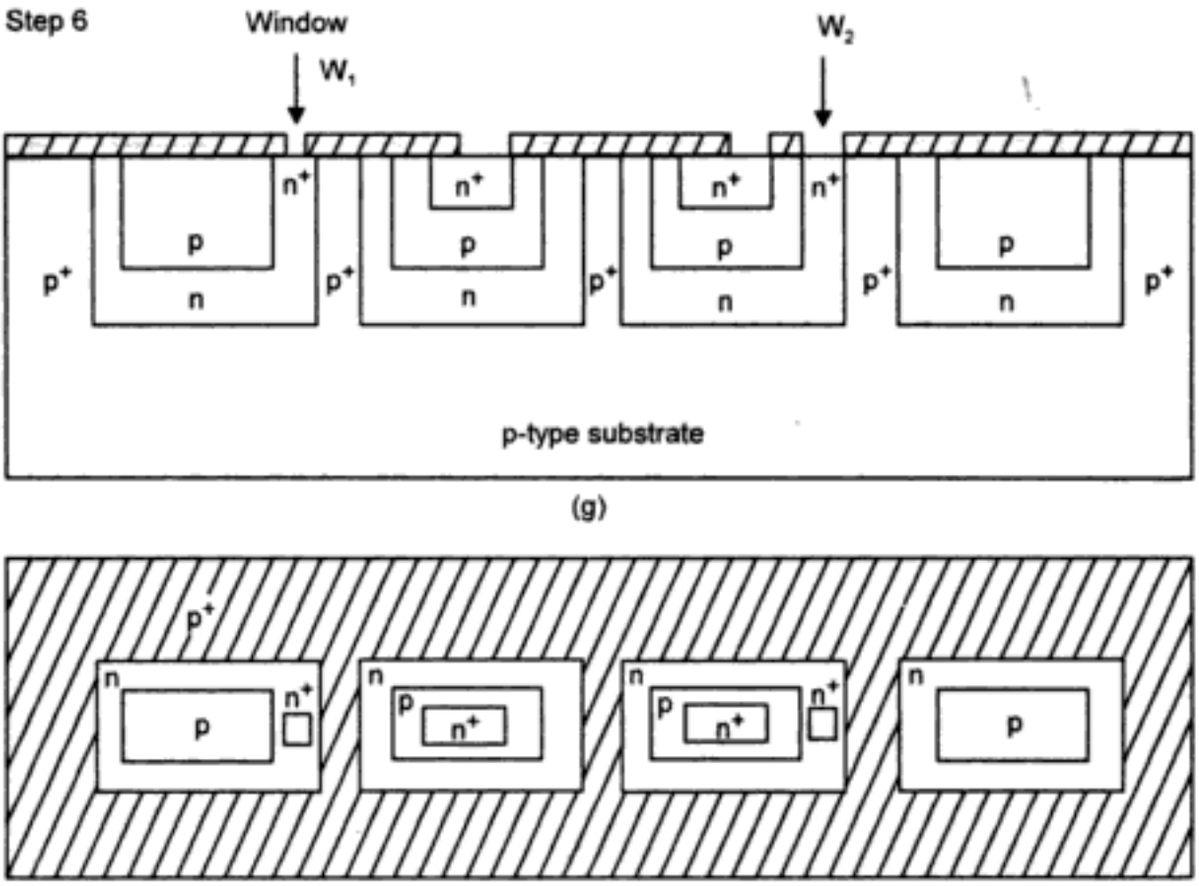


Fig. 1.14 (g-h)

Step 7: Aluminium Metallization

Now the IC chip is complete with all the active and passive devices and only interconnections between the various components have to be made in accordance with the circuit in Fig. 1.3. The chip is further subjected to the process of the formation of a new SiO_2 layer and masked etching to open a new set of windows at the points where contacts have to be made.

Now, a thin even coating of aluminium is vacuum-deposited over the entire surface of the wafer. The interconnection pattern between the components is then formed by photo resist techniques. The undesired aluminium areas are etched away leaving a pattern of interconnections between transistor, resistor, diode and capacitor as shown by the cross-sectional and top view in Fig. 1.14 (i) and Fig. 1.14 (j) respectively.

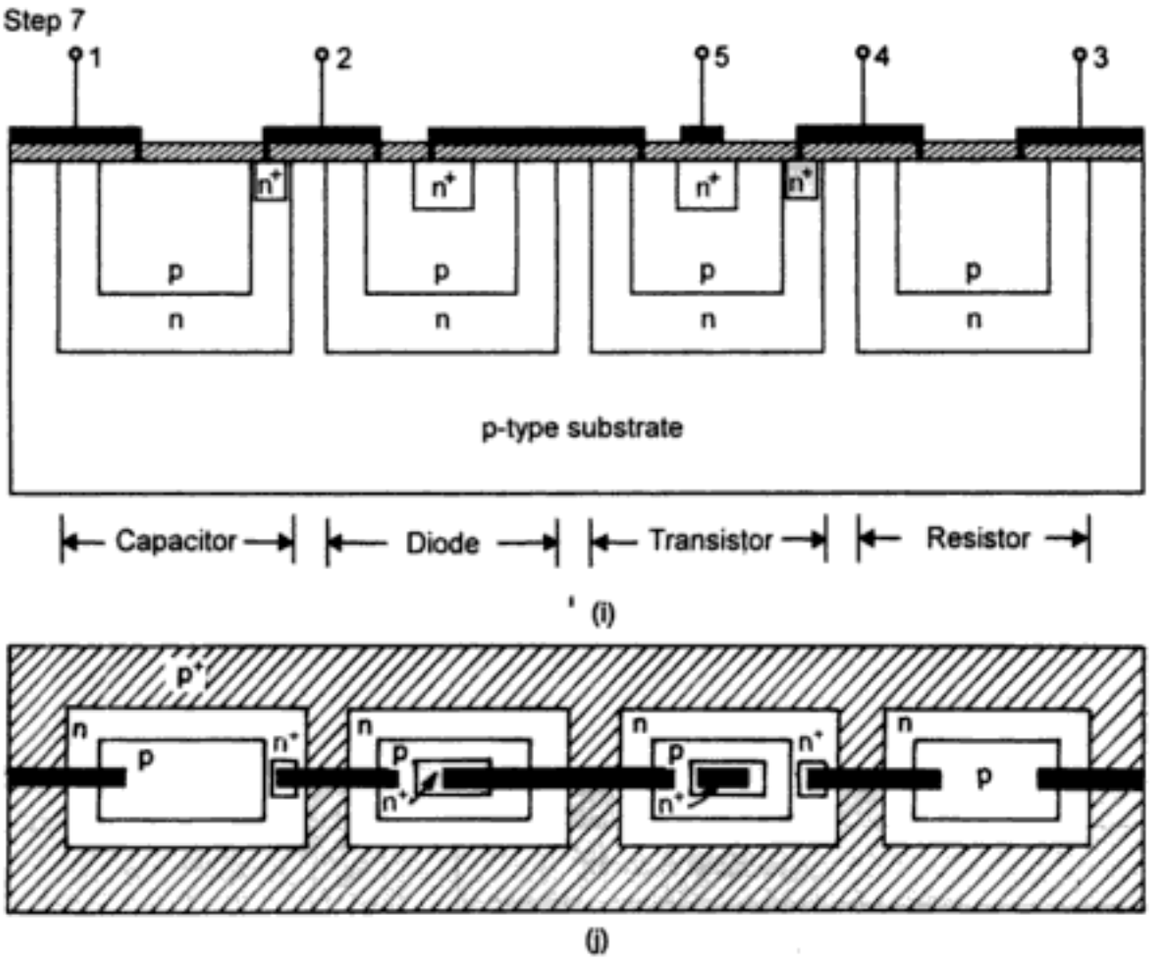


Fig. 1.14 (i, j)

1.7 ACTIVE AND PASSIVE COMPONENTS OF ICs

Now the reader is familiar with the basic technology involved in the fabrication of ICs. More light will be thrown on the various devices which constitute a monolithic circuit. These include:

1. Transistors
2. Diodes
3. Resistors
4. Capacitors
5. Inductors.

1.7.1 Monolithic Transistors

Figure 1.15 (a) shows the cross-sectional view of an IC transistor. Let us compare it with the conventional discrete transistor also fabricated using planar technology and shown in Fig. 1.15 (b).

The most striking feature in the two structures is that in the IC transistor, collector contact is on the top whereas in the discrete transistor it is at the bottom. In IC transistor, collector contact has to be taken from the top because collector is isolated from the substrate and the next isolation island by reverse-biased diodes. This structural

difference makes an integrated transistor poorer than discrete transistor in two ways:

(i) Collector contact being at the top increases the collector current path, thereby increasing the collector series resistance and hence $V_{CE\,(sat)}$ of the device.

(ii) In the integrated transistor, additional parasitic capacitance appears between collector and substrate is held at negative potential. However, these shortcomings of the integrated transistors can be overlooked on account of a number of advantages inherent in integrated technology. In this, circuit performance is highly improved as matched transistors can be obtained for example to be used in difference amplifiers. Integrated transistors spaced within 30 mils can have V_{BE} matching better than 5 mV and h_{FE} match of ± 10 percent.

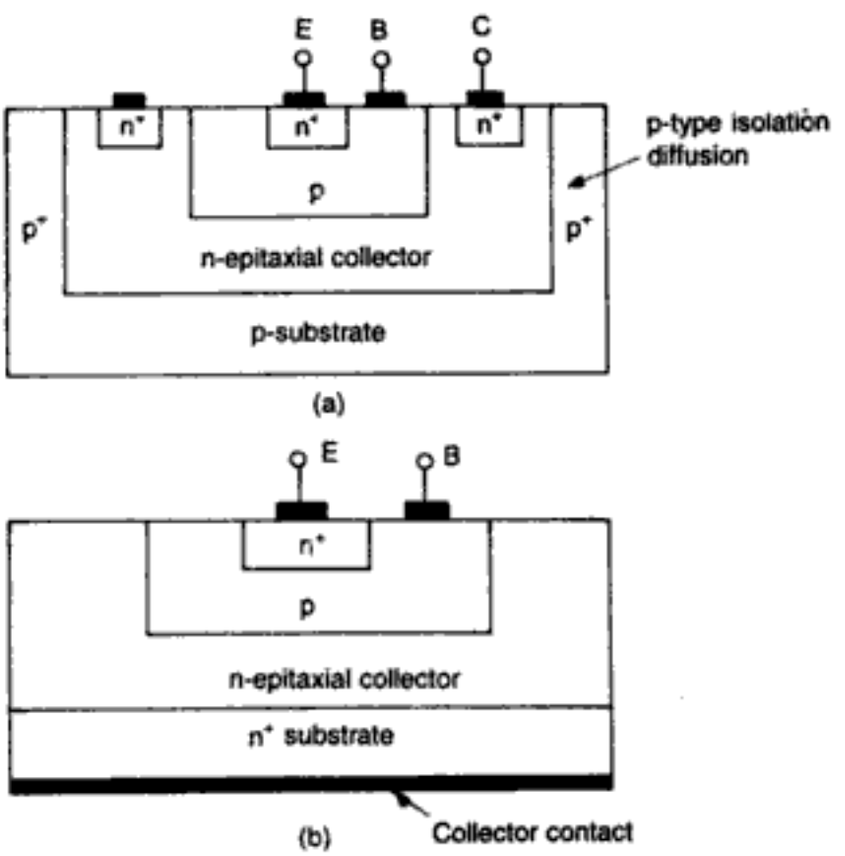


Fig. 1.15 Cross-section of (a) Monolithic integrated circuit transistor, (b) a discrete planar epitaxial transistor

Use of 'Buried n⁺ Layer' to reduce Collector Series Resistance

The higher collector series resistance of an integrated transistor can be easily reduced by a process known as 'buried layer' shown in Fig. 1.16. In this, a heavily doped n^+ region is sandwiched between the n-type epitaxial collector and p-type substrate. This buried n^+ region provides a low resistivity current path from the active collector region (n-type layer) to the collector contact (n^+ contact layer). In effect, the n^+ layer shunts the n-layer of the collector region with respect to the flow of the current thus effectively reducing the collector resistance.

pnp Transistor

pnp transistors in integrated circuits are fabricated in one of the following three ways:

Vertical or substrate *pnp*
Lateral *pnp*
Triple diffused *pnp*

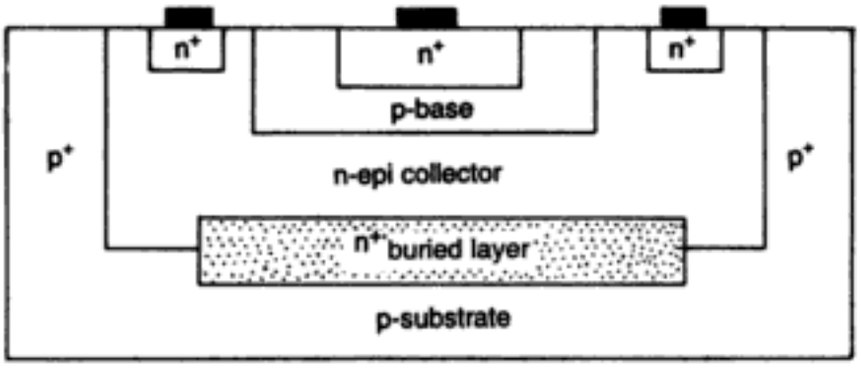


Fig. 1.16 Use of "buried n^+ layer" to reduce collector series resistance

Vertical pnp Transistor

The *p*-type substrate itself is used as *p*-collector, *n*-epitaxial layer for the base and the next *p*-diffusion (base in *npn* structure) as the emitter region. This type of *pnp* transistor has the limitation that collector has to be held at a fixed negative potential, as substrate is to be held at the most negative potential in the circuit for providing good isolation.

Lateral pnp-Transistor

This is the most common form of an integrated *pnp* transistor which can be fabricated simultaneously with the *npn* transistor and requires no additional masking or diffusion step. The *n*-type epi layer is used as the base of the *pnp* transistor. During the *p*-type base diffusion for the *npn* transistor, two adjacent *p*-regions are diffused to form emitter and collector regions of the lateral *pnp* transistor as shown in Fig. 1.17.

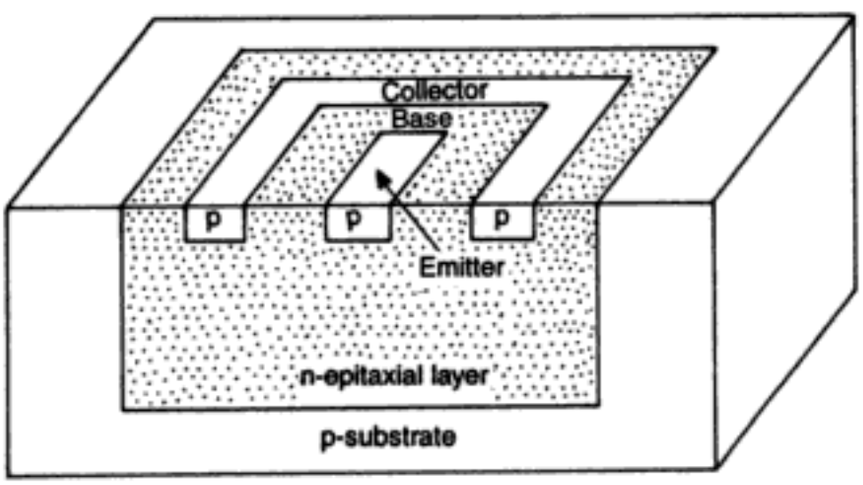


Fig. 1.17 A *pnp* lateral transistor

Triple Diffused pnp Transistor

If to a standard *npn* transistor, an extra *p*-type diffusion is added after the *n*-diffusion, it is quite possible to obtain a *pnp* transistor and is known as triple diffused *pnp* transistor. However the usefulness of such a structure is limited due to additional fabrication steps required and serious design considerations.

Comparison of npn and pnp IC Transistors

In general, *npn* transistors are preferred in integrated circuits compared to *pnp* transistors due to a variety of reasons.

1. A vertical *pnp* transistor has the disadvantage that its collector has to be held at a fixed negative voltage.
2. Lateral *pnp* transistor has inferior characteristic as the base width is usually larger controlled by lateral diffusion of p-type impurities and photographic limitations during mask making and alignment. Therefore, *pnp* transistor normally gives current gain as low as 1.5 to 30 compared to 50 to 300 for the *npn* transistor. With improved technology, however, it has now been possible to increase the gain to 100.
3. We know that collector region is heated during base and emitter diffusions, so the diffusion coefficient of the collector impurities should be as small as possible to avoid the movement of the collector junction. Since *n*-type impurities have smaller diffusion constant than *p*-type impurities, the *n*-type collector moves very little while *p*-type moves appreciably. This makes the *npn* transistor superior in performance with relatively easier process control.

Multi-emitter Transistor

In many applications such as transistor-transistor logic (TTL), we need multiemitter transistor of the type shown in Fig. 1.18 (a). The cross-sectional view of such a transistor is shown in Fig. 1.18 (b) where n^+ emitter is diffused at three places in the *p*-type base. Thus it is possible to save chip area and enhance component density of an IC.

The Schottky Transistor

In digital circuits, many times it is desired that the switching should be very fast. This can be achieved if the transistor is prevented from entering into saturation. Figure 1.19 (a) shows such an arrangement where a Schottky diode (Sec. 1.7.2) is used as a clamp between the base and collector.

If base current is increased to saturate the transistor, the voltage at the collector drops thereby making diode D conduct. As soon as diode D conducts, the base to collector voltage drops to about 0.4 V

which is less than the cut-in voltage for Si-base to collector junction ($\simeq$ 0.5 V), so that the transistor does not enter into saturation.

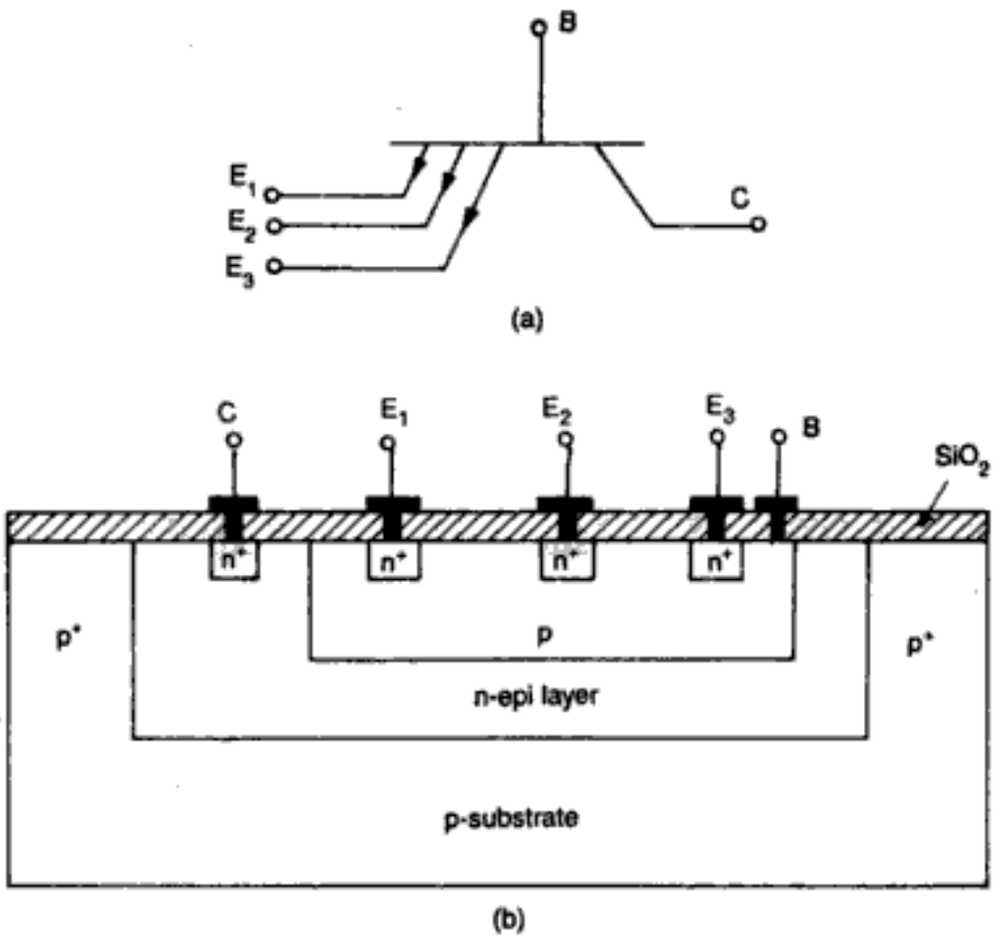


Fig. 1.18 (a) Multi-emitter transistor, (b) Cross-sectional view of a multi-emitter transistor

Figure 1.19 (b, c) shows the cross-sectional view of a Schottky transistor, and its symbol. A Schottky diode is formed between base and collector by allowing Al-metallization for the base lead to make contact with the n-type collector region. This is discussed in detail in Sec. 1.7.2.

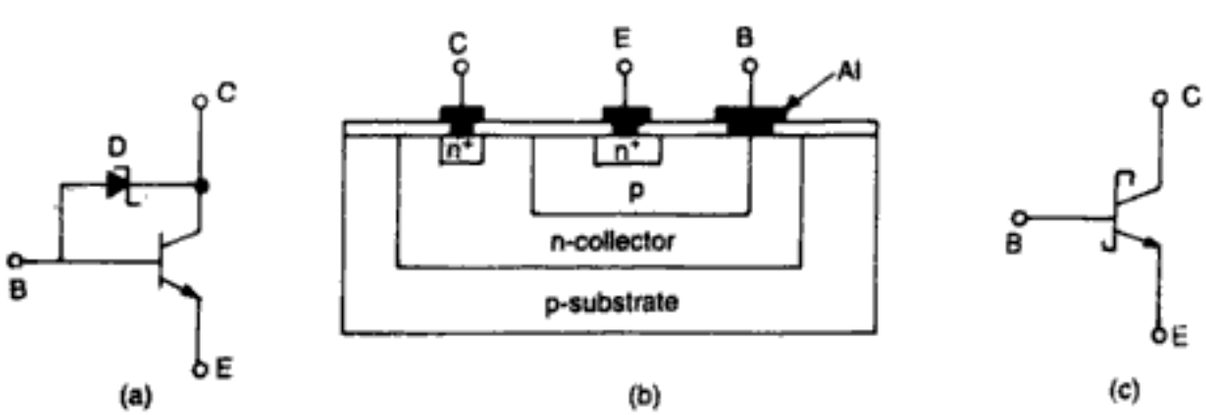


Fig. 1.19 (a) A transistor with a Schottky-barrier diode clamped between base and collector to prevent saturation, (b) Cross-section of a Schottky-barrier transistor, (c) Symbolic representation

1.7.2 Monolithic Diodes

Diodes find extensive use in integrated circuits, especially in digital applications. Figure 1.20 shows five different possible connections by which a transistor could be utilized as a diode. These configurations have slightly different characteristics as depicted in Table. 1.1 and the choice of the diode depends upon the application and circuit performance desired.

Table 1.1 Summary of typical values for various diode connections

Characteristic	*(a)* $V_{CB} = 0$	*(b)* $V_{CE} = 0$	*(c)* $V_{EB} = 0$	*(d)* $I_C = 0$	*(e)* $I_E = 0$
Breakdown voltage in volts	7	7	55	7	55
Storage time, n sec	9	100	53	56	85
Forward voltage in volts	.85	.92	.94	.96	.95

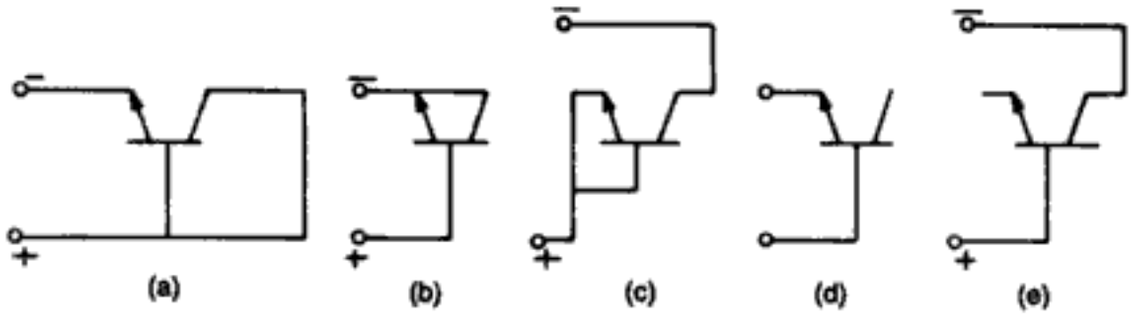


Fig. 1.20 Cross-section of various diode structures

It can be seen that diode 'a' is most useful for getting high speed diode to be used in digital integrated circuit due to its lowest storage time and lowest forward voltage drop. Diodes 'b' and 'd' can be utilized as a stored charge device as this feature gives a high speed turn-off of the transistor. Diode 'c' and 'e' have the advantage of highest breakdown voltage.

Schottky Barrier Diode

Metal to semiconductor junctions can be ohmic as well as rectifying. The ohmic contact is used when a lead is to be attached to a semiconductor device. And a rectifying contact called a metal semiconductor diode, (also called Schottky barrier diode) has characteristics very similar to an ordinary *pn* diode.

As already mentioned aluminium is a *p*-type impurity in silicon. So when it is used to make a contact with *n*-type Si, it is essential that contact is ohmic and no *pn* junction is formed. This is done by making n^+ diffusions in the n regions near the surface where Al is deposited. On the other hand, if Al is deposited directly upon the *n*-type Si, a metal semiconductor diode is formed. It is found that such a metal semiconductor diode has essentially the same type of V-I charcteristics as an ordinary *pn* junction, though the physical mechanism is very different and complicated.

Figure 1.21 (a) shows two contacts, where contact 1 is a Schottky barrier and contact 2 is an ohmic contact. The symbolic representation of a schottky diode is shown in Fig. 1.21 (b). The contact potential between the semiconductor and the metal creates a barrier to the flow of conduction electrons from semiconductor to metal. Forward biasing the junction lowers this barrier and permits electron flow from semiconductor to metal where electrons are abundant. Note that the majority carrier electrons carry current in a Schottky diode. On the other hand, in a *pn* junction diode, current is due to minority carriers and such a diode shows a substantial time delay from ***on*** to ***off***, as the minority carriers stored in the junction have to be totally removed. In this sense, Schottky diode exhibit negligible storage time, since electrons from the *n*-type Si enter the Al almost right at the contact surface, where they mix with the free electrons and are not stored.

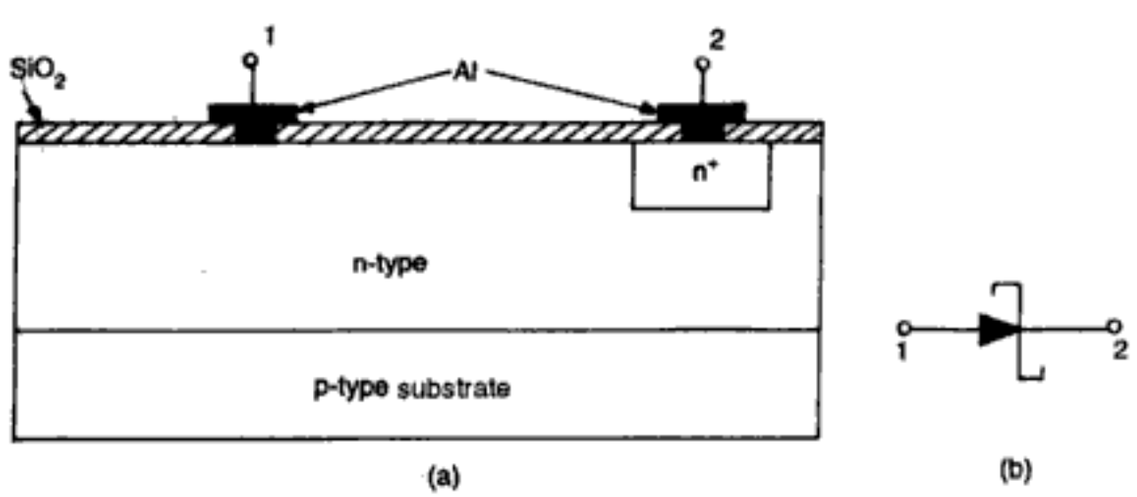


Fig. 1.21 (a) A Schottky diode, (b) Symbol for metal semiconductor diode

Another significant advantage of this type of diode is that it has less forward voltage ($V_\gamma \simeq 0.3V$) when compared to that of *pn* diode ($V_\gamma = 0.6V$). Thus it can be used for more ideal clamping, or as detectors in high frequency and microwave ICs.

1.7.3 Integrated Resistors

The basic technique for obtaining a resistor in integrated circuit is by utilising the bulk resistance of a defined volume of semicondector region. Four different methods are available for fabricating integrated resistors, namely:

Diffused Resistor
Epitaxial Resistor
Pinched Resistor
Thin Film Resistor

Diffused Resistor

In this method, resistor is formed in one of the isolated regions of epitaxial layer during base or emitter diffusion common to bipolar transistor fabrication. As no extra fabricating steps are required, this type of resistor is very economical. However, a severe limitation is the small range of resistances possible.

The value of the resistance depends upon the surface geometry. That is, length, width and upon the diffused impurity profile. In this context, a very useful quantity sheet resistance is defined as diffused layers are very thin.

Sheet Resistance R_S

Consider the square $L \times L$ of a material of resistivity ρ, thickness t, and cross-sectional area $A = L \times t$ shown in Fig. 1.22 (a). The resistance of this sheet of meterial can be written as

$$R_s = \frac{\rho L}{L \times t} = \frac{\rho}{t} \text{ (ohms per square)}$$

This quantity R_s is independent of the size of the square and mainly depends upon the diffusion characteristic of the material. Now consider Fig. 1.22 (b, c) which shows a base resistor and the emitter resistor. The resistance for these resistors can be expressed in terms of the sheet resistance R_s and the surface dimensions L and W.

Now $$R = \rho \frac{L}{W \times t}$$

or, $$R = R_s \frac{L}{W}$$

where the ratio L/W is called the aspect ratio of the surface geometry and is, therefore, the effective number of square contained in the resistor. The base resistor in the range of 20 Ω to 300 kΩ can be easily fabricated due to medium resistivity (200 Ω/square) p-type base region. However, the sheet resistance of the emitter diffusion is of the order of 5 Ω/sq. only. So emitter resistors are usually in the range of 10 to 1 kΩ.

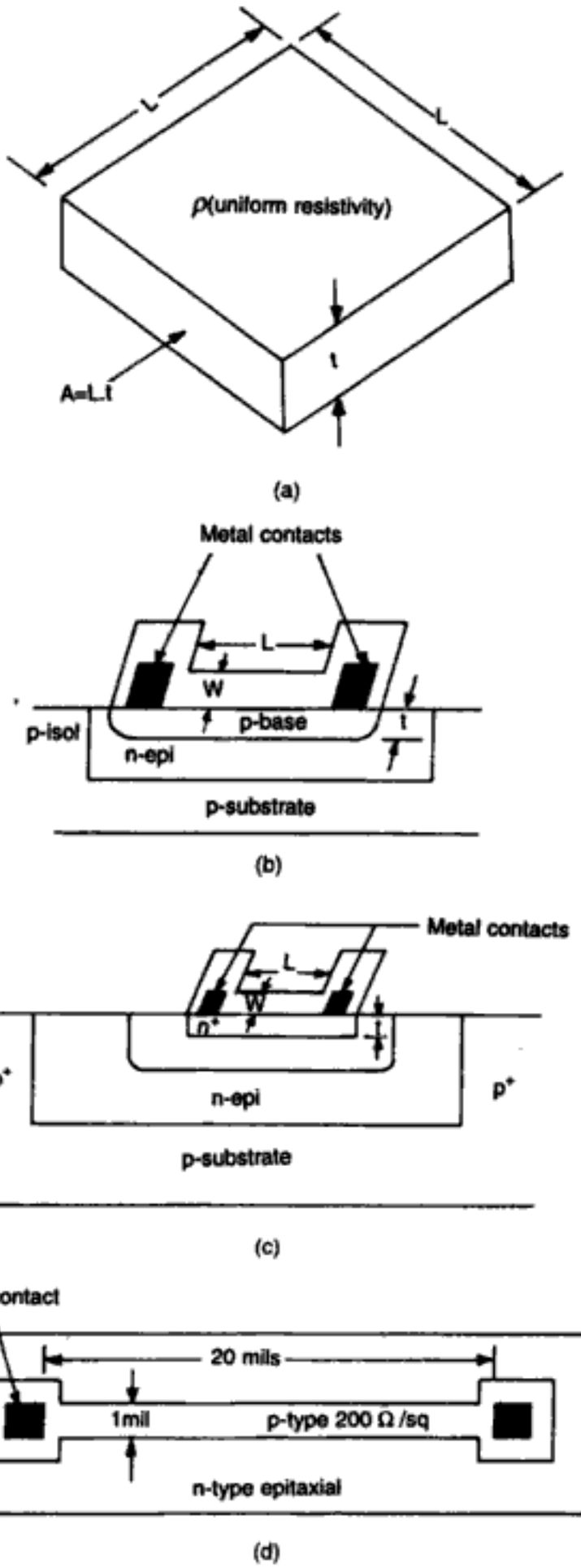


Fig. 1.22 (a) Sheet resistance (b) Base resistor (c) Emitter resistor (d) Top view showing dimensions for a 4000 Ω diffused resistor

Example

Design a 4 kΩ diffused resistor.

The sheet resistance of p-type diffusion is 200 ohm/sq.

Then $$\frac{L}{W} = \frac{R}{R_s} = \frac{4 \times 10^3}{200} = \frac{20}{1}$$

So a 4 kΩ resistor can be fabricated by using a pattern of 20 mils long by 1 mil wide as shown by the top view in Fig. 1.22 (d).

Epitaxial Resistor

Large value of resistance than possible by base or emitter resistor can be achieved by using n-epitaxial collector region as shown in Fig. 1.23 (a). Sheet resistance of epitaxial layer in the order of 1 to 10 kΩ/ square can be obtained.

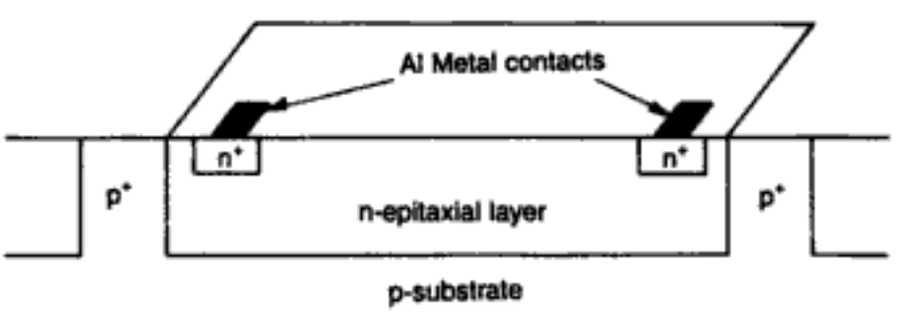


Fig. 1.23 (a) Epitaxial resistor

Pinched Resistor

The sheet resistivity of a semiconductor region can be increased by reducing its effective cross-sectional area. In a pinched resistor, this technique is used to achieve a high value of sheet resistance from the ordinary base diffused resistor.

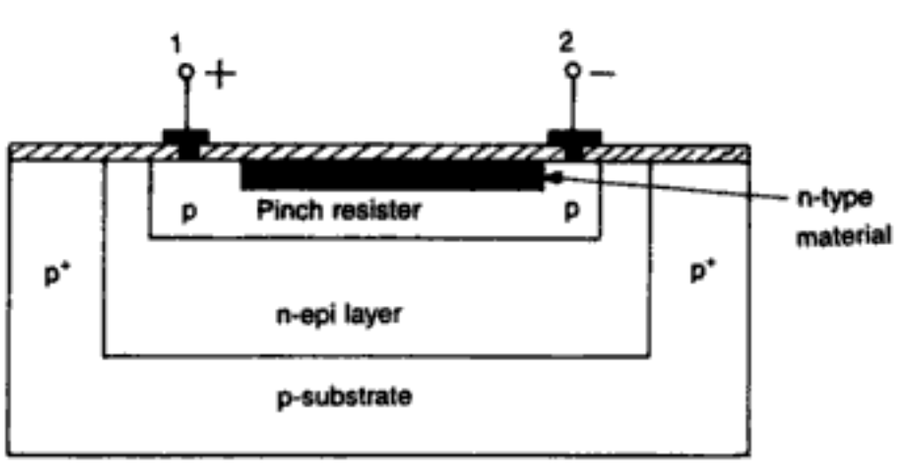


Fig. 1.23 (b) Cross-sectional view of a pinch resistor

A pinched base diffused resistor is shown in Fig. 1.23 (b). It can give resistances of the order of mega-ohm in a reasonably small area. In this structure, no current can flow through the *n*-type material (dark region) due to the diode at contact 2 in the reverse direction. Only a small reverse saturation current can flow through *n*-material. So, by creating this *n*-type region the effective cross-sectional area for the conduction path has been reduced and thus resistance between 1 and 2 increases.

Thin Film Resistor

Vapour thin film deposition techniques as discussed in Sec. 1.5.8 can also be used for the fabrication of IC resistors. In this, a very thin metallic film usually of Nichrome (NiCr) of thickness less than 1 μm is vapour deposited on the SiO_2 layer. Using masked etching, desired geometry of this thin film is achieved to obtain suitable values of resistors. The ohmic contacts are made using Al metallization and usual masked etching techniques. Nichrome resistors are available with typical sheet resistance values of 40 to 400 Ω/square depending upon film thickness, so that resistance in the range of 20 to 50 kΩ can be easily obtained. Figure 1.23 (c) shows the cross-sectional view of such a resistor. These thin film resistors have three distinct advantages over the diffused resistors.

1. Thin film resistors have lesser and smaller parasitic components and hence their high frequency behaviour is better.
2. The values of thin-film resistors can be easily adjusted even after fabrication by cutting a part of the resistor with a laser beam (Laser trimming).
3. Thin film resistors have low temperature coefficient, thereby making them more stable.

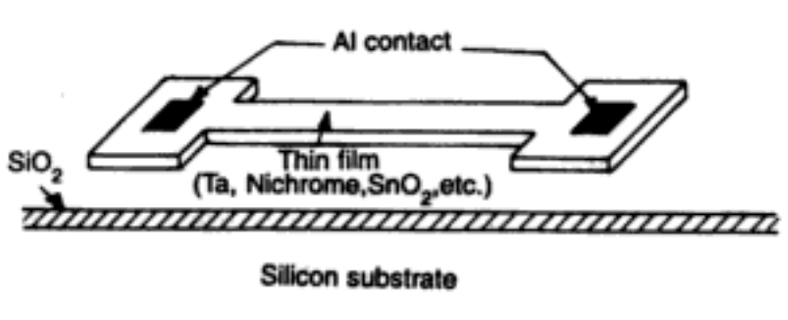


Fig. 1.23 (c) Cross-section of a thin film resistor

Higher values of thin film resistors have been obtained by depositing Tantalum over SiO_2 layer. The main disadvantage of thin film resistors is the additional process steps required in their fabrication.

1.7.4 Integrated Capacitors

Two commonly used methods for obtaining integrated capacitors are as follows:

(1) Junction capacitor
(2) MOS and thin film capacitor

Junction Capacitor

It is possible to use the junction capacitance of a reverse biased diode as an element in monolithic ICs. Figure 1.24 shows the cross-sectional view of a junction monolithic capacitor and its equivalent circuit. It can be seen that there are two junctions in this type of diffused capacitor. Junction J_2, if reverse biased, will produce the desired capacitance. However, a parasitic capacitance C_1 is inevitable due to the junction J_1 between n-type epitaxial layer and the substrate. Also a series resistance results due to the bulk resistance of the n-region. In the equivalent circuit, two diodes are the idealized diodes of the two junctions. The substrate must be held at the most negative point in the circuit, to minimize C_1. The value of the capacitance C_2 will depend upon the area of the junction, impurity concentration of the n-type epitaxial layer and the voltage across the junction. It can be seen that the capacitor C_2 is polarised and is obtained only when the junction J_2 is reverse biased.

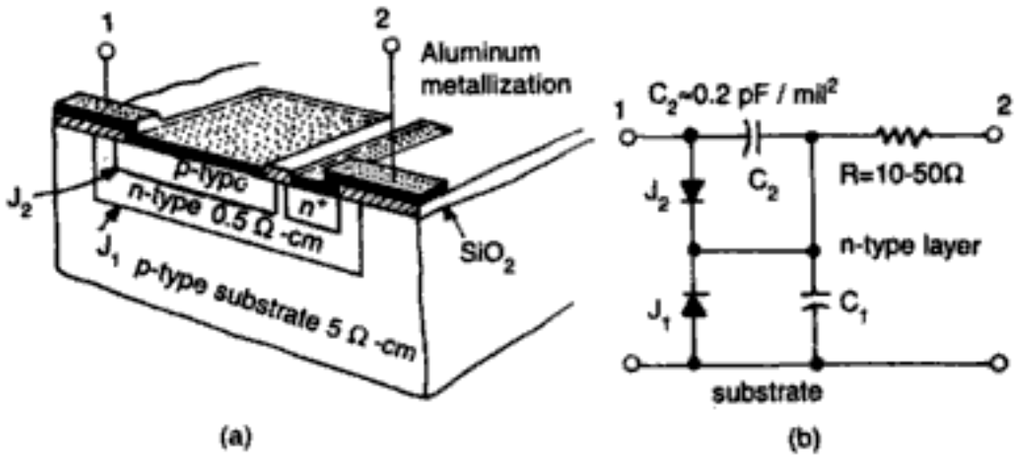


Fig. 1.24 (a) Junction-type IC capacitor, (b) Equivalent circuit

MOS and Thin Film Capacitor

A commonly used capacitor is the metal-oxide semiconductor capacitor for which the cross-sectional view and equivalent circuit is shown in Fig. 1.25. It is basically a parallel plate capacitor with SiO_2 as the dielectric. The heavily doped n^+ region formed during the emitter diffusion forms the lower plate and the thin film of aluminium metallization forms the upper plate of the capacitor with SiO_2 as the

dielectric. As shown in the equivalent circuit, the parasitic effects consist of a small series resistance R due to n^+ region, a collector substrate junction J_1, and its associated capacitance C_1.

This type of capacitor has the advantage of being nonpolar, that is, it does not matter which of the plates is positive or negative. Nor it is a function of the voltage applied, thus giving more circuit flexibility Silicon Nitride (Si_3N_4) can also be used as dielectric layer. Silicon Nitride offers a higher value of capacitance because of higher dielectric constant value, but requires extra processing steps.

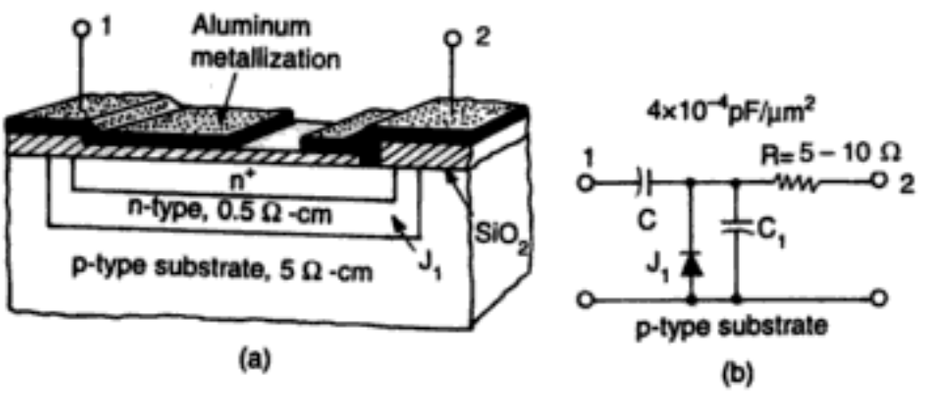


Fig. 1.25 (a) Structure and (b) equivalent circuit of a MOS capacitor

Thin film capacitor structures which use thin dielectric film layer between two metal layers are also in use. Although such a capacitor structure is almost free from substrate parasitics, it requires a number of additional masking and deposition steps beyond the basic MOS structure. In such a structure, either aluminium or tantalum is used as capacitor plates and aluminium oxide (Al_2O_3) or tantalum oxide (Ta_2O_5) as the dielectric material. Ta_2O_5 is particularly preferred for large value capacitors. One basic serious disadvantage of thin film capacitor is that they fail when the voltage rating exceeds due to breakdown of the dielectric. This is a destructive and irreversible failure mechanism and may require over-voltage protection.

1.7.5 Integrated Inductors

Inductors, transformers and chokes are the missing link in the chain of IC components. IC devices are essentially two dimensional as the depth dimension is usually very small (~ 1 to 10 μm) compared to the lateral dimensions. IC inductors can be made in the form of a flat metallic thin film spirals by successive deposition of conduction patterns. Very small values of inductance of the order of nano-henry with low quality factor can be only obtained. For any reasonable inductance value, a three dimensional coil structure is needed to obtain a large number of turns.

Most circuit designers go to great lengths to avoid the use of inductors or otherwise simulate them by using RC active networks. In

applications such as RF and IF circuits, where inductors cannot be avoided, inductors external to the IC-package are used. However, in thin-film hybrid microwave integrated circuit (MIC), thin film inductor spirals are used giving upto 250 nH.

1.8 FABRICATION OF FET

Unipolar monolithic ICs use JFET or MOSFET as an active device. The fabrication technique of JFET, MOSFET and CMOS is discussed.

1.8.1 JFET Fabrication

The structure of an n-channel JFET is shown in Fig. 1.26. The basic processes used are the same as in BJT fabrication. The epitaxial layer which formed the collector of the BJT is used as the n-channel of the JFET. The p^+ gate is formed in the n-channel by the process of diffusion or ion-implantation. The n^+ regions have been formed under the drain and source contact regions to provide good ohmic contact.

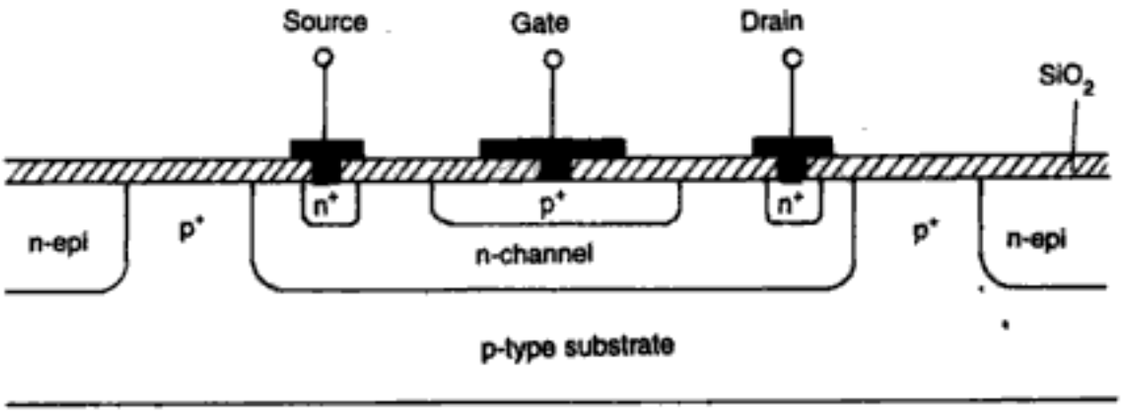


Fig. 1.26 n-channel JFET structure

1.8.2 MOSFET Fabrication

Two types of MOSFET devices are available, such as, enhancement type and depletion type. The cross-sectional view of n-channel aluminium gate enhancement MOSFET is shown in Fig. 1.27. In this structure, the metallic gate G is separated from the semiconductor channel by the insulating SiO_2 layer. The insulating layer of silicon dioxide gives an extremely high input resistance (10^{10} to 10^{15} Ω) for the MOSFET.

The value of V_T, the threshold voltage for MOSFET fabricated by this technique is typically 3 to 6V and power supply voltage of 12V is used for the drain supply. This large voltage is not compatible with the 5V supply used in digital ICs. A number of techniques have been developed to lower the magnitude of V_T which leads to improved device performance.

Use of Silicon Nitride (Si_3N_4)

It has been found that Si_3N_4 has superior masking properties compared to SiO_2. The Si_3N_4 is sandwiched between two SiO_2 layers and provides the necessary barrier to prevent impurities penetrating through the SiO_2 layer. The dielectric constant of Si_3N_4 is 7.5 whereas that of SiO_2 is 4. This increased overall dielectric constant reduces V_T.

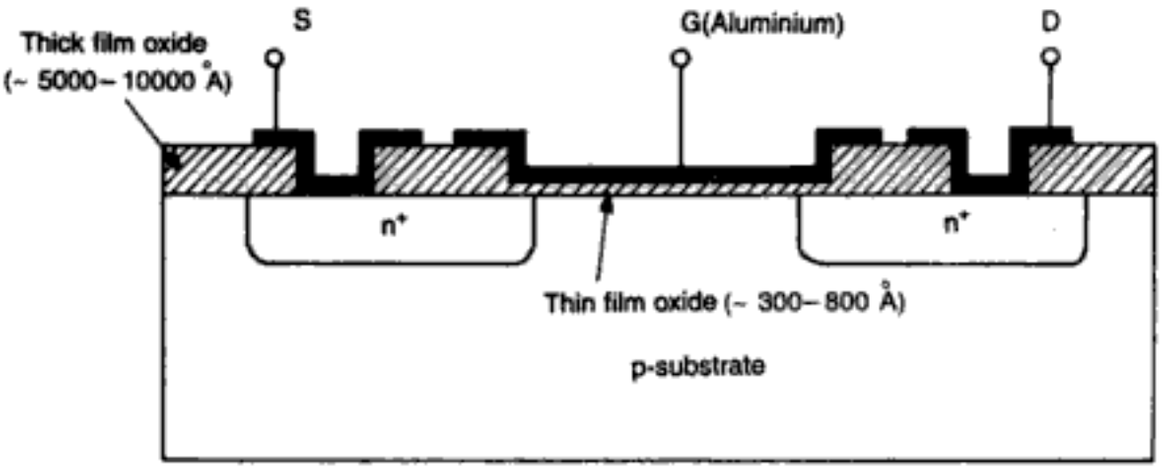


Fig. 1.27 n-channel MOSFET

Polysilicon Gate

Polycrystalline silicon when doped with phosphorus is conductive and is used as the gate electrode instead of aluminium. This reduces V_T to about 1 to 2V. Such devices are called silicon gate MOS transistors. The fabrication of NMOS enhancement device using these improved techniques is shown in Fig. 1.28.

The Si_3N_4 is first coated on the entire surface of a p-type wafer. With the help of a mask, sufficient area is defined to include the source, gate and drain. The Si_3N_4 is next etched away from the surface outside the transistor region. Now p^+ impurities are ion-implanted in the exposed p-substrate. These p^+ regions serve to isolate the various devices. Next a thick SiO_2 layer called field oxide is grown over the p^+ regions. The Si_3N_4 region, however, remains unaffected by the oxidation. The structure now is as shown in Fig. 1.28 (a).

The Si_3N_4 is now removed by selective etching and then SiO_2 layer (800 to 1000Å) is thermally grown over the transistor area as shown in Fig. 1.28 (b).

Polycrystalline silicon commonly known as polysilicon is now deposited over the entire wafer. The polysilicon gate is now formed by selective removal of polysilicon as shown in Fig. 1.28 (c).

The n^+ source and drain regions are formed by ion implantation. The field oxide and the polysilicon gate prevent the penetration of dopants below these regions. The thin oxide layer, however, allows the penetration of dopants and thus drain and source regions are formed.

After this, the entire wafer is covered with a protective isolating layer usually of SiO_2. The contact areas (including the body) are next defined using photolithographic process. Finally aluminium is evaporated over the entire wafer and another mark is used to pattern the circuit connections. The final cross-section is shown in Fig. 1.28 (d).

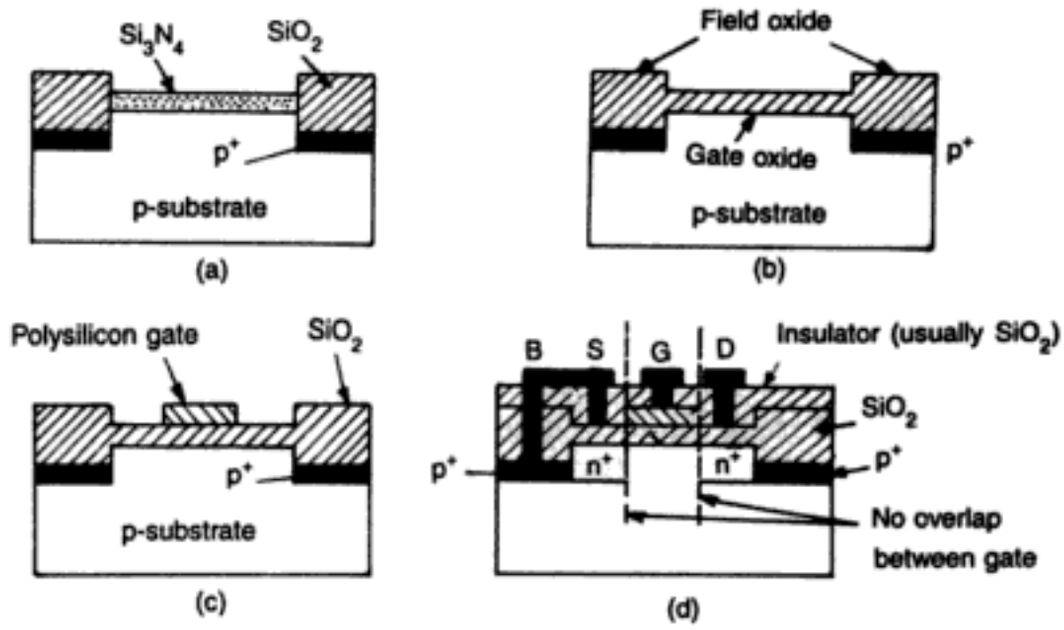


Fig. 1.28 Fabrication of polysilicon gate enhancement NMOS (a) Thick oxide growth and p^+ implantation, (b) Selective etching of Si_3N_4 and thin oxide growth, (c) Deposition of polysilicon gate, (d) Final cross-sectional view showing metallization and interconnection between substrate and source

There are two important points to be noticed in this structure.

1. The polysilicon-gate provides self alignment of the gate with the source and drain. In a conventional metal gate structure of Fig. 1.27, the gate electrode is normally designed to overlap the edges of the source and drain region by about 5 μm to avoid any masking errors. This, however, results in small overlap capacitance C_{gs} between gate G and source S and C_{gd} between gate G and drain D. These capacitances are of the order of 1 to 3 pF and lower the speed of operation and increase the power consumption. The silicon gate due to self aligning property eliminates these capacitances.
2. Another advantage of this structure is that no isolation island is required. This is because drain terminal in an NMOS device is held positive with respect to the source which is tied to the substrate. This cuts off the drain to substrate diode and the source to substrate diode formed due to p^+ region and the current flows only along the channel between D and S. In BJT the isolation diffusion occupies an extremely large percentage of chip area. With MOSFET, it is possible to get a packaging density twenty times more than that of BJT IC.

1.8.3 Complementary MOSFET (CMOS) Fabrication

It is possible to fabricate NMOS and PMOS enhancement devices on the same silicon chip. These devices are called complementary MOSFETs (abbreviated as CMOS, COS/MOS). The CMOS circuit of Fig. 1.29 (a) when implemented with polysilicon gate FETs has the cross-sectional view as shown in Fig. 1.29 (b). An n-type 'well' or 'tub' is diffused in the p-type substrate. The PMOS transistor (Q_2) is fabricated within this well. The n-type region forms the substrate or body B_2 for the the PMOS transistor. There are two additional steps required in the fabrication of PMOS transistor (Q_2) compared to NMOS transistor (Q_1), such as, the formation of n-region and ion implantation of p-type source and drain regions. The rest of the processes are the same as discussed for NMOS fabrication.

It can be seen that B_1 is tied to S_1 and is connected to the lowest voltage (GND) whereas B_2 is tied to S_2 and held at supply voltage V_{DD}. Since B_1 is p-type and B_2 is n-type, both the source substrate diodes (B_1-S_1 and B_2-S_2) are reverse biased and thus cut off. Thus isolation between NMOS and PMOS transistor is automatically achieved.

The circuit of Fig. 1.29 (a) is a CMOS inverter where G_1 is tied to G_2 and D_1 is connected to D_2. However, we have not shown these connections in the cross-sectional view of Fig. 1.29 (b).

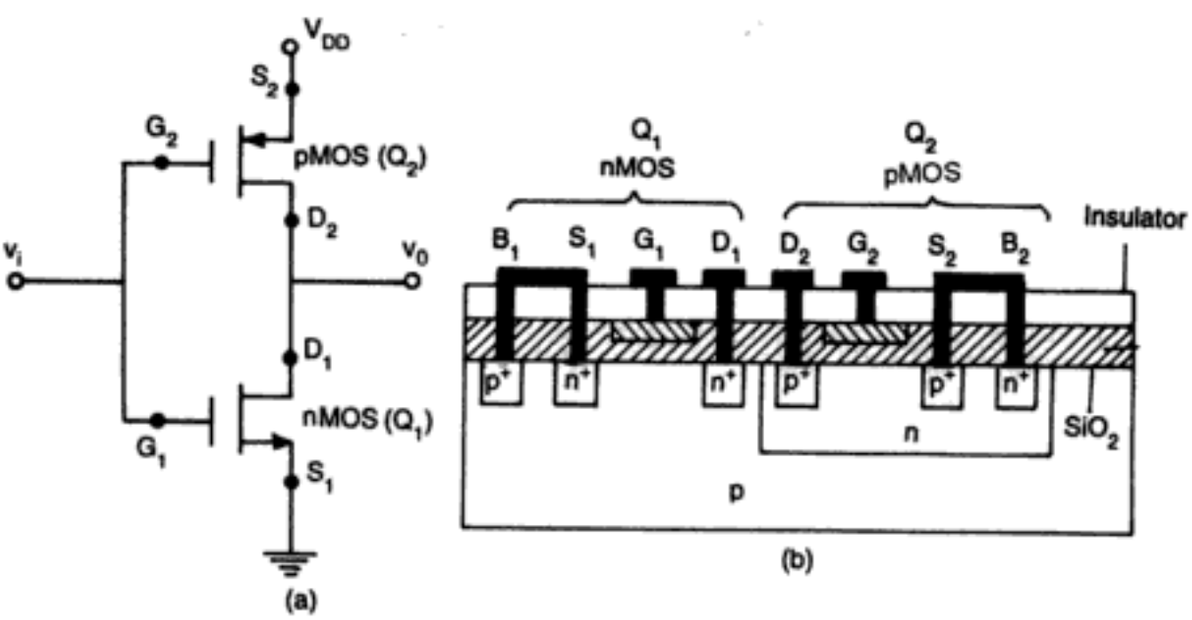


Fig. 1.29 (a) CMOS inverter, (b) Cross-section of CMOS IC

1.9 THIN AND THICK FILM TECHNOLOGY

Film ICs are classified as thick film and thin film circuits. Film technology at present can produce only passive components. The use of the term 'Thin Film' has been made in this chapter often, wherever

isolation or interconnections have to be made in integrated circuits. Thin film elements like resistors and capacitors have been discussed earlier also.

Conventional film circuits, both thick and thin, are made by depositing film capacitors and resistors on a passive substrate such as glass or ceramic and subsequently adding pre-fabricated active components to the film structure. Care has to be taken that the film elements and their interconnections are compatible with the rest of the integrated circuit.

Combining films and semiconductor technology, a circuit designer has greater degree of freedom, a wider range of component values and better electrical performance than either technology can provide separately.

Thin films are defined as the ones with thickness varying from 50 Å to 20,000 Å, whereas thick-films vary from 125000 Å (0.5 mil) to 625,000 Å (2.5 mils). However, a more fundamental difference between thin film and thick film is not the ultimate thickness, but the technology or the processes used for forming the film. Thick film ICs are made by the process of screen printing, usually silk screening techniques, whereas, the materials used to make thin film are generally deposited on to substrates in a vacuum chamber. Nevertheless, thick film technology produces cheap and rugged resistors, capacitors and conducting patterns. The processing equipment for thick film circuits is relatively inexpensive and easy to use. Thin film technology provides greater precision in manufacturing but is more costly than thick film technology.

1.9.1 Deposition of Thin Film

Various methods in use for deposition of thin film are:

1. Vacuum Evaporation
2. Sputtering
3. Gas plating
4. Electroplating
5. Electroless plating
6. Silk screening

The methods listed above have been used with varying degree of success. In this text however, we limit ourselves to discuss cathode sputtering and plating techniques only.

Vacuum Evaporation

The system used for depositing film using this method has been already discussed in sec. 1.5.8 where the technique has been used for depositing thin aluminium film for taking out contacts from the IC.

Cathode Sputtering

The system used for cathode sputtering is almost identical to that used for vacuum evaporation. The process however is much slower than evaporation, depositing a micron-thick film in minutes to hours, compared to seconds to minutes for evaporation. However, sputtering is superior to vacuum evaporation in the quality of the film produced but sputtering equipment is more costly than most evaporation systems. The process of cathode sputtering is performed at a low pressure (about 10^{-12} torr). The source material (material to be sputtered) is subjected to intense bombardment by the ions of a heavy inert gas such as argon. These gas ions are usually accelerated by making the source material as the cathode of a dc glow discharge. As atoms are ejected from the surface of the cathode, they diffuse away from it through a low pressure gas, depositing as a thin film on a nearby substrate. This sounds crude, but the high energy of the particles landing on the substrate actually results in a very uniform film with good crystal structure and adhesion. The principal parts of a sputtering system are shown in the Fig. 1.30. A potential typically 2 to 5 kV, is applied between the cathode (Source material) and anode, and produces a glow discharge that fills the entire interelectrode space, except for a thin region close to the cathode.

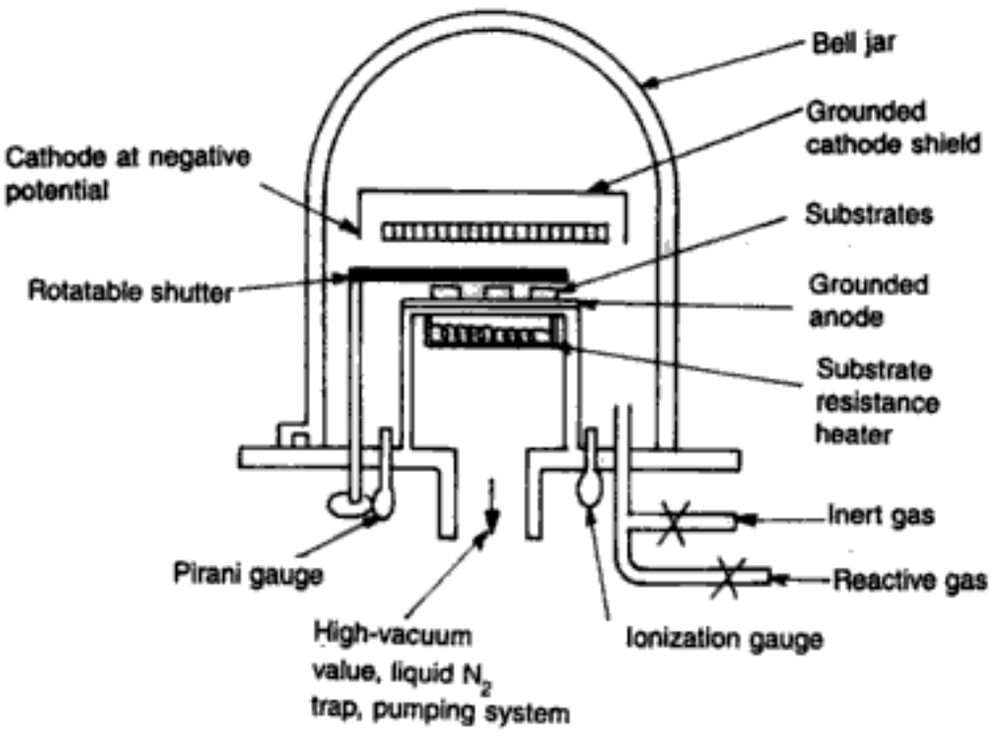


Fig. 1.30 The principal parts of sputtering system

Plating Technique

The two types of plating technique used are (i) Electroplating (ii) Electroless plating.

Electroplating uses for typical process of coating an object with one or more layers of different metals. Cathode and anode, in this case substrate and metal, are immersed in an electrolytic solution. When dc is passed through the solution, the positive metal ions migrate from the anode and deposit on the cathode. This method is suitable for making conduction films of gold or copper.

In electroless deposition of thin films, a metal ion in solution is reduced to the free metal and deposited as a metallic coating without the use of an electric current. This process can be used to deposit metals on any substrate such as glass, ceramic, plastic, etc., and films to considerable thickness can be deposited.

1.9.2 Thick Film Technology

The basic thick film process are:

(i) Screen printing,
(ii) Ceramic firing.

The process of screen printing patterns is an ancient one. The Egyptians used this technique thousands of years ago to decorate pottery and the walls of buildings and tombs. The same process is used today for production of thick film circuits, though considerably more complicated than simply forcing the ink through the screen as did the equipment used by the Egyptians. The screens used are woven from stainless steel wires to mesh size 320 and mounted on aluminium frame so as to keep the screen under uniform tension. The screen is next coated with a photo-sensitive emulsion which polymerizes on exposure to light. A mask (negative) of the desired pattern is made and kept on it. After exposure to light, it is developed. The screen becomes clear wherever thick film is to be deposited and blocked by the photoresist elsewhere. The screen is now placed on a substrate and carefully aligned components are deposited on the substrate through screening process. The screening process is carried out by a squeegee driven across the patterned screen at a constant rate. The squeegee forces an ink in the paste form through the openings on the screen. Different types of inks are used for depositing resistors conductors.

The desired physical and electrieal propertics from the thick films so deposited are now developed by thermal processing usually referred to as firing. It uses a furnace or kiln where temperature varies from 500°C to 1000°C in four to eight separately controlled zones. During the firing process, the organic binders of the thick film paste vaporizes and the remaining material fuses with the substrate, thereby, becoming a part of the ceramic structure. However, the structure and dimensions of most thick films are not compatible with monolithic circuits, therefore their use is limited to hybrid structures only.

1.9.3 Surface Mount Technology (SMT)

SMT is one of the advanced achievement in the area of semiconductor technology. This technology improves the product in terms of function, size and quality. It is difficult to automate production line with the use of conventional components. However, with surface mount devices, automation of manufacturing process as well as interconnection methodology can be achieved. The compact size of microcassette recorder, calculators, wrist watches and radios is the result of clever electronic component packing and assembly as a surface mount technology.

Surface mount technology utilizes micro-miniature leaded or leadless components called SMDs which are directly soldered to the specified areas on the PCB/surface without holes. The compact size of SMD components greatly reduce the area in a PCB, thus increasing packaging density. In this technology, both the components as well as conductive paths are installed on the same side of PCB, whereas, in conventional mounting technology, the components are mounted on one side and conductive paths are on the other side of PCB.

1.10. TECHNOLOGY TRENDS

The technology of semiconductor is advancing at a rapid rate. For high speed and low noise applications, bipolar technology is used. The heat dissipation in bipolar circuits is large and requires elaborate cooling arrangement. The MOS technology is becoming popular, because, high component density can be achieved. Originally, PMOS devices were used but now NMOS technology is predominant due to high-speed performance. The CMOS technology is now leading NMOS because of extremely low power consumption. The feature size of CMOS is also decreasing rapidly. In 1990s, the minimum feature size for CMOS was 0.5 micron (μm), which reduced to 0.12 μm in the year 2002 and it is predicted that 0.07 μm will be available for production by 2004.

The assembly of the chip is also improving drastically : 120 to 250-pin package are already available. It is predicted that 1000-pin package will be available. The electron-beam photolithographic techniques have been outdated and X-rays are in use exclusively. By 2003–04 new techniques EUV and Scalpel will also be used along with X-ray. The interconnections will also undergo change from aluminium to copper and optical interconnections may soon arrive.

The design styles and design tools are also undergoing rapid evolution. The design tools are sometimes referred to as computer-aided-design (CAD) tools and automatic testing is employed. The programs SPICE for circuit analysis and SUPREME for device

fabrication are the two widely used CAD tools. These tools are not used to design ICs but provide necessary information to evaluate a given design. No commercial IC is fabricated without such analysis.

Summary

1. An IC is a miniature, low cost electronic circuit fabricated on a single crystal chip of silicon.
2. An IC offers increased reliability, improved performance, high speed and lower power consumption.
3. ICs may be Linear or Digital.
4. Important IC technologies used are Monolithic technology and Hybrid technology.
5. The basic processes used in the silicon planar technology are (i) Substrate preparation (ii) Epitaxial Growth (iii) SiO_2 growth (iv) Photolithography (v) Diffusion (vi) Metallization
6. Order of magnitude for some important quantities:
   (i) Substrate thickness ~ 400–800 μm (16–32 mils)
   (ii) Epitaxial thickness ~ 5–20 μm
   (iii) Oxide thickness ~ 0.02–2 μm
   (iv) Al metallization ~ 1 μm
   (v) Base width (thickness) ~ 0.7 μm
   (vi) Diffusion time = about 2 hours
   (vii) Diffusion temperature = 1000°C
   (viii) Surface area for transistor ≃ 25 mils
   (ix) Wafer diameter = 10; 12.5; 15 cm
   (x) Chip size : 1 mm^2 (SSI); 16 mm^2 (MSI); 1 cm^2 (LSI)
   (xi) Concentration of acceptor atoms in the p-type substrate $N_A = 1.4 \times 10^{15}$ atoms/cm^3
   (xii) Concentration of acceptor atoms in isolation islands $N_A = 5 \times 10^{20}$/cm
   (xiii) Sheet resistance for
      (a) epitaxial collector region is 1 to 10 k Ω/sq.
      (b) *p*-type base region is 200 Ω/sq.
      (c) *n*-type emitter region is 5 Ω/sq.
7. The various components in an IC are provided electrical isolation by fabricating each component in an isolation island. Isolation techniques used are *pn* junction isolation and dielectric isolation.
8. ICs are available in three packages:
   (i) TO-5 glass metal package
   (ii) ceramic flat package
   (iii) Dual-in-line package

9. Buried layer is a heavily doped n^+ layer sandwiched between the p-type substrate and n-type epitaxial collector to reduce the collector series resistance of the IC transistor.
10. Aluminium used for making interconnections is a p-type impurity in silicon. The formation of a rectifying pn junction is avoided by making n^+ diffusions in the n-regions from where contact is to be made using aluminium. Such contacts are called ohmic.
11. The npn transistors are preferred over pnp transistors in ICs.
12. A Schottky barrier diode is clamped between base and collector of a transistor to avoid saturation.
13. It has not been possible to fabricate high-Q-inductors in monolithic ICs. Inductors have to be simulated by RC networks.
14. MOSFET occupies very small area and consumes less power. A polysilicon gate MOSFET has advantage over aluminium gate as (i) it lowers V_T, (ii) it reduces capacitances due to self-aligning property.
15. Thin and Thick film technology is used to make passive components like resistors and capacitors. Films with thickness greater than 0.5 mil are usually made by thick film technology.

Review Questions

1.1. List the advantages of integrated circuit over discrete component circuit.
1.2. Classify ICs on the basic of application, device used and chip complexity.
1.3. Name the technology used for the fabrication of transistors or ICs.
1.4. List the basic processes used in the silicon planar technology.
1.5. Explain how silicon wafers are prepared.
1.6. Explain the word "Epitaxy".
1.7. Describe the Epitaxial growth process.
1.8. Explain the importance of SiO_2 layer. How thick is this layer?
1.9. Explain briefly the photolithography process.
1.10. Describe the diffusion process.
1.11. What is ion implantation? Give its advantages.
1.12. Explain the need for making isolation islands.
1.13. Explain the various isolation techniques used in ICs.
1.14. To what voltage is the substrate connected and why?
1.15. Name the different types of IC packages.
1.16. Draw the cross-section of a discrete transistor and an IC transistor and hence compare their performance.
1.17. What is meant by parasitic capacitance?
1.18. Discuss the various ways for fabricating pnp transistor.

1.19. Compare the performance of *pnp* and *npn* transistor.
1.20. Explain why "buried layer" is used.
1.21. Show the cross-sectional structure of a multi-emitter transistor.
1.22. What is a Schottky transistor? Draw the cross-sectional view and explain its operation.
1.23. Give the various ways for making diodes in ICs.
1.24. Explain the operation of a Schottky-barrier diode.
1.25. What is an ohmic contact?
1.26. Give the advantages of Schottky barrier diode over *pn* junction diode.
1.27. Discuss the various methods used for fabricating IC resistors and compare their performance.
1.28. Define sheet resistance R_s.
1.29. Sketch the cross-section of a junction capacitor and draw its equivalent circuit.
1.30. Sketch a MOS capacitor and explain the difference in junction capacitor and MOS capacitor.
1.31. What is a thin film capacitor?
1.32. Explain why inductors are difficult to fabricate in ICs.
1.33. Draw the cross-section of an *n*-channel MOSFET.
1.34. Discuss the various ways for reducing V_T of a MOSFET.
1.35. What is the effect of using a polysilicon gate?
1.36. Discuss the self aligning property of a polysilicon gate MOSFET.
1.37. Sketch the cross-section of a CMOS transistor.
1.38. Discuss the difference between thin films and thick films.
1.39. List the various methods used for depositing thin films.
1.40. Discuss cathode sputtering.
1.41. Describe thick film technology.

2

Operational Amplifier

2.1 INTRODUCTION

Linear integrated circuits are being used in a number of electronic applications such as in fields like audio and radio communication, medical electronics, instrumentation control, etc. An important linear IC is operational amplifier which will be discussed in this chapter.

The operational amplifier (commonly referred to as op-amp) is a multi-terminal device which internally is quite complex. Fortunately, for the ordinary user, it is not necessary to know about the op-amp's internal make-up. The manufacturers have done their job so well that op-amp's performance can be completely described by its terminal characteristics and those of external components that are connected to it. However, for the designer's interest, the electronics of op-amp is described where the various stages of op-amp are discussed. Then some of the FET op-amps are described. The dc and ac characteristics with compensating techniques and the various applications of op-amp are taken up later.

2.2 BASIC INFORMATION OF OP-AMP

Circuit Symbol

The circuit schematic of an op-amp is a triangle as shown in Fig. 2.1. It has two input terminals and one output terminal. The terminal

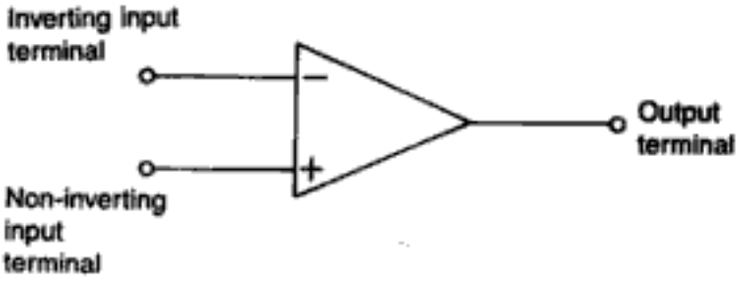


Fig. 2.1 Op-amp circuit symbol

with a (–) sign is called inverting input terminal and the terminal with (+) sign is called the non-inverting input terminal.

Packages

There are three popular packages available:

1. The metal can (TO) package
2. The dual-in-line package (DIP)
3. The flat package or flat pack

Op-amp packages may contain single, two (dual) or four (quad) op-amps. Typical packages have 8 terminals (the can and the DIP or MINI DIP), 10 terminals (flatpacks and some cans) and 14 terminals (the DIP and the flat pack). The widely used very popular type, for example μA741 is a single op-amp and is available as an 8-pin can, an 8-pin DIP, a 10-pin flatpack or a 14-pin DIP. The μA747 is a dual 741 and comes in either a 10-pin can or a 14-pin DIP. Figure 2.2 shows the various IC packages along with the top view of connection diagram.

OP-AMP Terminals

Op-amps have five basic terminals, that is, two input terminals, one output terminal and two power supply terminals. The significance of other terminals varies with the type of the op-amp.

Refer to the top view of a metal can package (μA741) in Fig. 2.2 (a). The metal can has eight pins with pin number 8 identified by a tab. The other pins are numbered counter-clockwise from pin 8, beginning with pin 1. Pin 2 is called the inverting input terminal and pin 3 is the non-inverting input terminal, pin 6 is the output terminal and pins 7 and 4 are the power supply terminals labelled as V^+ and V^- respectively. Terminals 1 and 5 are used for dc offset. The pin 8 marked NC indicates 'No Connection'. In case of DIP package of 741 as in Fig. 2.2 (b, c), the top pin on the left of the notch locates pin 1, and the flat pack of Fig. 2.2 (d) has a dot on it for identification. The other pins are numbered counter-clockwise from pin 1. The pin numbers have been illustrated only for some popular op-amps and the user should consult the manufacturer's data sheet before connecting a given op-amp into a circuit.

Power Supply Connections

The V^+ and V^- power supply terminals are connected to two dc voltage sources. The V^+ pin is connected to the positive terminal of one source and the V^- pin is connected to the negative terminal of the other source as illustrated in Fig. 2.3 (a) where the two sources are 15 V batteries each. These are typical values, but in general, the power supply voltage may range from about ± 5 V to ± 22 V. The common

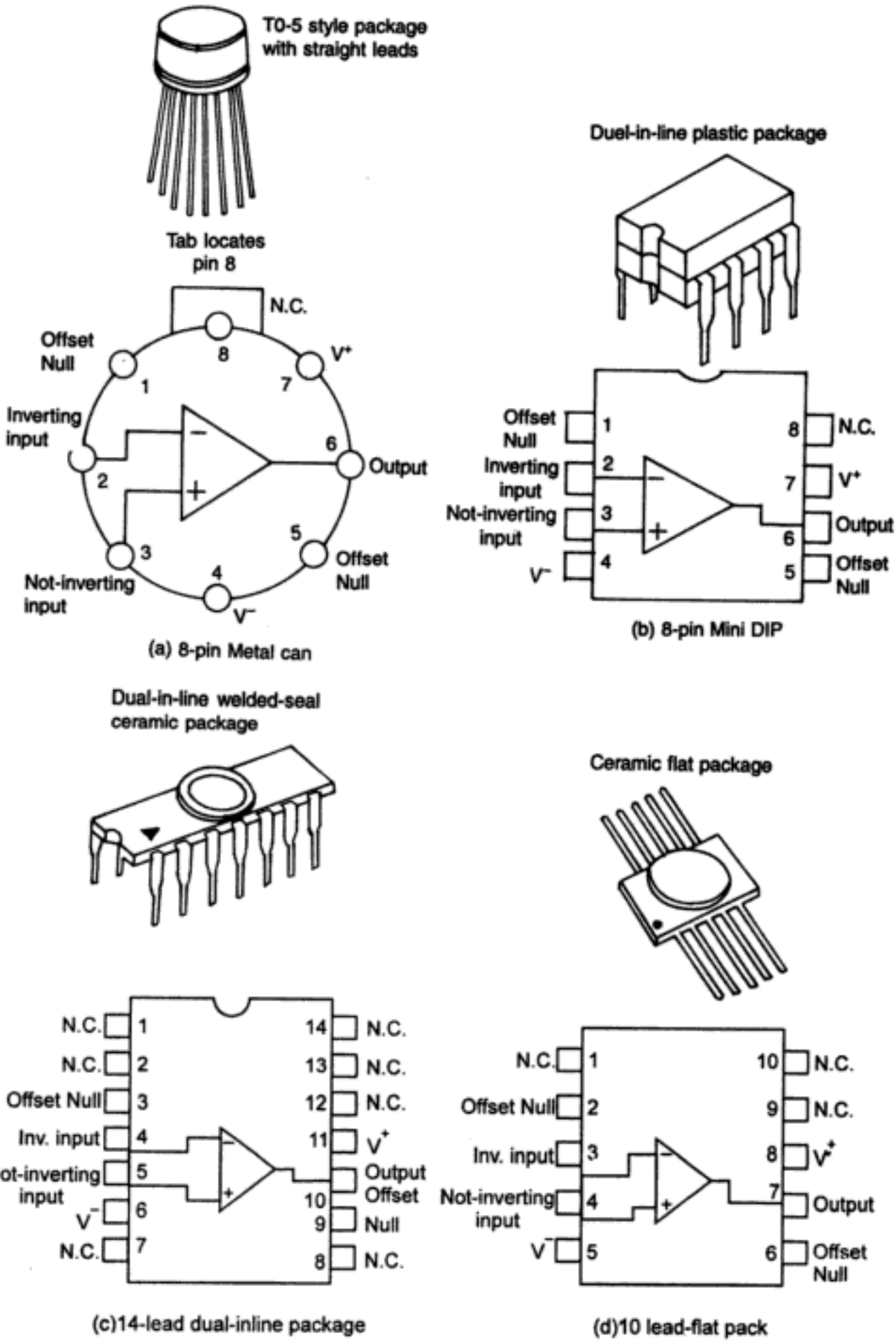


Fig. 2.2 (a, b, c, d) Various IC packages of $\mu A741$ op-amp along with connection diagrams (top view)

terminal of the V^+ and V^- sources is connected to a reference point or ground. Some op-amps have a ground terminal, but most do not. The ground is simply a convenient point on the circuit bread-board to which the op-amp is connected through the power supplies. The equivalent representation of Fig. 2.3 (a) is given in Fig. 2.3 (b). The common point of the two supplies must be grounded, otherwise twice the supply

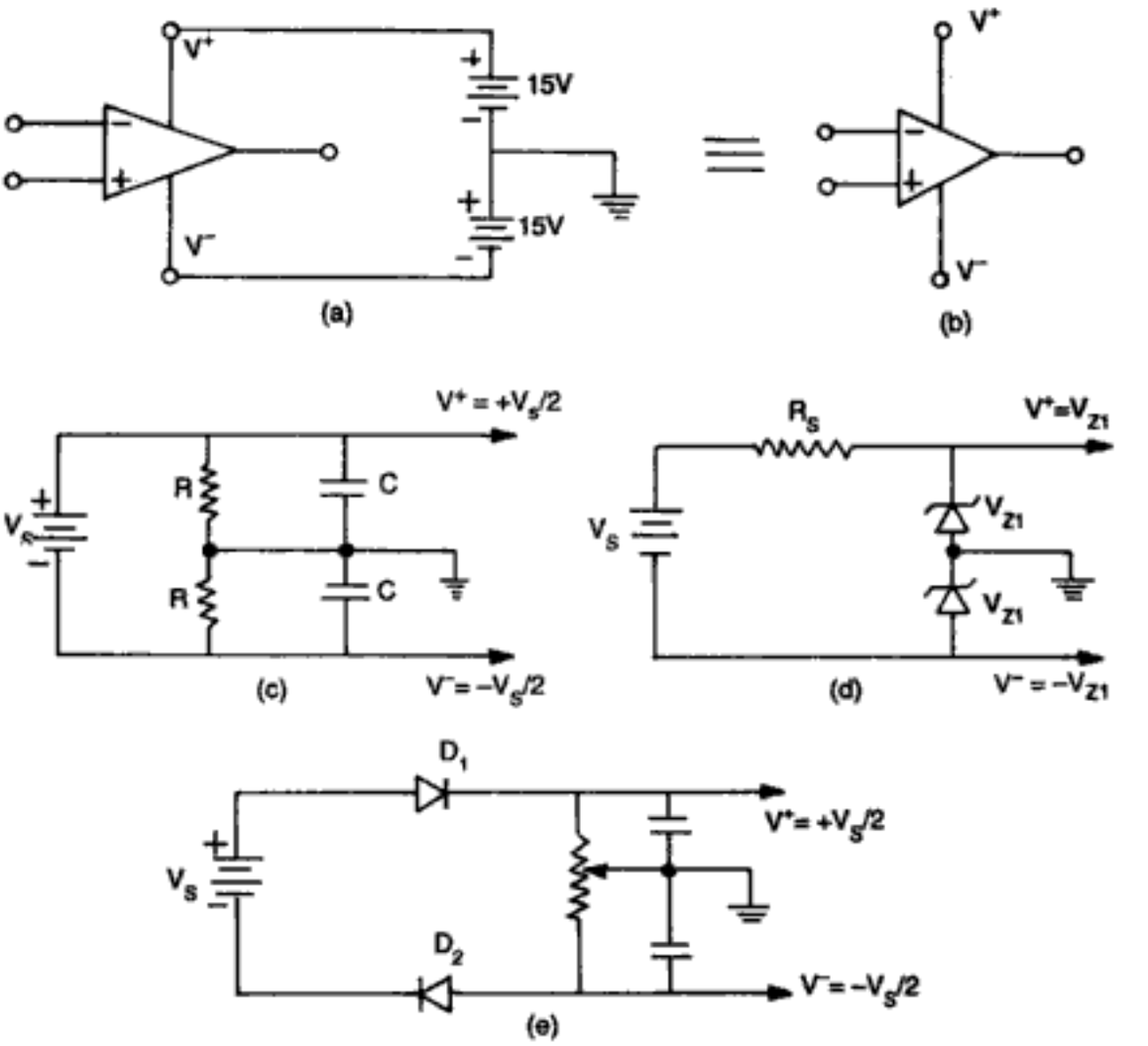


Fig. 2.3 (a) Power supply connections (b) Circuit symbol showing power supply terminals (c, d, e) Different circuits for obtaining positive and negative supply voltages for op-amp

voltage will get applied and it may damage the op-amp. Instead of using two power supplies, one can use a single power supply to obtain V^+ and V^- as shown in circuits of Fig. 2.3 (c, d, e). In Fig. 2.3 (c), resistor R should be greater than 10 kΩ so that it does not draw more current from the supply V_s. The two capacitors provide decoupling of the power supply and range in value from 0.01 to 10 μF. In the circuit of Fig. 2.3 (d), zener diodes are used to give symmetrical supply voltages. The value of the resistor R_s is chosen such that it supplies sufficient current for the zener diodes to operate in the avalanche mode. In Fig. 2.3 (e), potentiometer is used to get equal values of V^+ and V^-. Diodes D_1 and D_2 protect the IC if the positive and negative

leads of the supply voltage V_s are accidentally reversed. These diodes can also be connected in the circuits of Fig. 2.3 (c) and 2.3 (d).

Manufacturer's Designation for Linear ICs

Each manufacturer uses a specific code and assigns a specific type number to the ICs produced. For example, 741 an internally compensated op-amp originally manufactured by Fairchild is sold as μA741. Here μA represents the identifying initials used by Fairchild. The codes used by some of the well-known manufacturers of linear ICs are:

(1)	Fairchild	μA, μAF
(2)	National Semiconductor	LM, LH, LF, TBA
(3)	Motorola	MC, MFC
(4)	RCA	CA, CD
(5)	Texas Instruments	SN
(6)	Signetics	N/S, NE/SE
(7)	Burr-Brown	BB

A number of manufacturers also produce popular ICs of the other manufacturers. For easy use, they usually retain the original type number of the IC alongwith their identifying initials. For example, Fairchild's original μA741 is also manufactured by other manufacturers as follows:

(1)	National Semiconductor	LM741
(3)	Motorola	MC1741
(4)	RCA	CA3741
(5)	Texas Instruments	SN52741
(6)	Signetics	N5741

It may be noted that the last three digits in each manufacturer's designation are 741. All these op-amps have the same specifications. Since a number of manufacturers produce the same IC, one can refer to such ICs by their type number only and delete manufacturer's identifying initials. For example, μA741 or MC1741 may simple be referred as 741.

Some linear ICs are available in different classes such as A, C, E, S and SC. For example 741, 741 A, 741 C, 741 E, 741 S and 741 SC are different versions of the same op-amp. The main difference of these op-amps are:

741	Military grade op-amp (Operating temperature range –55° to 125°C)
741C	Commercial grade op-amp (Operating temperate range 0° to 70°/75°C)

741A	Improved version of 741	Better electrical specifications
741E	Improved version of 741 C	
741S	Military grade op-amp with higher slew-rate	
741SC	Commercial grade op-amp with higher slew-rate	

2.3 THE IDEAL OPERATIONAL AMPLIFIER

The schematic symbol of an op-amp is shown in Fig. 2.4 (a). It has two input terminals and one output terminal. Other terminals have not been shown for simplicity. The – and + symbols at the input refer to inverting and non-inverting input terminals respectively, i.e if $v_1 = 0$, output v_0 is 180° out of phase with input signal v_2. And, when $v_2 = 0$, output v_o will be in phase with the input signal applied at v_1. This op-amp is said to be ideal if it has the following characteristics.

Open loop voltage gain,	A_{OL}	=	∞
Input impedance,	R_i	=	∞
Output impedance	R_o	=	0
Bandwidth	BW	=	∞

Zero offset, i.e. $v_o = 0$ when $v_1 = v_2 = 0$.

It can be seen that

(i) an ideal op-amp draws no current at both the input terminals i.e., $i_1 = i_2 = 0$. Because of infinite input impedance, any signal source can drive it and there is no loading on the preceding driver stage.

(ii) Since gain is ∞, the voltage between the inverting and non-inverting terminals, i.e., differential input voltage $v_d = (v_1 - v_2)$ is essentially zero for finite output voltage v_o.

(iii) The output voltage v_o is independent of the current drawn from the output as $R_o = 0$. The output thus can drive an infinite number of other devices.

The above properties can never be realized in practice. However, the use of such an 'Ideal op-amp' model simplifies the mathematics involved in op-amp circuits. There are practical op-amps that can be made to approximate some of these characteristics.

A physical amplifier is not an ideal one. So, the equivalent circuit of an op-amp may be shown in Fig. 2.4 (b) where $A_{OL} \neq \infty$, $R_i \neq \infty$ and $R_o \neq 0$. It can be seen that op-amp is a voltage controlled voltage source and $A_{OL}\, v_d$ is an equivalent *Thevenin* voltage source and R_o is the *Thevenin* equivalent resistance looking back into the output terminal of an op-amp. The equivalent circuit is useful in analyzing the basic operating principles of op-amp. For the circuit shown in Fig. 2.4 (b), the output voltage is

$$\begin{aligned} v_o &= A_{OL}\, v_d \\ &= A_{OL}\, (v_1 - v_2) \end{aligned} \qquad (2.1)$$

The equation shows that the op-amp amplifies the difference between the two input voltages.

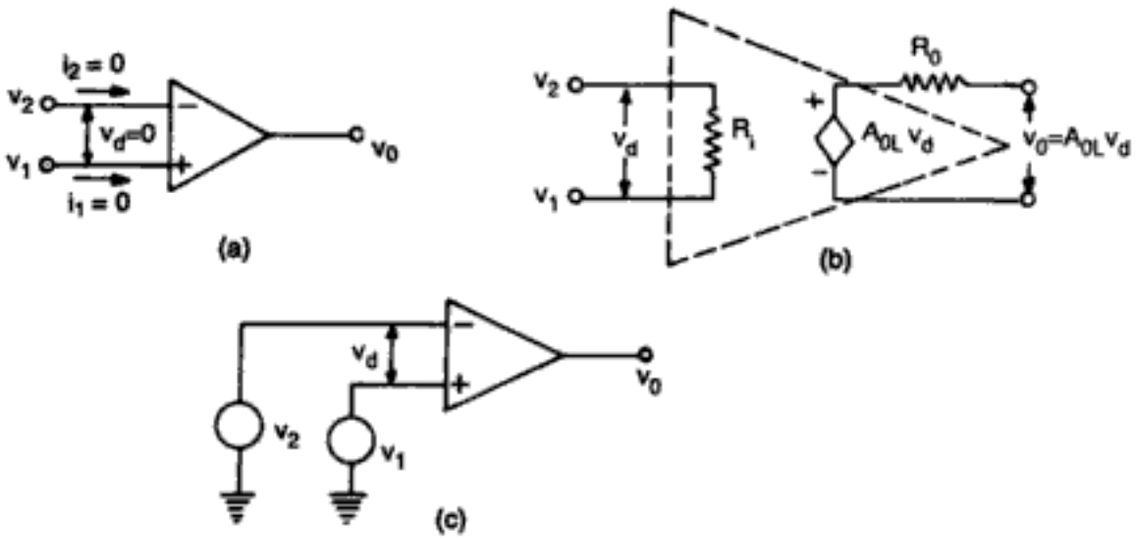


Fig. 2.4 (a) Ideal op-amp (b) Equivalent circuit of an op-amp (c) Open loop circuit

2.3.1 Open Loop Operation of Op-Amp

The simplest way to use an op-amp is in the open loop mode. Refer to Fig. 2.4 (c) where signals v_1 and v_2 are applied at non-inverting and inverting input terminals respectively. Since the gain is infinite, the output voltage v_o is either at its positive saturation voltage ($+ V_{sat}$) or negative saturation voltage ($-V_{sat}$) as $v_1 > v_2$ or $v_2 > v_1$ respectively. The output assumes one of the two possible output states, that is, $+V_{sat}$ or $-V_{sat}$ and the amplifier acts as a switch only. This has a limited number of applications such as voltage comparator, zero crossing detector etc. which are discussed later.

2.3.2 Feedback in Ideal Op-Amp

The utility of an op-amp can be greatly increased by providing negative feedback. The output in this case is not driven into saturation and the circuit behaves in a linear manner.

Two Important Negative Feedback Circuits

There are two basic feedback connections used. In order to understand the operation of these circuits, we make two realistic simplifying assumptions discussed earlier also.

1. The current drawn by either of the input terminals (non-inverting and inverting) is negligible.
2. The differential input voltage v_d between non-inverting and inverting input terminals is essentially zero.

2.3.3 The Inverting Amplifier

This is perhaps the most widely used of all the op-amp circuits. The circuit is shown in Fig. 2.5 (a). The output voltage v_o is fed back to the inverting input terminal through the $R_f - R_1$ network where R_f is the feedback resistor. Input signal v_i is applied to the inverting input terminal through R_1 and non-inverting input terminal of op-amp is grounded.

Analysis: For simplicity, assume an ideal op-amp. As $v_d = 0$, node 'a' is at ground potential and the current i_1 through R_1 is

$$i_1 = \frac{v_i}{R_1} \tag{2.2}$$

Also since op-amp draws no current, all the current flowing through R_1 must flow through R_f. The output voltage,

$$v_o = -i_1 R_f = -v_i \frac{R_f}{R_1} \tag{2.3}$$

Hence, the gain of the inverting amplifier (also referred as closed loop gain) is,

$$A_{CL} = \frac{v_o}{v_i} = -\frac{R_f}{R_1} \tag{2.4}$$

Alternatively, the nodal equation at the node 'a' in Fig. 2.5 (a) is

$$\frac{v_a - v_i}{R_1} + \frac{v_a - v_o}{R_f} = 0$$

where v_a is the voltage at node 'a'. Since node 'a' is at virtual ground $v_a = 0$. Therefore, we get,

$$A_{CL} = \frac{v_o}{v_i} = -\frac{R_f}{R_1}$$

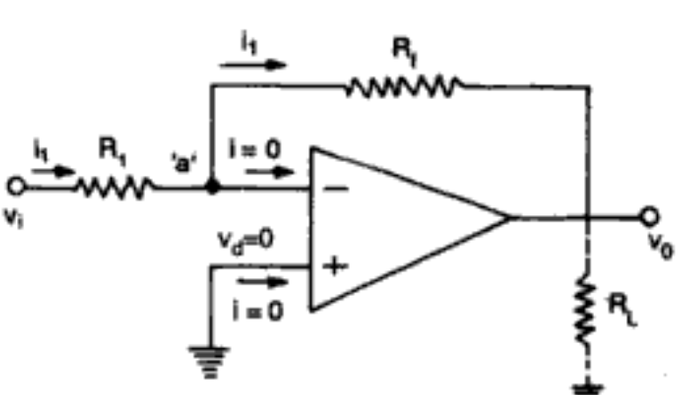


Fig. 2.5 (a) Inverting amplifier

The negative sign indicates a phase shift of 180° between v_i and v_o. Also since inverting input terminal is at virtual ground, the effective

input impedance is R_1. The value of R_1 should be kept fairly large to avoid loading effect. This however, limits the gain that can be obtained from this circuit. A load resistor R_L is usually put at the output in actual practice otherwise, the input impedance of the measuring device such as oscilloscope or DVM acts as the load. The calculation of load and output currents is shown in the Example 2.2.

If, however, resistances R_1 and R_f in Fig. 2.5 (a) are replaced by impedances Z_1 and Z_f respectively, then the voltage gain, A_{CL} will be

$$A_{CL} = -\frac{Z_f}{Z_i} \tag{2.5}$$

This expression for the voltage gain will be used in op-amp application, such as integrator, differentiator etc.

Example 2.1

Design an amplifier with a gain of –10 and input resistance equal to 10 kΩ.

Solution

Since the gain of the amplifier is negative, an inverting amplifier has to be made.

In Fig. 2.5 (a) choose $R_1 = 10\ \text{k}\Omega$

Then $R_f = -A_{CL}\, R_1$ (from Eq. 2.4)

$= -(-10) \times 10\ \text{k}\Omega = 100\ \text{k}\Omega$

Example 2.2

In Fig. 2.5 (b), $R_1 = 10\ \text{k}\Omega$, $R_f = 100\ \text{k}\Omega$, $v_i = 1\ V$. A load of 25 kΩ is connected to the output terminal. Calculate (i) i_1 (ii) v_o (iii) i_L and total current i_o into the output pin.

Solution

(a) $i_1 = \dfrac{v_i}{R_1} = \dfrac{1\,V}{10\ \text{k}\Omega} = 0.1\ \text{mA}$

(b) $v_o = -\dfrac{R_f}{R_1} v_i = -\dfrac{100\ \text{k}\Omega}{10\ \text{k}\Omega} 1\,V = -10V$

(c) $i_L = \dfrac{v_o}{R_L} = \dfrac{10\,V}{25\ \text{k}\Omega} = 0.4\ \text{mA}$

The direction of i_L is shown in Fig. 2.5 (b).

(d) i_1 as calculated above is 0.1 mA.
Therefore, total current $i_o = i_1 + i_L = 0.1\ \text{mA} + 0.4\ \text{mA} = 0.5\ \text{mA}$. In an inverting amplifier, for a + ive input, output will be –ive, therefore the direction of i_o is as shown in Fig. 2.5 (b).

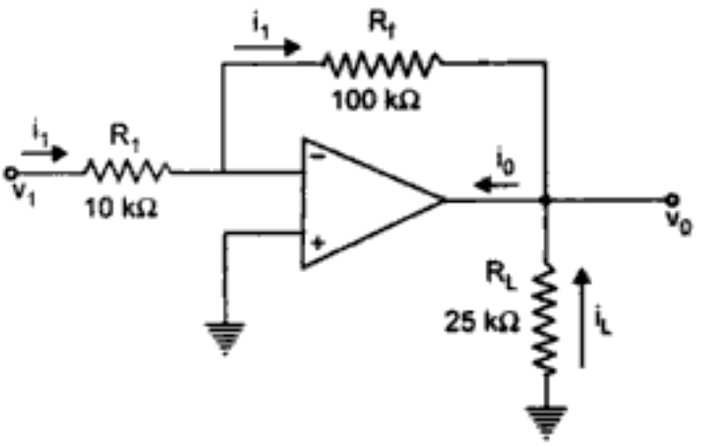


Fig. 2.5 (b) Circuit for Example 2.2

Practical Inverting Amplifier

Equation (2.4) is valid only if the op-amp is an ideal one. For a practical op-amp, the expression for the closed loop voltage gain should be calculated using the low frequency model of Fig. 2.4 (b). The equivalent circuit of a practical inverting amplifier is shown in Fig. 2.6 (a). This circuit can be simplified by replacing the signal source v_i and resistors R_1 and R_i by Thevenin's equivalent as shown in Fig. 2.6 (b) which is analysed to calculate the exact expression for closed loop gain, A_{CL} and input impedance R_{if}.

The input impedance R_i of an op-amp is usually much greater than R_1, so one may assume, $v_{eq} \cong v_i$ and $R_{eq} \cong R_1$.

From the output loop in Fig. 2.6 (b)

$$v_o = iR_o + A_{OL}\, v_d \tag{2.6}$$

Also
$$v_d + iR_f + v_o = 0 \tag{2.7}$$

Putting the value of v_d from Eq. (2.6) to Eq. (2.7) and simplifying,

$$v_o(1 + A_{OL}) = i(R_o - A_{OL}\, R_f) \tag{2.8}$$

Also the KVL loop equation gives

$$v_i = i(R_1 + R_f) + v_o \tag{2.9}$$

Putting the value of i from Eq. (2.8) in Eq. (2.9) and solving for closed loop gain $A_{CL} = \frac{v_o}{v_i}$, gives

$$A_{CL} = \frac{v_o}{v_i} = \frac{R_o - A_{OL}\, R_f}{R_o + R_f + R_1\,(1 + A_{OL})} \tag{2.10}$$

It can be seen from Eq. (2.10) that if $A_{OL} >> 1$ and $A_{OL} R_1 >> R_0 + R_f$,

$$A_{CL} \cong -\frac{R_f}{R_1}.$$

Input Resistance R_{if}

In Fig. 2.6 (b), it can be seen that

$$R_{if} = \frac{v_d}{i}$$

Writing the loop equation and solving for R_{if},

$$v_d + i\,(R_f + R_o) + A_{OL}\,v_d = 0$$

We obtain

$$R_{if} = \frac{R_f + R_o}{1 + A_{OL}} \tag{2.11}$$

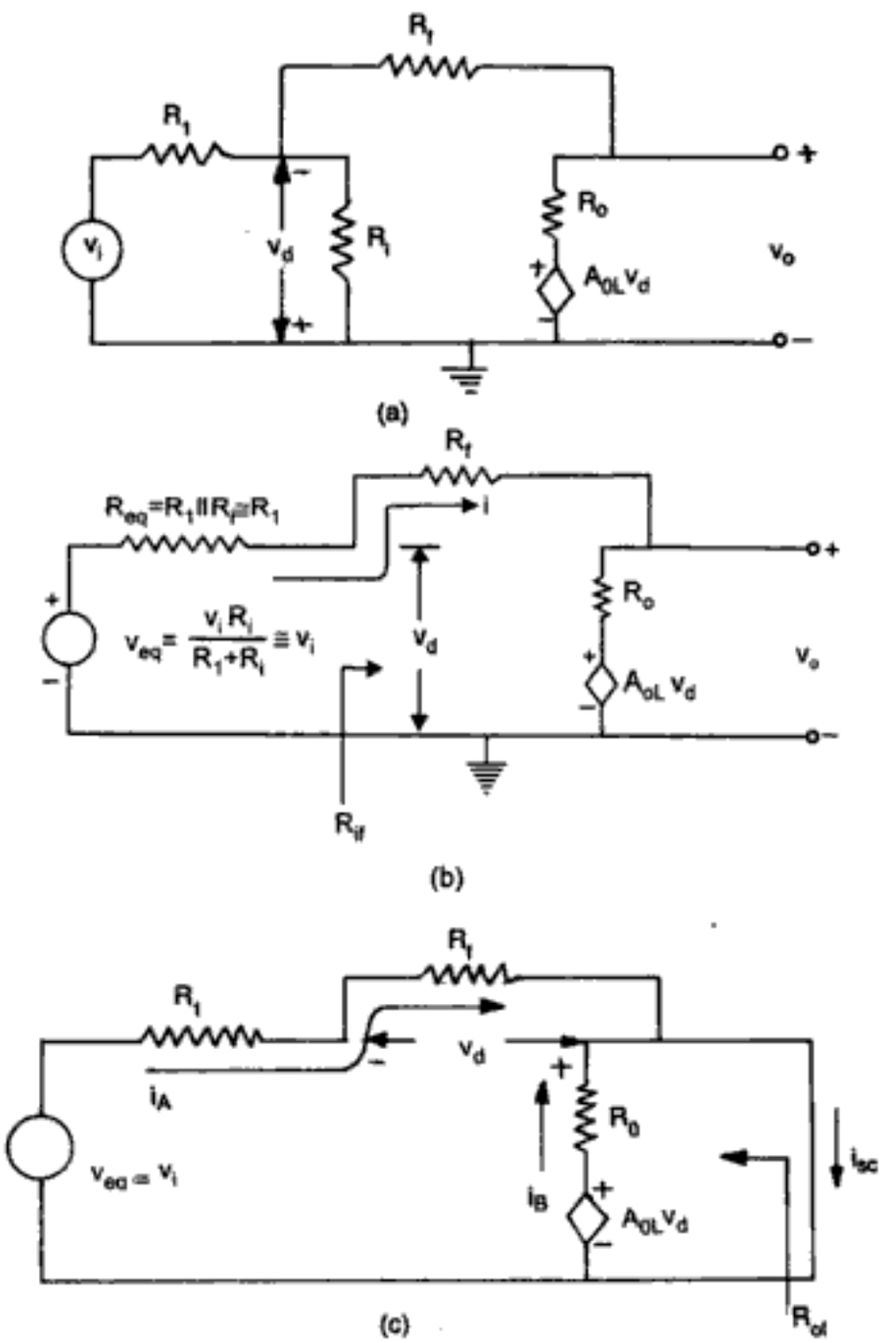


Fig. 2.6 (a) Equivalent circuit of a practical op-amp inverting amplifier (b) Simplified circuit by using Thevenin's equivalent (c) Equivalent circuit for computing R_{of}

Output Resistance R_{of}

Output impedance R_{of} (without load resistance R_L) is calculated from the open circuit output voltage v_{oc} and short circuit output circuit i_{sc}. Now consider the circuit shown in Fig. 2.6 (c). Under short circuit conditions at output,

$$i_A = \frac{v_i - 0}{R_1 + R_f} \tag{2.12}$$

and,
$$i_B = \frac{A_{OL}\, v_d}{R_o} \tag{2.13}$$

Since $v_d = -i_A R_f$

So, $$i_B = -\frac{A_{OL}\, i_A\, R_f}{R_o}$$

Solving for $i_{sc} = i_A + i_B$, we obtain

$$i_{sc} = i_A + i_B = v_i \frac{(R_o - A_{OL} R_f)}{R_o(R_1 + R_f)} \tag{2.14}$$

Since

$$R_{of} = \frac{v_{oc}}{i_{sc}}$$

and
$$A_{CL} = \frac{v_{oc}}{v_i}$$

Therefore,
$$R_{of} = \frac{A_{CL}\, v_i}{v_i \left[(R_o - A_{OL} R_f) \Big/ R_o(R_1 + R_f) \right]} \tag{2.15}$$

Putting the value of A_{CL} from Eq. (2.10), we obtain

$$R_{of} = \frac{R_o(R_1 + R_f)}{R_o + R_f + R_1(1 + A_{OL})} \tag{2.16}$$

Eq. (2.16) may alternatively be written as

$$R_{of} = \frac{\dfrac{R_o(R_1 + R_f)}{R_o + R_1 + R_f}}{1 + \dfrac{R_1 A_{OL}}{R_o + R_1 + R_f}} \tag{2.17}$$

It may be seen that numerator consists of a term $R_o \| (R_1 + R_f)$ and is therefore smaller than R_o. The output resistance R_{of} (with feedback) is, therefore always less than R_o and for $A_{CL} \to \infty$, $R_{of} \to 0$.

2.3.4 The Non-Inverting Amplifier

If the signal is applied to the non-inverting input terminal and feedback is given as shown in Fig. 2.7 (a), the circuit amplifies without inverting the input signal. Such a circuit is called non-inverting amplifier. It may be noted that it is also a negative feed-back system as output is being fed back to the inverting input terminal.

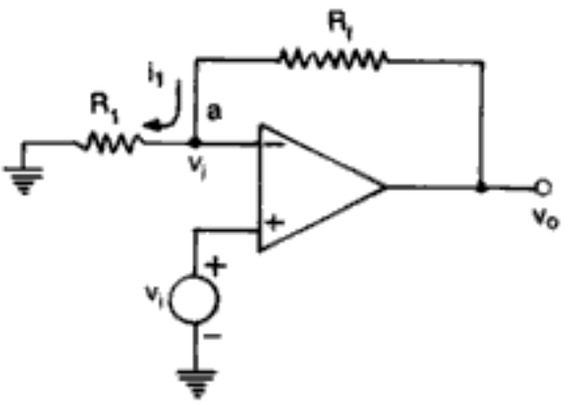


Fig. 2.7 (a) Non-inverting amplifier

As the differential voltage v_d at the input terminal of op-amp is zero, the voltage at node 'a' in Fig. 2.7 (a) is v_i, same as the input voltage applied to non-inverting input terminal. Now R_f and R_1 forms a potential divider. Hence

$$v_i = \frac{v_o}{R_1 + R_f} R_1 \tag{2.18}$$

as no current flows into the op-amp.

$$\frac{v_o}{v_i} = \frac{R_1 + R_f}{R_1} = 1 + \frac{R_f}{R_1} \tag{2.19}$$

Thus, for non-inverting amplifier the voltage gain,

$$A_{CL} = \frac{v_o}{v_i} = 1 + \frac{R_f}{R_1} \tag{2.20}$$

The gain can be adjusted to unity or more, by proper selection of resistors R_f and R_1. Compared to the inverting amplifier, the input resistance of the non-inverting amplifier is extremely large (= ∞) as the op-amp draws negligible current from the signal source.

Practical Non-Inverting Amplifier

The analysis of a practical non-inverting amplifier can be performed by using the equivalent circuit shown in Fig. 2.7 (b). Writing KCL at the input node,

$$(v_i - v_d)\, Y_1 + v_d Y_i + (v_i - v_d - v_o) Y_f = 0$$

or,
$$-(Y_1 + Y_i + Y_f)\, v_d + (Y_1 + Y_f)\, v_i = Y_f v_o \tag{2.21}$$

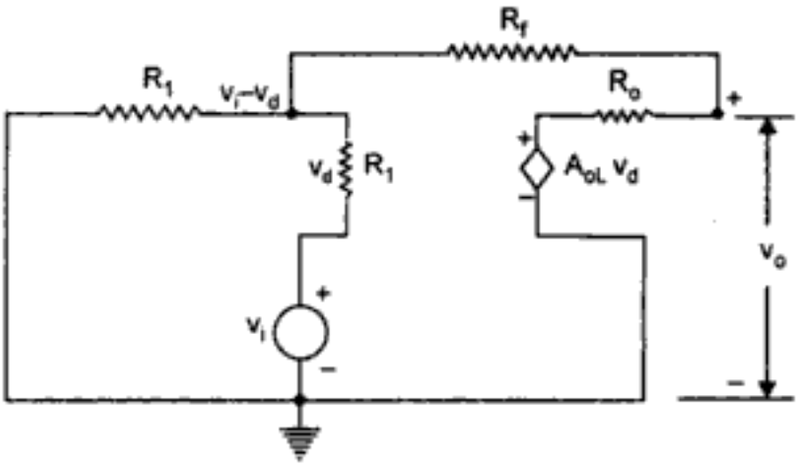


Fig. 2.7 (b) Equivalent circuit of non-inverting amplifier using low frequency model

Similarly at output node, KCL gives

$$(v_i - v_d - v_o)Y_f + (A_{OL}\, v_d - v_o)Y_o = 0$$

that is, $$-(Y_f - A_{OL}\, Y_o)\, v_d + Y_f v_i = (Y_f + Y_o)\, v_o \qquad (2.22)$$

Now solving Eqs. (2.21) and (2.22) for v_o/v_i, we get

$$A_{CL} = \frac{v_o}{v_i} = \frac{A_{OL}\, Y_o (Y_1 + Y_f) + Y_f Y_i}{(A_{OL} + 1)\, Y_o Y_f + (Y_1 + Y_i)(Y_f + Y_o)} \qquad (2.23)$$

where all admittances have been taken for simplicity.

If $A_{OL} \to \infty$, Eq. (2.23) reduces to

$$A_{CL} = \frac{A_{OL}\, Y_o (Y_1 + Y_f)}{A_{OL}\, Y_o Y_f} = \frac{Y_1 + Y_f}{Y_f} = 1 + \frac{Y_1}{Y_f}$$

$$= 1 + \frac{R_f}{R_1}$$

which is the same expression as in Eq. (2.20)

2.3.5 Voltage Follower

In the non-inverting amplifier of Fig. 2.7 (a) if $R_f = 0$ and $R_1 = \infty$, we get the modified circuit of Fig. 2.7 (c). From Eq. (2.20) we get,

$$v_o = v_i \qquad (2.24)$$

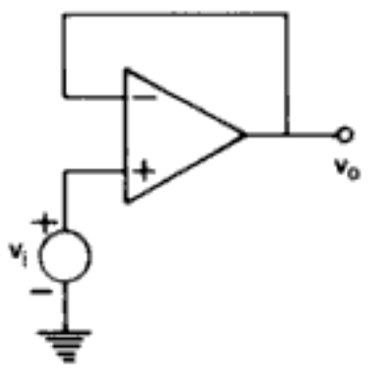


Fig. 2.7 (c) Voltage follower

That is, the output voltage is equal to input voltage, both in magnitude and phase. In other words, we can also say that the output voltage follows the input voltage exactly. Hence, the circuit is called a voltage follower. The use of the unity gain circuit lies in the fact that its input impedance is very high (i.e. MΩ order) and output impedance is zero. Therefore, it draws negligible current from the source. Thus a voltage follower may be used as buffer for impedance matching, that is, to connect a high impedance source to a low impedance load.

Example 2.3

Design an amplifier with a gain of +5 using one op-amp.

Solution

Since the gain is positive, we have to make a non-inverting amplifier. In Fig. 2.7 (a) select $R_1 = 10$ kΩ. Then from Eq. (2.20)

$$A_{CL} = 1 + R_f/R_1$$

or, $$5 = 1 + R_f/10 \text{ k}\Omega$$

or, $$R_f = 4 \times 10 \text{ k}\Omega = 40 \text{ k}\Omega$$

Example 2.4

In the circuit of Fig. 2.7 (a), let $R_1 = 5$ kΩ, $R_f = 20$ kΩ and $v_i = 1$ V. A load resistor of 5 kΩ is connected at the output as in Fig. 2.5 (b). Calculate, (i) v_o (ii) A_{CL} (iii) the load current i_L (iv) the output current i_o indicating proper direction of flow,

Solution

(i) $$v_o = \left(1 + \frac{R_f}{R_1}\right) v_i = \left(1 + \frac{20 \text{ k}\Omega}{5 \text{ k}\Omega}\right)(1 \text{ V}) = 5 \text{ V}$$

(ii) $$A_{CL} = \frac{v_o}{v_i} = \frac{5 \text{ V}}{1 \text{ V}} = 5$$

(iii) $$i_L = \frac{v_o}{R_L} = \frac{5 \text{ V}}{5 \text{ k}\Omega} = 1 \text{ mA}$$

(iv) $$i_1 = \frac{v_i}{R_1} = \frac{v_o - v_i}{R_f} = 0.2 \text{ mA}$$

Therefore, $i_o = i_L + i_1 = 1 \text{ mA} + 0.2 \text{ mA} = 1.02 \text{ mA}$

The op-amp output current i_o flows outwards from the output junction.

2.3.6 Differential Amplifier

A circuit that amplifies the difference between two signals is called a difference or differential amplifier. This type of the amplifier is very useful in instrumentation circuits (see section 4.3). A typical circuit is shown in Fig. 2.8. Since, the differential voltage at the input terminals of the op-amp is zero, nodes 'a' and 'b' are at the same potential, designated as v_3. The nodal equation at 'a' is,

$$\frac{v_3 - v_2}{R_1} + \frac{v_3 - v_o}{R_2} = 0 \tag{2.25}$$

and at 'b' is

$$\frac{v_3 - v_1}{R_1} + \frac{v_3}{R_2} = 0 \tag{2.26}$$

Rearranging, we get

$$\left(\frac{1}{R_1} + \frac{1}{R_2}\right) v_3 - \frac{v_2}{R_1} = \frac{v_o}{R_2} \tag{2.27}$$

$$\left(\frac{1}{R_1} + \frac{1}{R_2}\right) v_3 - \frac{v_1}{R_1} = 0 \tag{2.28}$$

Subtracting Eq. (2.28) from (2.27) we get,

$$\frac{1}{R_1}(v_1 - v_2) = \frac{v_o}{R_2} \tag{2.29}$$

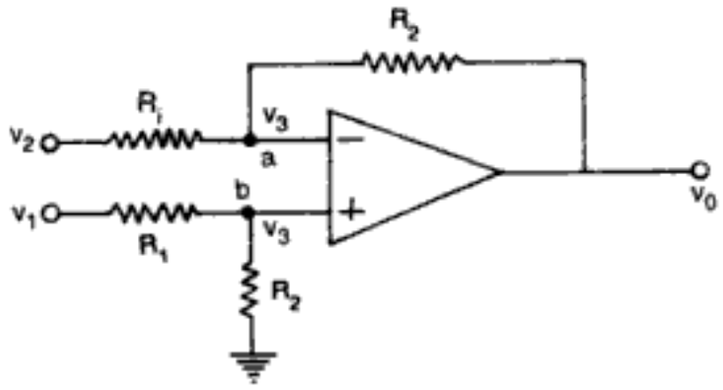


Fig. 2.8 A differential amplifier

Therefore,

$$v_o = \frac{R_2}{R_1}(v_1 - v_2) \tag{2.30}$$

Such a circuit is very useful in detecting very small differences in signals, since the gain R_2/R_1 can be chosen to be very large. For

example, if $R_2 = 100\ R_1$, then a small difference $v_1 - v_2$ is amplified 100 times.

Difference-mode and Common-mode Gains

In Eq. (2.30) if $v_1 = v_2$ then $v_o = 0$. That is, the signal common to both inputs gets cancelled and produces no output voltage. This is true for an ideal op-amp, however, a practical op-amp exhibits some small response to the common mode component of the input voltages too. For example, the output v_o will have different value for case (i) with $v_1 = 100\ \mu V$ and $v_2 = 50\ \mu V$ and case (ii) with $v_1 = 1000\ \mu V$ and $v_2 = 950\ \mu V$, even though the difference signal $v_1 - v_2 = 50\ \mu V$ in both the cases. The output voltage depends not only upon the difference signal v_d at the input, but is also affected by the average voltage of the input signals, called the common-mode signal v_{CM} defined as,

$$v_{CM} = \frac{v_1 + v_2}{2}$$

For differential amplifier, though the circuit is symmetric, but because of the mismatch, the gain at the output with respect to the positive terminal is slightly different in magnitude to that of the negative terminal. So, even with the same voltage applied to both inputs, the output is not zero. The output, therefore, must be expressed as,

$$v_o = A_1 v_1 + A_2 v_2 \tag{2.31}$$

where, A_1 (A_2) is the voltage amplification from input 1 (2) to the output with input 2(1) grounded. Since $v_{CM} = (v_1 + v_2)/2$ and $v_d = (v_1 - v_2)$,

$$v_1 = v_{CM} + \frac{1}{2} v_d \tag{2.32}$$

and

$$v_2 = v_{CM} - \frac{1}{2} v_d \tag{2.33}$$

Substituting the value of v_1 and v_2 in Eq. (2.31), we get

$$v_o = A_{DM}\, v_d + A_c\, v_c \tag{2.34}$$

where,

$$A_{DM} = \frac{1}{2}(A_1 - A_2) \tag{2.35}$$

and

$$A_{CM} = A_1 + A_2 \tag{2.36}$$

The voltage gain for the difference signal is A_{DM} and that for the common-mode signal is A_{CM}.

2.3.7 Common-Mode Rejection Ratio

The relative sensitivity of an op-amp to a difference signal as compared to a common-mode signal is called common-mode rejection ratio

(CMRR) and gives the figure of merit ρ for the differential amplifier. So, CMRR is given by:

$$\rho = \left| \frac{A_{DM}}{A_{CM}} \right| \tag{2.37}$$

and is usually expressed in decibels (dB). For example, the μA741 op-amp has a minimum CMRR of 70 dB whereas a precision op-amp such as μA725A has a minimum CMRR of 120 dB. Clearly, we should have A_{DM} large and A_{CM} should be zero ideally. So, higher the value of CMRR, better is the op-amp.

Example 2.5

In Fig. 2.9 is shown a differential amplifier using ideal op-amp.

(a) Find the output voltage v_o.

(b) Show that the output corresponding to common-mode voltage $v_{CM} = \frac{(v_1 + v_2)}{2}$ is zero if $\frac{R'}{R} = \frac{R_2}{R_1}$. Find v_o in this case.

(c) Find CMRR of the amplifier if $\frac{R'}{R} \neq \frac{R_2}{R_1}$

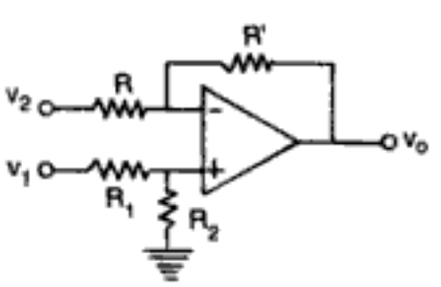


Fig. 2.9 Circuit of Example 2.5

Solution

The voltage at the non-inverting input terminal is $\frac{R_2}{R_1 + R_2} v_1$. Using principle of superposition and Eqs. (2.4) and (2.20), we have

$$\text{(a)}\quad v_o = -\frac{R'}{R} v_2 + \left(\frac{R + R'}{R}\right)\left(\frac{R_2}{R_1 + R_2} v_1\right) \tag{2.38}$$

$$\text{(b)}\quad v_{CM} = \frac{1}{2}(v_1 + v_2) \text{ and } v_d = (v_1 - v_2)$$

So, $v_1 = v_{CM} + \frac{v_d}{2}$ and $v_2 = v_{CM} - \frac{v_d}{2}$

v_o from Eq. (2.38) is,

$$v_o = -\frac{R'}{R}\left(v_{CM} - \frac{v_d}{2}\right) + \frac{R_2}{R}\,\frac{R+R'}{R_1+R_2}\left(v_{CM} + \frac{v_d}{2}\right)$$

$$= \left(\frac{R_2}{R}\,\frac{R+R'}{R_1+R_2} - \frac{R'}{R}\right)v_{CM} + \left(\frac{R'}{R} + \frac{R_2}{R}\,\frac{R+R'}{R_1+R_2}\right)\frac{v_d}{2} \qquad (2.39)$$

Now, if $\frac{R'}{R} = \frac{R_2}{R_1}$, we get,

$$\frac{R'}{R} + 1 = \frac{R_2}{R_1} + 1$$

or, $$\frac{R'+R}{R} = \frac{R_1+R_2}{R_1}$$

So, from Eq. (2.39) the term corresponding to v_{CM} is zero, and

$$v_o = \left(\frac{R'}{R} + \frac{R_2}{R_1}\right)\frac{v_d}{2} = \left(\frac{R_2}{R_1}\right)v_d \qquad (2.40)$$

(c) $\text{CMRR} = \dfrac{A_{DM}}{A_{CM}}$

From Eq. (2.39), find (i) $A_{DM} = v_o/v_d$ by putting $v_{CM} = 0$
and (ii) $A_{CM} = v_o/v_{CM}$ by putting $v_d = 0$
then we get

$$\text{CMRR} = \frac{R'(R_1+R_2) + R_2(R+R')}{R'(R_1+R_2) - R_1(R+R')} \qquad (2.41)$$

2.4 OPERATIONAL AMPLIFIER INTERNAL CIRCUIT

Commercial IC op-amps usually consists of four cascaded blocks as shown in Fig. 2.10. The first two stages are cascaded differential amplifiers used to provide high gain and high input resistance. The third stage acts as a buffer as well as a level shifter. The buffer is usually an emitter follower whose input impedance is very high so that it prevents loading of the high gain stage. The level shifter adjusts the d.c. voltages so that output voltage is zero for zero inputs. The adjustment of d.c. level is required as the gain stages are direct coupled. As it is not possible to fabricate large value of capacitors, all IC's are direct coupled usually. The output stage is designed to provide a low output impedance as demanded by the ideal op-amp characteristics. The output voltage should swing symmetrically with respect to ground. To allow such symmetrical swing, the amplifier is provided with both

positive and negative supply voltages. Power supply voltages of ± 15V are common. Additionally, an op-amp generally incorporates circuitry to provide drift compensation and frequency compensation which are discussed in section 3.3.3.

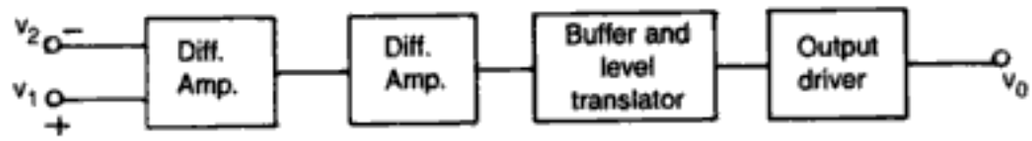


Fig. 2.10 Block schematic of an op-amp

Before describing the detailed IC circuit, we shall discuss each of the blocks in detail.

2.4.1 Differential Amplifier

The main purpose of the difference amplifier stage is to provide high gain to the difference-mode signal and cancel the common-mode signal. The relative sensitivity of an op-amp to a difference signal as compared to common-mode signal is called common-mode rejection ratio (CMRR) and gives the figure of merit of the differential amplifier. The higher the value of CMRR, better is the op-amp. Another requisite of a good op-amp is that it should have high input impedance. In this section, we discuss in detail, the various circuits and then modifications to achieve these characteristics of a good op-amp.

A cascaded dc amplifier can provide high gain down to zero frequency as it has no coupling capacitor. However, such an amplifier suffers from the major problem of drift of the operating point due to temperature dependency of I_{CBO}, V_{BE} and h_{FE} of the transistor. This problem can be eliminated by using a balanced or differential amplifier as shown in Fig. 2.11 (a). It may be seen that it is essentially an

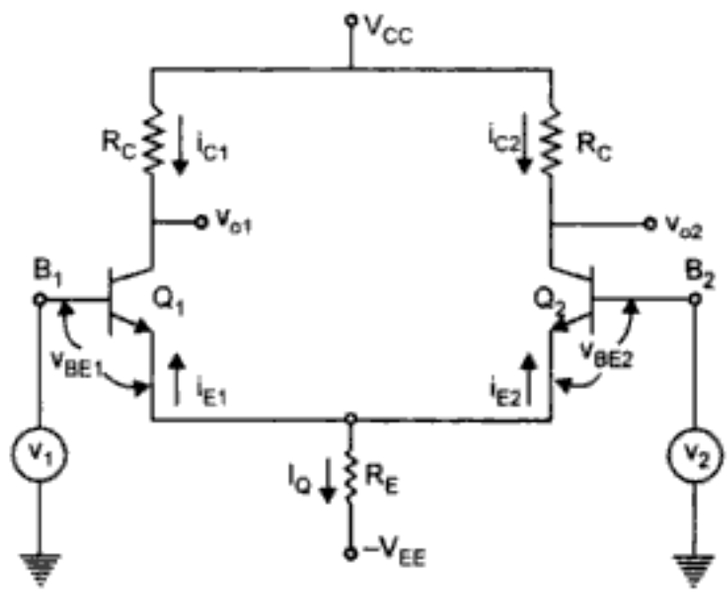


Fig. 2.11 (a) The basic differential amplifier

emitter-coupled differential amplifier. This circuit has low drift on account of symmetrical construction. It can be designed to give high input resistance. It has two input terminals and it may be seen easily that terminal B_2 is the inverting input terminal since transistor Q_2 provides a phase shift of 180° for the output taken at the collector of Q_2. Obviously, B_1 is the non-inverting input terminal. So, a differential amplifier is well suited to obtain the ideal characteristics of an op-amp as discussed in Sec. 2.3.

A differential amplifier of the type shown in Fig. 2.11 (a) can be used in four different configurations depending upon the number of input signals used and the way output is taken. These four configurations are:

(i) Differential-input, differential-output or Dual-input balanced-output
(ii) Differential-input, single ended-output
(iii) Single-input, differential-output
(iv) Single-input, single ended-output

If signal is applied to both the inputs, then it is differential input or Dual input and the difference of signals applied to the two inputs gets amplified. In many applications a single input is only used as we shall see later. Similarly, if output voltage is measured between two collectors then it is a differential output. This is also referred to as a balanced output, as both collectors are at the same d.c. potential w.r.t. ground. We will come across these various configuration as we proceed further.

To understand the working of a differential amplifier first consider the case when both the bases B_1 & B_2 are joined together and connected to a voltage v_{CM} called the common-mode voltage. Thus in Fig. 2.11 (b), $v_1 = v_2 = v_{CM}$. As transistors Q_1 and Q_2 are matched and due to symmetry of the circuit, the current I_Q divides equally through transistors Q_1 and Q_2, that is, $i_{E1} = i_{E2} = -I_Q/2$. The collector currents i_{C1} and i_{C2} through the resistors R_c is $\alpha_F I_Q/2$. The voltage at each of the collectors will be $V_{cc} - \alpha_F \frac{I_Q}{2} R_C$ and, therefore the difference of the voltage between the two collectors ($v_{01} - v_{02}$) will be zero. Now, even if the value of v_{CM} is changed, the voltage across the collectors will not change. Thus, the differential pair does not respond to (or rejects) the common-mode input signals. Now, consider the case when the voltage v_2 is made zero and voltage $v_1 = 1$ V (say) as shown in Fig. 2.11 (c). It can be seen that the transistor Q_1 will conduct and transistor Q_2 will be **off**. The entire current I_Q will now flow through Q_1. Since Q_1 is **on**, the voltage at its emitter will be 0.3 V. This will make emitter-base junction of Q_2 reverse-biased and thus Q_2 will be **off.** The collector voltages will be $v_{o1} = V_{CC} - \alpha_F I_Q R_C$ and $v_{o2} = V_{CC}$.

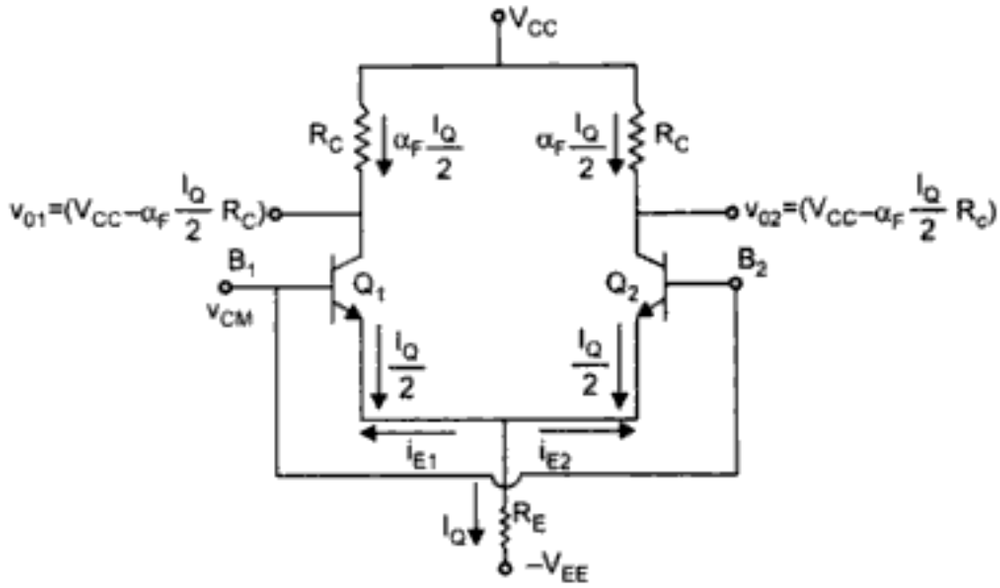


Fig. 2.11 (b) The differential pair with a common-mode input signal v_{CM}

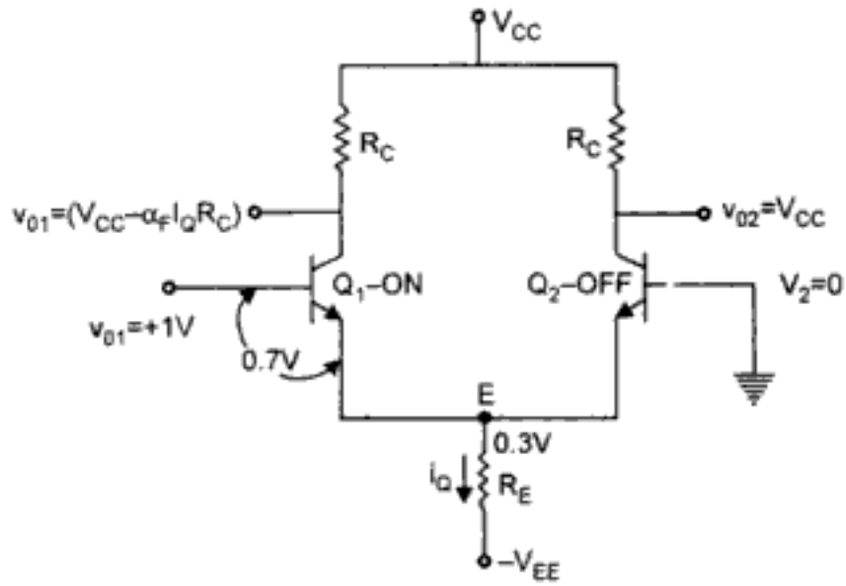


Fig. 2.11 (c) The differential pair with 'large' differential input signal

If, however, $v_1 = -1$ V and $v_2 = 0$ V, it can be seen that Q_1 will be **off** and the entire current I_Q will flow through Q_2. The voltage at the common emitter point '*E*' will now be – 0.7 V which makes Q_1 **off** and Q_2 **on**. The collector voltages will be $v_{01} = V_{CC}$ and $v_{02} = V_{CC} - \alpha_F I_Q R_C$.

Thus, we see that the differential pair responds only to the difference mode signals and rejects common-mode signals. In the next section, we discuss the transfer characteristics of the circuit to show that a differential pair can be used either as a switch or a linear amplifier.

2.4.2 Transfer Characteristics

In Fig. 2.11 (a) collector currents i_{C1} and i_{C2} for transistors Q_1 and Q_2 biased in the forward-active mode may be given by (neglecting reverse saturation currents of the collector base junction)

$$i_{C1} = \alpha_F I_{ES}\, e^{v_{BE1}/V_T} \tag{2.42}$$

$$i_{C2} = \alpha_F I_{ES}\, e^{v_{BE2}/V_T} \tag{2.43}$$

Here, I_{ES} is the reverse saturation current of emitter-base junction and V_T is volts equivalent of temperature.

From Eqs. (2.42) and (2.43), we may write

$$\frac{i_{C1}}{i_{C2}} = e^{(v_{BE1} - v_{BE2})/V_T} \tag{2.44}$$

We may also write KVL for the loop containing two emitter-base junctions as

$$v_1 - v_{BE1} + v_{BE2} - v_2 = 0$$

or
$$v_{BE1} - v_{BE2} = v_1 - v_2 = v_d$$

where, v_d is the difference of two input voltages.

Also in Fig. 2.11 (a)

$$I_Q = -(i_{E1} + i_{E2})$$

$$= \frac{i_{C1}}{\alpha_F} + \frac{i_{C2}}{\alpha_F}$$

$$= \frac{i_{C1}}{\alpha_F}\left(1 + \frac{i_{C2}}{i_{C1}}\right) \tag{2.45}$$

Using Eqs. (2.44) & (2.45) and solving for i_{C1} and i_{C2}, gives

$$i_{C1} = \frac{\alpha_F I_Q}{1 + e^{-v_d/V_T}} \tag{2.46}$$

$$i_{C2} = \frac{\alpha_F I_Q}{1 + e^{v_d/V_T}} \tag{2.47}$$

From Eqs. (2.46) and (2.47), the transfer characteristics (i_C vs v_d) for a differential amplifier are obtained as shown in Fig. 2.12.

The following important points are observed from the transfer characteristics:

1. For $v_d > 4\ V_T$ (~ 100 mV), $i_{C1} = \alpha_F I_Q$ and $i_{C2} = 0$, Hence
   $$v_{01} = V_{CC} - \alpha_F\, I_Q R_C$$
   and
   $$v_{02} = V_{CC}$$
   By proper choice of R_C, v_{01} can be made very small.
2. For $v_d < -4\ V_T$, $i_{C1} = 0$ and $i_{C2} = \alpha_F I_Q$. Hence $v_{01} = V_{CC}$ and V_{02} is negligible. Thus, for $4V_T < v_d < -4V_T$, we can say that a differential amplifier can be made to function as a switch.
3. The differential amplifier functions as a very good limiter for $v_d > \pm 4\ V_T$.

4. DA can function as an automatic gain control (AGC) by varying I_Q.
5. Between the values $-2V_T \leq v_d \leq 2V_T$, DA functions as a linear amplifier.

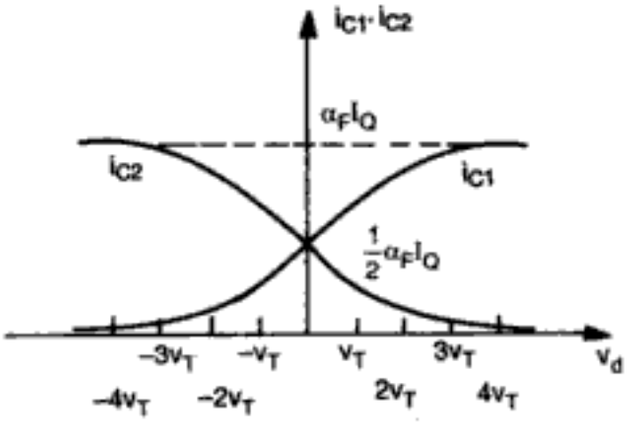


Fig. 2.12 Transfer characteristics (i_C vs v_d) for the differential pair

2.4.3 Low Frequency Small Signal Analysis of Differential Amplifier

An ideal dual-input balanced output differential amplifier as shown in Fig. 2.11 (a), should amplify only the differential signal at the two inputs and reject the signal common to these inputs. As transistors Q_1 and Q_2 are a matched pair of transistors, thus any unwanted signal, such as noise or hum pick up which is common to both the inputs would get rejected. However in a practical case transistors Q_1 and Q_2 are not equally matched and output does appear even when same voltage is applied to the two input terminals. In this section, we will discuss how to compute the small signal differential mode gain, A_{DM} and common-mode gain A_{CM}. These expressions help in finding the figure of merit CMRR of the differential amplifier and hence the ways to improve it.

The a.c. analysis of the differential amplifier can be performed either by using hybrid-π model or h-parameter model. Both the approaches have been dealt with.

Differential-mode gain, A_{DM}

In Fig. 2.11 (a) for $v_1 = v_2$, the current I_Q divides equally into the two transistors Q_1 and Q_2 because of the symmetry of the circuit. However, if v_1 is now increased by an incremental voltage (small signal) $v_d/2$ and v_2 is decreased by $v_d/2$, it can be seen that the differential amplifier is being fed by differential small signal v_d. The common mode small signal is naturally zero. The collector current i_{C1} will now increase by an incremental current i_c and i_{C2} will decrease by an equal amount. The sum of total currents in transistors Q_1 and Q_2 however remains constant as constrained by the constant current I_Q.

As there is no change of current through R_E, the voltage V_E at the common emitter point '*E*' remains constant. Thus, for small signal analysis, the common emitter point 'E' can be considered to be at ground potential. Fig. 2.13 (a) shows the small signal equivalent circuit of the differential amplifier under the differential input signal conditions described above. It may be noted that for differential amplifier to behave as a linear amplifier, the differential signal $v_d \leq 2V_T$ (that is, v_d should be smaller than about 50 mV) as discussed in the transfer characteristics (section 2.4.2).

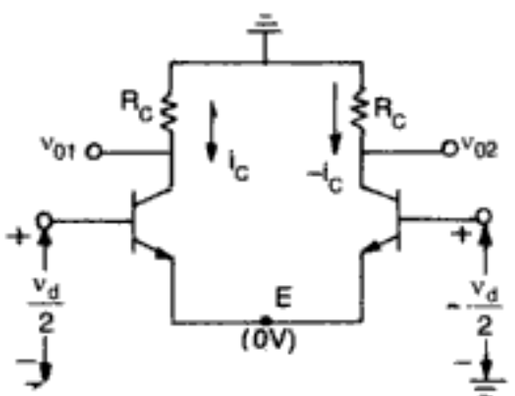


Fig. 2.13 (a) Differential amplifier when differential input signal applied.

Analysis

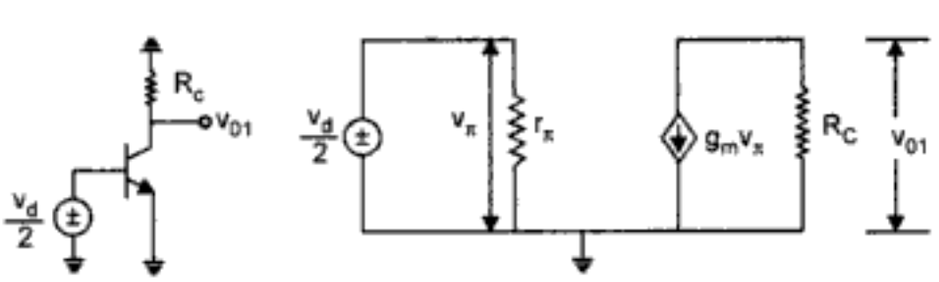
(i) *Using hybrid-π Model*

Since the performance of two sides of the differential amplifier is identical, we need to analyze only one side of the differential amplifier called differential-half circuit. Fig. 2.13 (b) shows a single stage CE transistor amplifier fed by a small signal voltage $v_d/2$ and it's a.c. equivalent circuit using hybrid-π model is shown in Fig. 2.13 (c).

From Fig. 2.13 (c),

$$\frac{v_{01}}{v_d/2} = -g_m R_C$$

or
$$\frac{v_{01}}{v_d} = -\frac{1}{2} g_m R_C \tag{2.48}$$



ig. 2.13 (b) Differential mode half circuit (c) ac-equivalent circuit using hybrid-π model.

Similarly, it can be seen that

$$\frac{v_{02}}{v_d} = \frac{1}{2} g_m R_C \tag{2.49}$$

The output voltage signal of a differential amplifier can be taken either differentially (i.e. between the two collectors) or single-ended (i.e. between one collector and ground). If the output is taken differentially, then the differential-mode gain, A_{DM} is given by

$$A_{DM} = \frac{v_{01} - v_{02}}{v_d} = -g_m R_C \text{ (differential-input, differential-output)} \tag{2.50}$$

On the other hand, if output is single-ended, (say between collector of transistor Q_1 and ground), then the differential-mode gain A_{DM} is given by

$$A_{DM} = \frac{v_{01}}{v_d} = -\frac{1}{2} g_m R_C \text{ (differential-input, single-ended output)} \tag{2.51(a)}$$

and

$$\frac{v_{02}}{v_d} = \frac{1}{2} g_m R_C \tag{2.51(b)}$$

In the above analysis, we have not included the transistor model parameter r_0. If r_0 is included, Eq. (2.50) will modify to

$$A_{DM} = -g_m (R_C \| r_0).$$

(ii) *Using 'h' parameters*

The a.c. equivalent circuit for Fig. 2.13(b) using approximate h-parameter model is shown in Fig. 2.13(d)

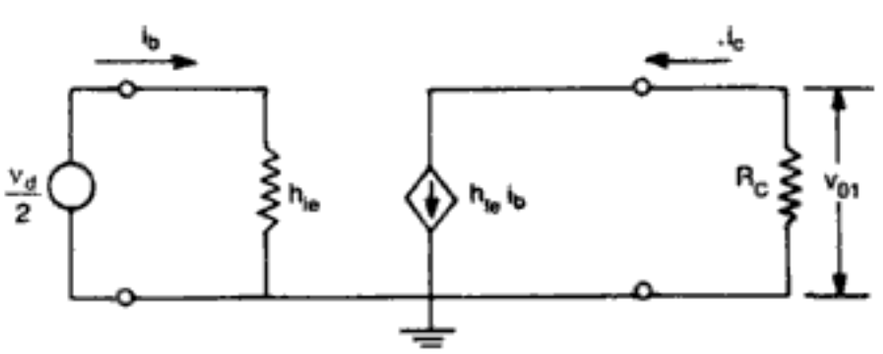


Fig. 2.13 (d) Small signal equivalent circuit of differential half circuit using h-parameter model

From Fig. 2.13 (d),

$$v_{01} = -i_C R_C = -h_{fe}\, i_b\, R_C$$

and

$$\frac{v_d}{2} = i_b h_{ie}$$

Therefore, differential mode gain, A_{DM} is given by

$$A_{DM} = \frac{v_{01}}{v_d} = -\frac{1}{2}\frac{h_{fe}}{h_{ie}} R_C \quad \text{(Single-ended output)} \qquad (2.52\ (a))$$

Similarly, we may write

$$A_{DM} = \frac{v_{02}}{v_d} = \frac{1}{2}\frac{h_{fe} R_C}{h_{ie}} \quad \text{(Single-ended output)} \qquad (2.52\ (b))$$

If the output is taken differentially between the two collectors, then

$$A_{DM} = \frac{v_{01} - v_{02}}{v_d} = -\frac{h_{fe} R_C}{h_{ie}} \quad \text{(differential-output)} \qquad (2.53)$$

In the above analysis, the source resistance R_s has not been taken into account.

Common-mode gain, A_{CM}

Now, consider the case when v_1 and v_2 both are increased by an incremental voltage v_c. The differential signal v_d now is zero and common-mode signal is v_c. Both the collector currents i_{C1} and i_{C2} will increase by an incremental current i_c. The current through R_E now increases by $2i_c$. The voltage, V_E at emitter node is now $2i_c R_E$ and no longer constant. In order to draw the common mode half circuit, replace resistance R_E by $2R_E$ as shown in Fig. 2.14 (a). The common-mode gain, A_{CM} is calculated from the small-signal hybrid-π equivalent model shown in Fig. 2.14 (b). It can be seen,

$$A_{CM} = \frac{v_{01}}{v_c} = \frac{v_{02}}{v_c} = \frac{-\beta_0 R_C}{r_\pi + 2(1+\beta_0)R_E} \qquad (2.54)$$

For $\beta_0 >> 1$,

$$A_{CM} = \frac{-g_m R_C}{1 + 2g_m R_E} \cong -\frac{R_C}{2R_E} \qquad (2.55)$$

It can be seen that, if the output is taken differentially, then the output voltage $v_{01} - v_{02}$ will be zero and the common-mode gain will be zero. However, if the output is taken single ended, the common-mode gain will be finite and given by Eqs. (2.54) and (2.55).

The common mode gain, A_{CM}, using h-parameter model can be easily computed as

$$A_{CM} = \frac{v_{01}}{v_c} = \frac{-h_{fe} R_C}{h_{ie} + (1 + h_{fe})2R_E} \qquad (2.56)$$

The common-mode rejection ratio (CMRR) is defined as

$$\text{CMRR} = \frac{|A_{DM}|}{|A_{CM}|}$$

For differential-input, differential-output, using Eqs (2.50) and (2.55), we obtain

$$\begin{aligned}\text{CMRR} &\cong \frac{g_m R_C (1 + 2 g_m R_E)}{g_m R_C} \\ &= 1 + 2 g_m R_E \\ &\cong 2 g_m R_E\end{aligned} \tag{2.57}$$

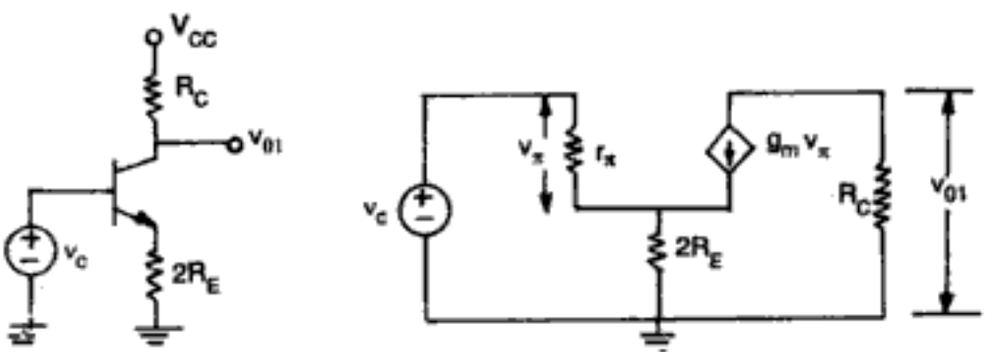


Fig. 2.14 (a) common-mode half circuit (b) ac equivalent ckt using hybrid-π model

2.4.4 Circuits for Improving CMRR

For CMRR to be large, A_{CM} should be as small as possible. From Eq. (2.56), it can be seen that $A_{CM} \to 0$ as $R_E \to \infty$. There are, however, practical limitations on the magnitude of R_E because of the quiescent dc voltage across it. If R_E is made large, the emitter supply V_{EE} will also have to be increased in order to maintain the proper quiescent current. And if the operating currents of the transistors are allowed to decrease, then h_{ie} will decrease, thereby decreasing h_{fe} too. This too will decrease the common mode rejection ratio.

The use of a constant current bias in place of R_E is found to be a practical solution to the problem discussed above. In Fig. 2.15, R_E is replaced by a constant current transistor circuit in which R_1, R_2 and R_3 can be adjusted to give the same quiescent conditions for the transistors Q_1 and Q_2 as in the original circuit of Fig. 2.11 (a). The modified circuit presents a very high effective emitter resistance R_E even for very small values of R_3. Typically, R_E is hundreds of kΩ even if R_3 is as small as 1 kΩ.

Let us calculate the current I_Q and verify that the emitter circuit really behaves as a constant current source. Writing KVL for the base circuit of Q_3, we get

$$V_{BE3} + I_3R_3 = V_D + (V_{EE} - V_D)\frac{R_2}{R_1 + R_2} \tag{2.58}$$

Here V_D represents the drop across the diode D. If the base current is neglected, then

$$I_Q \simeq I_3 = \frac{1}{R_3}\left(\frac{V_{EE}R_2}{R_1 + R_2} + \frac{V_DR_1}{R_1 + R_2} - V_{BE3}\right) \tag{2.59}$$

By proper choice of resistors R_1 and R_2, it is possible to set,

$$\frac{V_DR_1}{R_1 + R_2} = V_{BE3} \tag{2.60}$$

Then,
$$I_Q \simeq \frac{1}{R_3}\left(\frac{V_{EE}R_2}{R_1 + R_2}\right) \tag{2.61}$$

So, it can be seen that the current I_Q will be essentially constant as it does not depend upon signal voltages v_1 and v_2.

What is the use of the diode D in this circuit? The diode D makes I_Q independent of temperature. We know that V_{BE3} decreases approximately by 2.5 mV/°C and the diode D also has the same temperature dependence. Hence, the two variations cancel each other and I_Q becomes independent of temperature. It is usually difficult to satisfy Eq. (2.60) with a single diode D in the circuit of Fig. 2.15 as

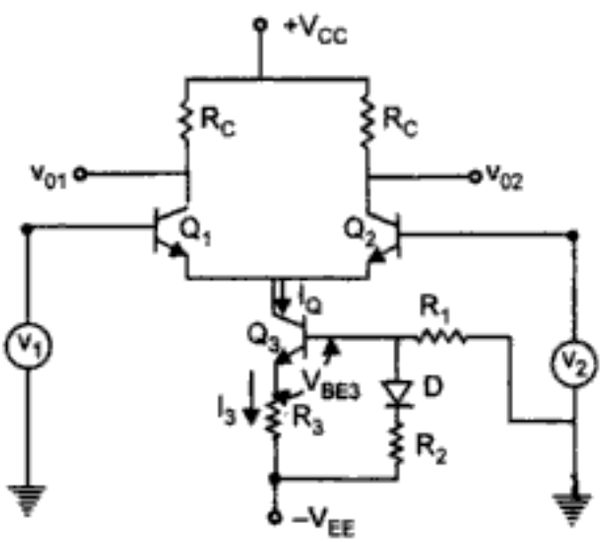


Fig. 2.15 Differential amplifier using constant current bias

V_D and V_{BE3} have almost the same value. Hence two diodes are normally used for V_D.

With I_Q constant, it can be shown that the common-mode gain is zero, so that the circuit provides very high CMRR. Under quiescent conditions (no ac signal) the current I_Q gets divided equally in identical

transistors Q_1 and Q_2 and $I_{C1} = I_{C2} = I_{Q/2}$. Now if the same signal ($v_1 = v_2$) is applied to both the inputs, there will still be no change in the collector currents i_{C1} and i_{C2} as I_Q is constant. Thus the small signal current i_c flowing through the load resistor R_C is zero resulting in zero output voltage. Thus we can state that a diff-amp, if supplied by a constant current bias gives very high CMRR. The constant current circuit of the type shown in Fig. 2.15 is used in Motorola MC1530 (Fig. 2.21). A more commonly used IC op-amp μA-741 uses a different type of constant current source which is very simple and uses less number of components. This circuit is called current mirror and offers extremely large resistance under a.c. conditions, thereby providing a high value of CMRR.

Constant Current Source (Current Mirror)

A constant current source makes use of the fact that for a transistor in the active mode of operation, the collector current is relatively independent of the collector voltage. In the basic circuit shown in Fig. 2.16 transistors Q_1 and Q_2 are matched as the circuit is fabricated using IC technology. It may be noted that bases and emitter of Q_1 and Q_2 are tied together and thus have the same V_{BE}. In addition, transistor Q_1 is connected as a diode by shorting its collector to base.

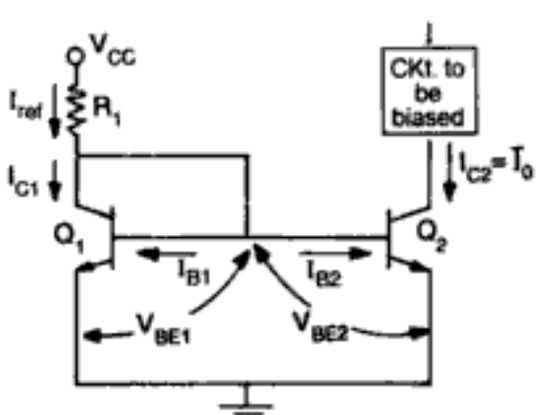


Fig. 2.16 The basic BJT current mirror

The input current I_{ref} flows through the diode-connected transistor Q_1 and thus establishes a voltage across Q_1. This voltage in turn appears between the base and emitter of Q_2. Since Q_2 is identical to Q_1, the emitter current of Q_2 will be equal to emitter current of Q_1 which is approximately equal to I_{ref}. Thus, we can say that as long as Q_2 is maintained in the active region, its collector current $I_{C2} = I_o$ will be approximately equal to I_{ref}. Since the output current I_o is a reflection or mirror of the reference current I_{ref}, the circuit is often referred to as a current mirror.

This mirror effect is however, valid only for large values of β. To study the effect of β on the operation of the current mirror circuit, we analyze it further.

Analysis

The collector currents I_{C1} and I_{C2} for transistors Q_1 and Q_2 can be approximately expressed as

$$I_{C1} \cong \alpha_F I_{ES}\, e^{V_{BE1}/V_T} \tag{2.62}$$

$$I_{C2} \cong \alpha_F I_{ES}\, e^{V_{BE2}/V_T} \tag{2.63}$$

From Eqns. (2.62) and (2.63), we may write

$$\frac{I_{C2}}{I_{C1}} = e^{(V_{BE2} - V_{BE1})/V_T} \tag{2.64}$$

Since $V_{BE1} = V_{BE2}$, we obtain

$$I_{C2} = I_{C1} = I_C = I_0$$

Also since both the transistors are identical, $\beta_1 = \beta_2 = \beta$.

KCL at the collector of Q_1 gives

$$I_{ref} = I_{C1} + I_{B1} + I_{B2} \tag{2.65}$$

$$= I_{C1} + \frac{I_{C1}}{\beta_1} + \frac{I_{C2}}{\beta_2}$$

$$= I_C\left(1 + \frac{2}{\beta}\right) \tag{2.66}$$

Solving Eq. (2.66), I_C may be expressed as

$$I_C = \frac{\beta}{\beta + 2} I_{ref} \tag{2.67}$$

where I_{ref} from Fig. 2.16 can be seen to be

$$I_{ref} = \frac{V_{CC} - V_{BE}}{R_1} \cong \frac{V_{CC}}{R_1} \text{ (as } V_{BE} = 0.7 \text{ V is small)} \tag{2.68}$$

From Eq. (2.67), for $\beta >> 1$, $\beta/(\beta + 2)$ is almost unity and the output current I_o is equal to the reference current, I_{ref} which for a given R_1 is constant. Typically I_o various by about 3% for $50 \le \beta \le 200$.

The circuit however operates as a constant current source as long as Q_2 remains in the active region. From the volt-ampere characteristics of Q_2 shown in Fig. 2.17, it can be seen that for $V_{CE2} < 0.3$ V, Q_2 is saturated. For $V_{CE2} > 0.3$ V, transistor operates in the active

region and I_{C2} is essentially constant. The slight increase in I_{C2} is due to Early effect. The slope of the curve in this region gives the output resistance r_0 of the current source.

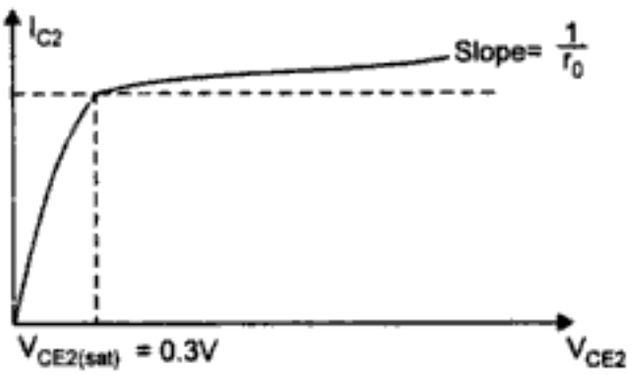


Fig. 2.17 Volt-ampere characteristics for current mirror

The consequences of Early effect is to deviate I_{C1}/I_{C2} from unity. These, however, are not being discussed here. For all practical purposes, Early voltage may be assumed to be infinite, so that $r_0 \to \infty$ and I_{C2} is constant.

Example 2.6

The current mirror of Fig. 2.16 is to provide a 1.0 mA current with V_{CC} = 10 V. Assume β = 125 and V_{BE} = 0.7 V. Determine (a) the value of R_1 (b) value of R_1 for I_C = 10 μA.

Solution

(a) From Eq. (2.67), we have

$$1.0 \text{ mA} = \frac{125}{125+2} \times \frac{10 \text{ V} - 0.7 \text{ V}}{R_1}$$

$$R_1 = 9.15 \text{ k}\Omega$$

(b) Again using Eq. (2.67), the value of R_1 is found to be

$$R_1 = 915 \text{ k}\Omega$$

Widlar current source

The basic current mirror of Fig. 2.16 has a limitation. Whenever, we need low value current source as in example 2.6 part (b), the value of the resistance R_1 required is sufficiently high and can not be fabricated economically in IC circuits. In Fig. 2.18 is shown a widlar current source which is particularly suitable for low value of currents. The circuit differs from the basic current mirror only in the resistance R_E that is included in the emitter lead of Q_2. It can be seen that due to R_E, the base-emitter voltage V_{BE2} is less than V_{BE1} and consequently current I_0 is smaller than I_{C1}.

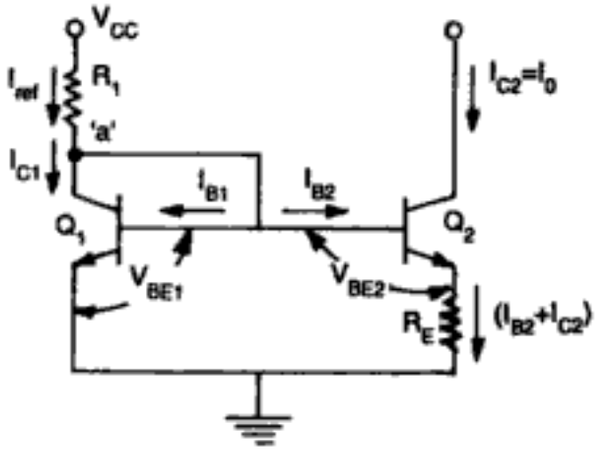


Fig. 2.18 Widlar current source

The ratio of collector currents I_{C1} and I_{C2} using Eqs. (2.62) and (2.63) is given by

$$\frac{I_{C1}}{I_{C2}} = e^{(V_{BE1} - V_{BE2})/V_T} \tag{2.69}$$

Taking natural logarithm of both sides, we get

$$V_{BE1} - V_{BE2} = V_T \ln\left(\frac{I_{C1}}{I_{C2}}\right) \tag{2.70}$$

Writing KVL for the emitter base loop

$$V_{BE1} = V_{BE2} + (I_{B2} + I_{C2})R_E \tag{2.71}$$

or
$$V_{BE1} - V_{BE2} = (1/\beta + 1)\, I_{C2}R_E \tag{2.72}$$

From Eqs. (2.70) and (2.72) we obtain

$$\left(\frac{1}{\beta} + 1\right) I_{C2}R_E = V_T \ln \frac{I_{C1}}{I_{C2}} \tag{2.73}$$

or
$$R_E = \frac{V_T}{\left(1 + \frac{1}{\beta}\right) I_{C2}} \ln \frac{I_{C1}}{I_{C2}} \tag{2.74}$$

A relation between I_{C1} and the reference current I_{ref} is obtained by writing KCL at the collector point of Q_1 (note 'a')

$$I_{ref} = I_{C1} + I_{B1} + I_{B2} \tag{2.75}$$

$$= I_{C1}\left(1 + \frac{1}{\beta}\right) + \frac{I_{C2}}{\beta} \tag{2.76}$$

(Assuming $\beta_2 = \beta_1 = \beta$ for identical transistors)

In the widlar current source $I_{C2} << I_{C1}$, therefore the term I_{C2}/β may be neglected in Eq. (2.76).

Thus $$I_{ref} \cong I_{C1}\left(1+\frac{1}{\beta}\right) \tag{2.77}$$

or $$I_{C1} = \frac{\beta}{\beta+1} I_{ref} \tag{2.78}$$

where $$I_{ref} = \frac{V_{CC} - V_{BE}}{R_1} \tag{2.79}$$

For $\beta >> 1$, $$I_{C1} \cong I_{ref} \tag{2.80}$$

The design and advantages of Widlar current source are illustrated in the following example:

Example 2.7

Design a Widlar current source for generating a constant current $I_0 = 10\ \mu A$. Assume $V_{CC} = 10\ V$, $V_{BE} = 0.7\ V$, $\beta = 125$. Use $V_T = 25\ mV$.

Solution

For the Widlar current source of Fig. 2.18, we must first decide a suitable value for I_{ref}. If we choose $I_{ref} = 1\ mA$, then, R_1 is given by

$$R_1 = \frac{10\,V - 0.7\,V}{1\,mA} = 9.3\,k\Omega$$

The value of R_E is determined from Eq. (2.74)

$$R_E = \frac{0.025}{\left(1+\frac{1}{125}\right)10\times10^{-6}} \ln\left(\frac{1\,mA}{10\,\mu A}\right)$$

$$= 11.5\ k\Omega$$

It is clearly seen that Widlar circuit allows the generation of small constant using relatively small resistors.

Sometimes, it is convenient to use emitter resistances in both the transistors Q_1 and Q_2 as shown in Fig. 2.19. If $R_1 = R_2$ the currents $I_{C1} = I_{C2}$. The same circuit can also be used to provide different currents in Q1 and Q2, as we shall now see.

Analysis

Rewriting Eq. (2.64) as

$$V_{BE2} - V_{BE1} = V_T \ln \frac{I_{C2}}{I_{C1}} \tag{2.81}$$

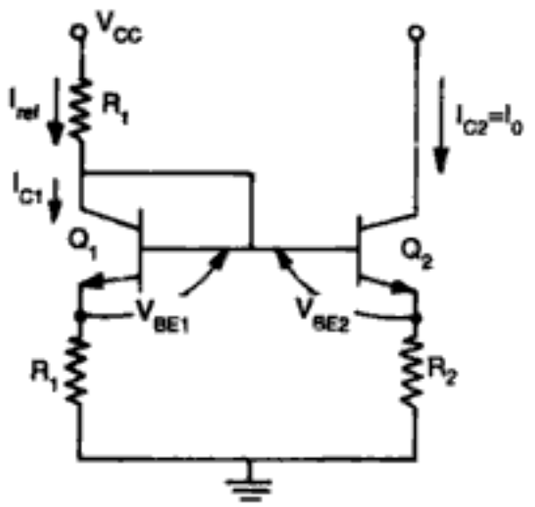


Fig. 2.19 A current mirror with magnification ($I_{c2}/I_{c1} \cong R_1/R_2$)

Writing KVL in the base-emitter loop

$$V_{BE2} - V_{BE1} = I_{C1}R_1 - I_{C2}R_2 \text{ (Neglecting base current)} \quad (2.82)$$

From Eq. (2.81) and Eq. (2.82),

$$I_{C1}R_1 - I_{C2}R_2 = V_T \ln \frac{I_{C2}}{I_{C1}} \quad (2.83)$$

$$\frac{I_{C2}}{I_{C1}}\frac{R_2}{R_1} = 1 - \frac{V_T}{I_{C1}R_1} \ln \frac{I_{C2}}{I_{C1}} \quad (2.84)$$

$$\frac{I_{C2}}{I_{C1}} = \frac{R_1}{R_2}\left(1 - \frac{V_T}{I_{C1}R_1} \ln \frac{I_{C2}}{I_{C1}}\right) \quad (2.85)$$

For the range $0.1 < \frac{I_{C2}}{I_{C1}} < 10$, we can assume $\frac{I_{C2}}{I_{C1}} \cong \frac{R_1}{R_2}$. Thus even large ratios $\frac{I_{C2}}{I_{C1}}$ (say 10) is easily obtained by the modified circuit.

Current Repeaters

The basic current mirror of Fig. 2.16 can be used to source current to more than one load. Such a circuit is called current repeater and is shown in Fig. 2.20. If all the transistors are identical, then the current $I_C = I_{C1} = \ldots \ldots = I_{CN} \cong I_{ref}$.

It can be seen from Fig. 2.20 at node 'a'

$$I_{ref} = I_C + I_B + N I_B \text{ (Assuming identical transistors)} \quad (2.86)$$

$$= I_C + \frac{(1+N)}{\beta} I_C$$

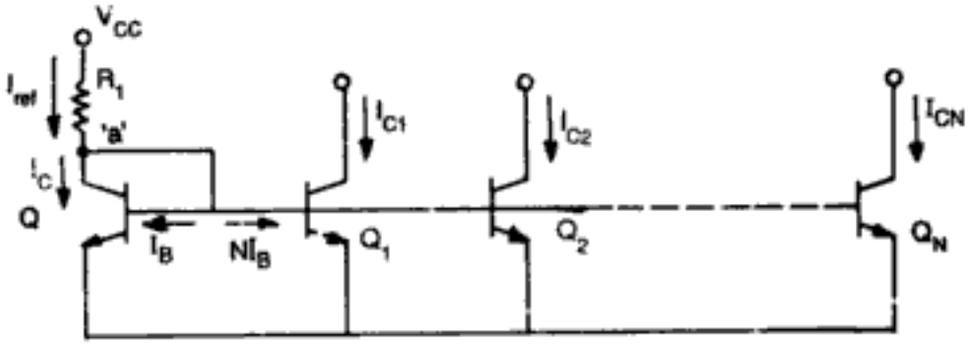


Fig. 2.20 A current repeater to source current to N transistors $Q_1, Q_2, \ldots \ldots Q_N$

$$= I_C\left(1+\frac{(1+N)}{\beta}\right) \tag{2.87}$$

$$\text{Thus } I_C = I_{ref}\frac{\beta}{\beta+1+N} \tag{2.88}$$

It is possible to achieve different value of I_{C1}, I_{C2}, ... I_{CN} by scaling the emitter area of transistors Q_1, Q_2, ... Q_N. The same can also be achieved by using emitter resistance as it illustrated by the example that follows.

Example 2.8

For the circuit shown in Fig. 2.21 determine I_{C1}, I_{C2}, and I_{C3}. Assume $\beta = 125$

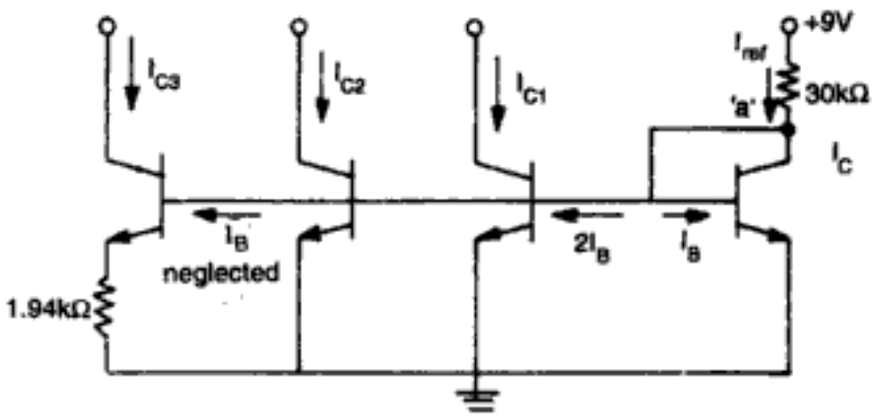


Fig. 2.21 Circuit for Example 2.8

Solution

$$I_{ref} = \frac{9\text{V} - 0.7\text{V}}{30\ \text{k}\Omega} = 0.277\ \text{mA}$$

Also at node 'a'

$$I_{ref} = I_C + 3I_B \text{ (Assume } I_{B3} \text{ of Widlar source negligible)}$$

$$= I_C\left(1+\frac{3}{\beta}\right)$$

$$I_C = I_{ref}\left(\frac{\beta}{3+\beta}\right)$$

Putting the values and solving, we get,

$$I_{C1} = I_{C2} = 0.271 \text{ mA}$$

Calculate I_{C3}, using Eq. (2.74) gives

$$1.94 = \frac{0.025}{I_{C3}\left(1+\frac{1}{125}\right)} \ln \frac{0.271}{I_{C3}}$$

Solving the transcendental equation by trial and error, we obtain

$$I_{C3} = 0.0287 \text{ mA}$$

Improved current source circuits

A good current source must meet two requirements. The first is that the output current, I_0 should not be dependent upon β and secondly the output resistance of the current source should be very high. The need for high output resistance current source can be seen because the common-mode gain of the differential amplifier (used as basic building block in op-amps) can only be reduced by using high resistance current sources. Also, all differential amplifiers invariably use current source as a load. Thus to obtain high voltage gain a large output resistance load is required. Now, we discuss two circuits that exhibit reduced dependence on β or increased output resistance.

A current source with gain

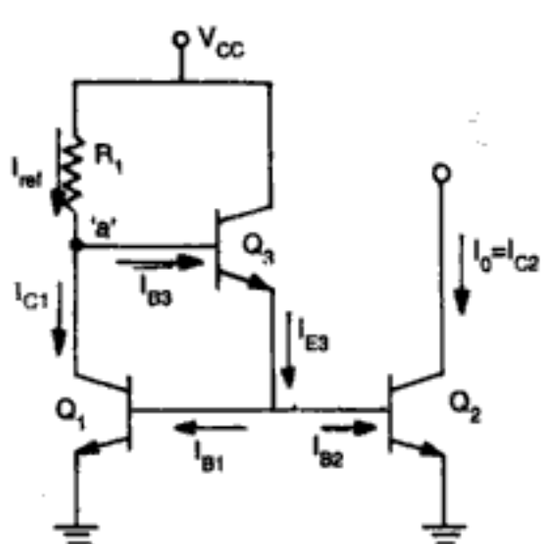


Fig. 2.22 A current source with gain

The circuit shown in Fig. 2.22 includes a transistor Q_3 whose emitter current supplies the base currents of Q_1 and Q_2. The expression for the source current $I_0 = I_{C2}$ be derived by writing KCL at node 'a'

$$I_{ref} = I_{C1} + I_{B3}$$

$$= I_{C1} + \frac{I_{E3}}{1+\beta}$$

$$= I_{C2} + \frac{I_{E3}}{1+\beta} \quad (V_{BE1} = V_{BE2}\ ;\ I_{C1} = I_{C2} = I_o) \qquad (2.89)$$

Also $$I_{E3} = I_{B1} + I_{B2}$$

$$= 2I_B \qquad \text{(since } Q_1 \text{ and } Q_2 \text{ are identical)}$$

Thus,

$$I_{ref} = I_{C1} + \frac{2I_B}{1+\beta} \qquad (2.90)$$

$$= I_C + \frac{2I_C}{\beta(1+\beta)}$$

$$= I_C\left(1 + \frac{2}{\beta(1+\beta)}\right)$$

or $$I_0 = I_C = I_{ref}\,\frac{\beta(1+\beta)}{\beta^2+\beta+2} \qquad (2.91)$$

It is easily seen from Eq. (2.91) that the output current is essentially independent of β. The output resistance of the current source is only r_0. It can however be increased by using emitter resistances in Q_1 and Q_2 as is done in the modified Widlar source circuit in Fig. 2.19. The two emitter resistors can also be used to make I_0 different from I_{ref}.

Wilson current source

The final current source shown in Fig. 2.23 provides an output current I_0, which is very nearly equal to I_{ref} and also exhibits a very high output resistance.

Analysis

Since $$V_{BE1} = V_{BE2}$$

$$I_{C1} = I_{C2} \text{ and } I_{B1} = I_{B2} = I_B$$

At node 'b'

$$I_{E3} = 2I_B + I_{C2}$$

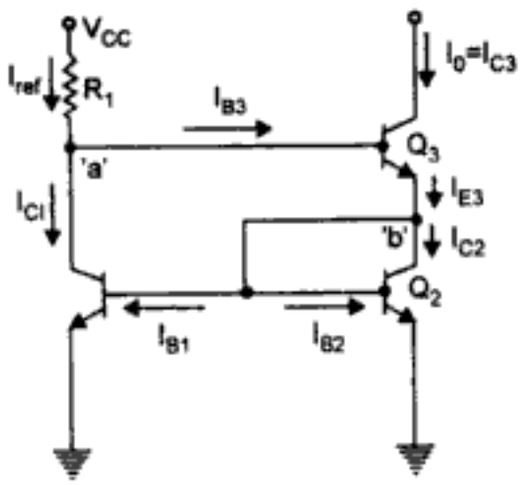


Fig. 2.23 A Wilson current source

$$= \left(\frac{2}{\beta} + 1\right) I_{C2} \tag{2.92}$$

I_{E3} is also equal to

$$I_{E3} = I_{C3} + I_{B3}$$

$$= I_{C3}\left(1 + \frac{1}{\beta}\right) \tag{2.93}$$

From Eqs. (2.92) and (2.93), we obtain

$$I_{C3}\left(1 + \frac{1}{\beta}\right) = I_{C2}\left(1 + \frac{2}{\beta}\right)$$

$$I_{C3} = I_0 = \left(\frac{\beta + 2}{\beta + 1}\right) I_{C2} \tag{2.94}$$

Since $I_{C1} = I_{C2}$

$$I_0 = \left(\frac{\beta + 2}{\beta + 1}\right) I_{C1} \tag{2.95}$$

At node 'a'

$$I_{ref} = I_{C1} + I_{B3}$$

$$= \frac{\beta + 1}{\beta + 2} I_0 + \frac{I_0}{\beta}$$

$$= \frac{\beta^2 + 2\beta + 2}{\beta^2 + 2\beta} I_0$$

or $$I_0 = \frac{\beta^2 + 2\beta}{\beta^2 + 2\beta + 2} I_{ref} \quad (2.96)$$

where $$I_{ref} = \frac{V_{CC} - 2V_{BE}}{R_1} \quad (2.97)$$

The difference $$I_0 - I_{ref} = \frac{2}{\beta^2 + 2\beta + 2} I_{ref} \quad (2.98)$$

is extremely small error for modest values of β. The output resistance of a Wilson current mirror is substantially greater $\left(\cong \beta \frac{r_0}{2}\right)$ than simple current mirror or Widlar current mirror.

More Solved Examples

Example 2.9

For the circuit shown in Fig. 2.24, determine the value of I_0 for β = 100. Assume V_{BE} = 0.7 V

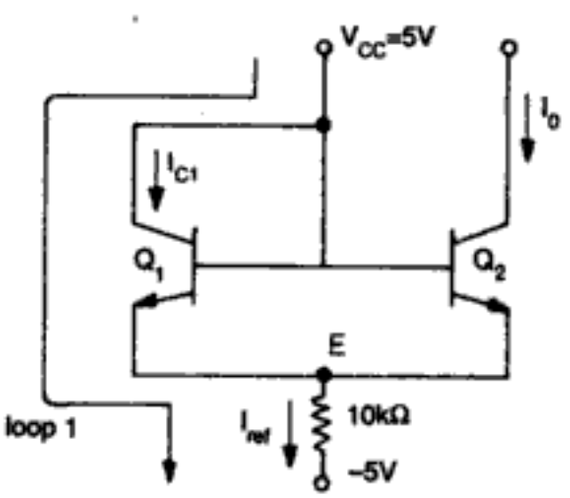


Fig. 2.24 Circuit for Example 2.9

Solution

Writing KVL for the indicated loop 1

$$5\text{V} - V_{BE} - 10\ \text{k}\Omega \times I_{ref} + 5\text{V} = 0$$

$$I_{ref} = \frac{10\text{V} - 0.7}{10\ \text{k}\Omega} = 0.93\ \text{mA}$$

At emitter node '*E*'

$$I_{ref} = 2I_E \quad \text{(Assuming identical transistors)}$$

$$= 2(I_C + I_B)$$

$$= 2I_C\left(1 + \frac{1}{\beta}\right)$$

Then $$I_C = \frac{\beta}{2(1+\beta)} I_{ref} = 0.46 \text{ mA}$$

Due to mirror effect $I_0 = I_{C1} = I_C = 0.46$ mA

Example 2.10

For the circuit shown in Fig. 2.25.

(a) Determine I_{C1} and I_{C2}

(b) Find R_C so that $V_0 = 6$ V. Assume $\beta = 200$

Solution

(a) $$I_{ref} = \frac{12\text{ V} - 0.7\text{ V}}{15\text{ k}\Omega} = 0.75 \text{ mA}$$

and $$I_1 = \frac{0.7\text{V}}{2.8\text{ k}\Omega} = 0.25 \text{ mA}$$

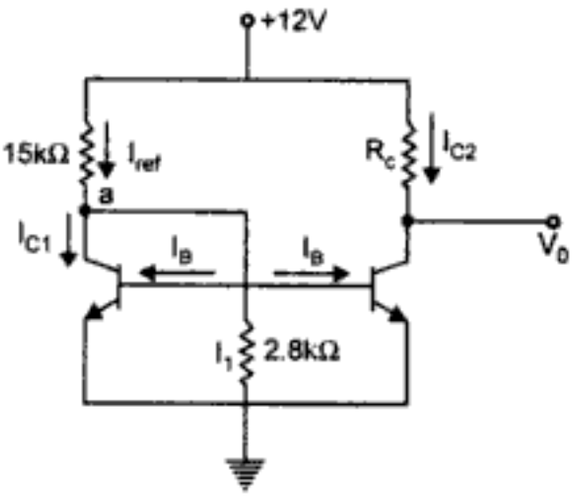


Fig. 2.25 Circuit for Example 2.10

At node 'a'

$$I_{ref} = I_{C1} + 2I_B + I_1$$

$$= I_{C1}\left(1 + \frac{2}{\beta}\right) + I_1$$

Solving for I_{C1} gives

$$I_{C1} = 0.495 \text{ mA}$$

$$\cong 0.5 \text{ mA}$$

$$I_{C2} = I_{C1} \qquad \text{(due to mirror effect)}$$

(b) From the outer loop

$$12\text{ V} = I_{C2}R_C + V_0$$

$$R_C = \frac{12\text{ V} - 6\text{ V}}{0.5\text{ mA}} = 12\text{ k}\Omega$$

Example 2.11

Figure 2.26 shows a modified current mirror circuit. Determine the emitter current in transistor Q_3 if $\beta = 100$ and $V_{BE} = 0.75\,V$.

Solution

From Fig. 2.26 at node 'a'

$$I = I_{C1} + I_1$$

$$= I_{C1} + I_{B1} + I_1'$$

or,
$$I = I_{C1}\left(1 + \frac{1}{\beta}\right) + I_1'$$

$$\simeq I_{C1} + I_1' \qquad (\text{as } \beta >> 1)$$

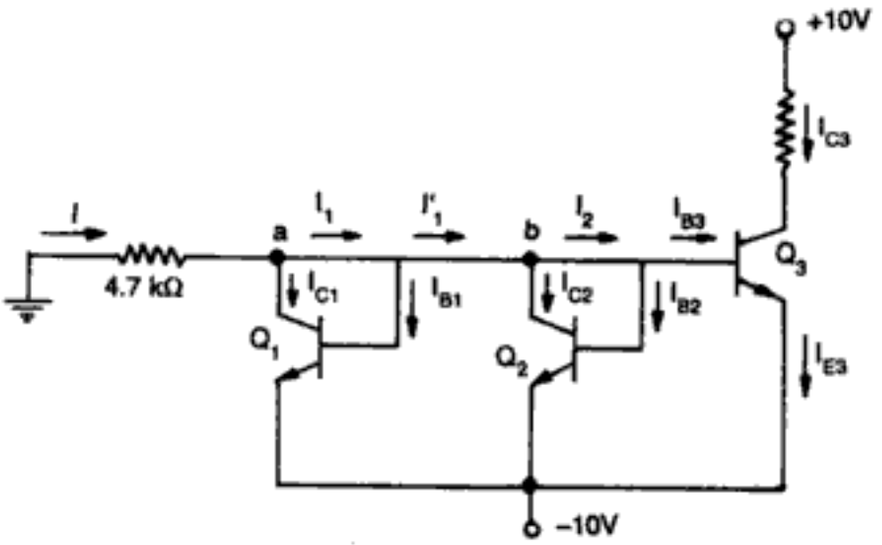


Fig. 2.26 Circuit of Example 2.11

Also at node 'b'

$$I_1' = I_{C2} + I_2$$

$$= I_{C2} + I_{B2} + I_{B3}$$

$$= I_{C2}\left(1 + \frac{1}{\beta}\right) + I_{B3}$$

$$\simeq I_{C2} + I_{B3}$$

Putting the value of I_1', we get

$$I = I_{C1} + I_{C2} + I_{B3}$$

$$= 2I_C + I_{B3} \qquad [\text{as } I_{C1} = I_{C2} = I_C]$$

$$\simeq I_C\left(2 + \frac{1}{\beta}\right) \simeq 2I_C$$

The current I is given by,

$$I = \frac{10 - 0.75}{4.7\ \text{k}\Omega} = \frac{9.25}{4.7\ \text{k}\Omega} = 1.97\ \text{mA}$$

The collector current of Q_3 is equal to the collector current of Q_1 and Q_2 due to mirror action. Therefore, the emitter current

$$I_{E3} \simeq I_{C3} = I_C = \frac{I}{2} = 0.98\ \text{mA}$$

2.4.5 Input Resistance

The resistance offered by the differential amplifier of Fig. 2.27 to the differential input signal $(v_1 - v_2)$ is called differential input resistance R_{id}. The emitters of Q_1 and Q_2 are floating as R_E is replaced by a constant current source, therefore $R_{id} \simeq h_{ie1} + h_{ie2} = 2\ h_{ie}$. If input 2 is grounded, then input 1 is loaded by $2\ h_{ie}$. The value of h_{ie} can be increased by reducing the biasing currents for Q_1 and Q_2 and input resistance of the order of 500 kΩ can be obtained.

Higher values of input resistance can be obtained by using a Darlington pair in place of transistor Q_1 and Q_2 of Fig. 2.27 as shown in Fig. 2.28. One drawback of the Darlington differential amplifier is the higher offset voltage V_{os}, (due to cascaded stages) which is about 2 times larger than the ordinary two transistor differential amplifier.

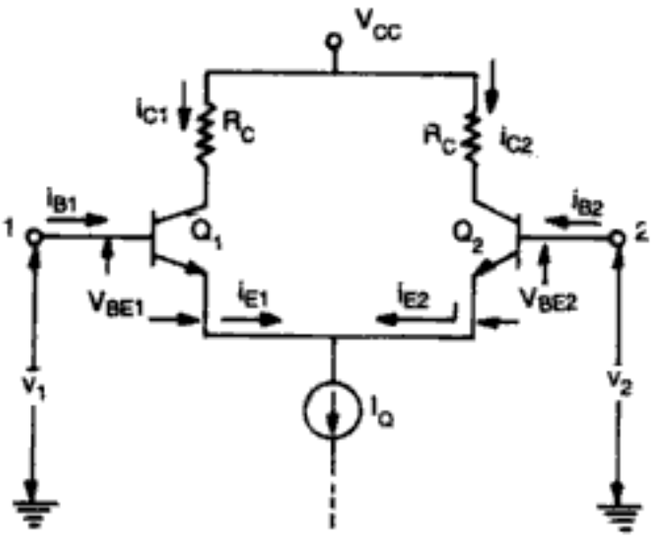


Fig. 2.27 Differential amplifier

The most important feature of the Darlington pair differential amplifier is its extraordinary large current gain. For the circuit shown in Fig. 2.28, the overall current gain is

$$\beta = \frac{I_C}{I_{B1}} = \frac{I_{C1} + I_{C2}}{I_{B1}}$$

$$= \frac{I_{C1}}{I_{B1}} + \frac{I_{C2}}{I_{B1}}$$

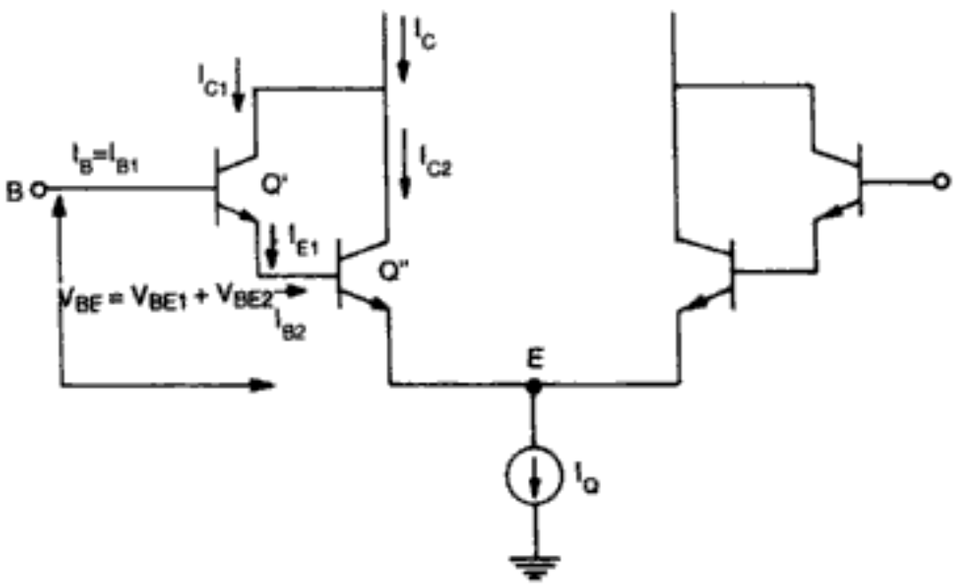


Fig. 2.28 Differential amplifier using Darlington pair

$$= \frac{I_{C1}}{I_{B1}} + \frac{I_{C2}}{I_{B2}} \times \frac{I_{B2}}{I_{B1}}$$

$$= \beta_1 + \beta_2 (\beta_1 + 1) \quad \left[\begin{matrix} I_{B2} = I_{E1} \\ = I_{C1} + I_{B1} \end{matrix} \right]$$

$$\cong \beta_2 \beta_1$$

So, the overall current gain β of the Darlington circuit will be of the order of 10,000 if the current gain of the individual transistor is about 100. Another method to get higher input resistance is to fabricate a FET differential pair as the input stage with the rest of the stages made of BJTs. Input resistance of the order of $10^{12}\Omega$ is possible with such JFET inputs. A number of such op-amps are described in Sec. 2.6.

2.4.6 Active Load

The open circuit voltage gain of an op-amp should be as large as possible and this is achieved by cascading gain stages. However, this increases the phase shift too and amplifier becomes more susceptible to breaking out into oscillations. One can think of increasing gain by using large collector resistance values as gain is proportional to load resistor R_C. However, there are limitations to the maximum value of R_C to be used due to the following two reasons:

(i) A large value of resistance requires a large chip area.

(ii) For large R_C quiescent drop across it increases and hence a large power supply will be required to maintain a given quiescent collector current. These difficulties are circumvented by using a current source of the type shown in Fig. 2.16 as load in the place of R_C.

The current mirror discussed earlier has a dc resistance of the order of few kilohms, as the quiescent voltage across it is a fraction of the supply voltage and the current is in milliamperes. However, since it acts as a constant current source, its dynamic resistance (ac) is very high. Hence, a current mirror can also be used as an active load for an amplifier to obtain a very large voltage gain. Figure 2.29 (a) shows a diff-amp with an active load. The current mirror uses *pnp* transistors Q_3 and Q_4. The constant current I_Q may also be obtained from a current mirror. The operation of the circuit in Fig. 2.29 (a) is as follows:

Under the quiescent conditions, $v_1 = v_2 = 0$. From symmetry of Q_1 and Q_2, $I_1 = I_2 = I_Q/2$ where base currents are assumed to be neglected. Since Q_3 and Q_4 form a current mirror, $I = I_1 = I_2$. The load current I_L entering the next stage is

$$I_L = I - I_2 = 0 \tag{2.99}$$

However, when v_1 is increased over v_2, I_1 increases whereas I_2 decreases, since $I_1 + I_2 = I_Q$ (constant). Also the current I always remains equal to I_1 due to the current mirror. The load current is given by

$$\begin{aligned} I_L &= I - I_2 = I_1 - I_2 \\ &= g_m v_1 - g_m v_2 \\ &= g_m (v_1 - v_2) \\ &= g_m v_d \end{aligned} \tag{2.100}$$

The circuit thus behaves as a transconductance amplifier.

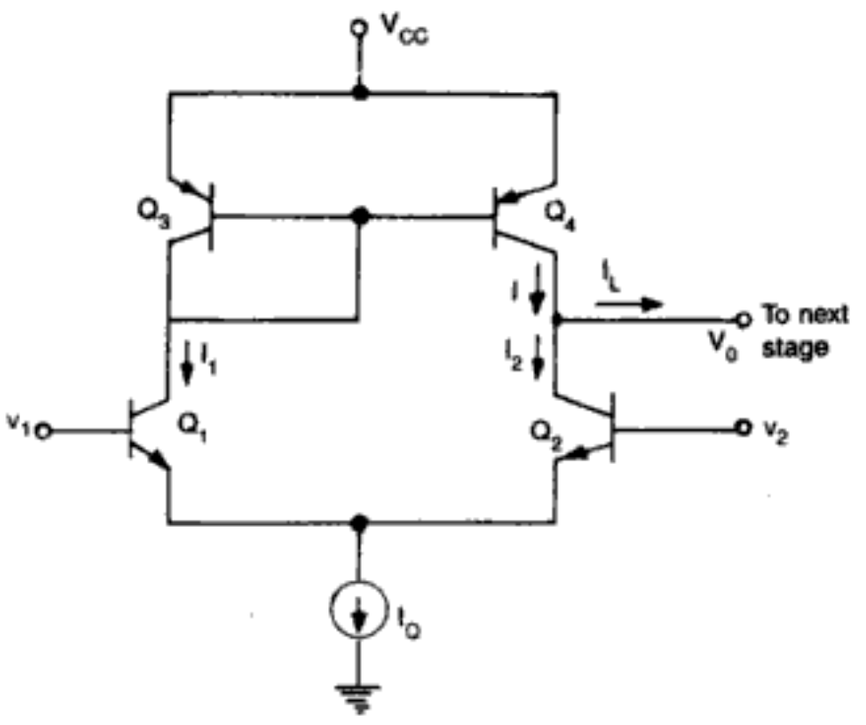


Fig. 2.29 (a) A differential amplifier with an active load Q_3–Q_4

A popular op-amp (μA 741) by Fairchild uses an alternate active load as shown in Fig. 2.29 (b). The transistors Q_1–Q_3 and Q_2–Q_4 are in cascode configuration (*CE-CB*) with input signal as v_1 (v_2). The transistors Q_5, Q_6 and Q_7 form the active load of the type shown in Fig. 2.22. The transistors Q_8 and Q_9 form the current mirror to provide the constant current I_Q required for high CMRR of the diff-amp. If base currents are neglected, then $I_Q \simeq I_3$. The arrangement Q_{10} and Q_{11} is another current mirror where $I_3 << I_4$ due to 5 kΩ emitter resistor. Consequently $I_Q = I_3$ is small (of the order of μA) giving a very high input resistance.

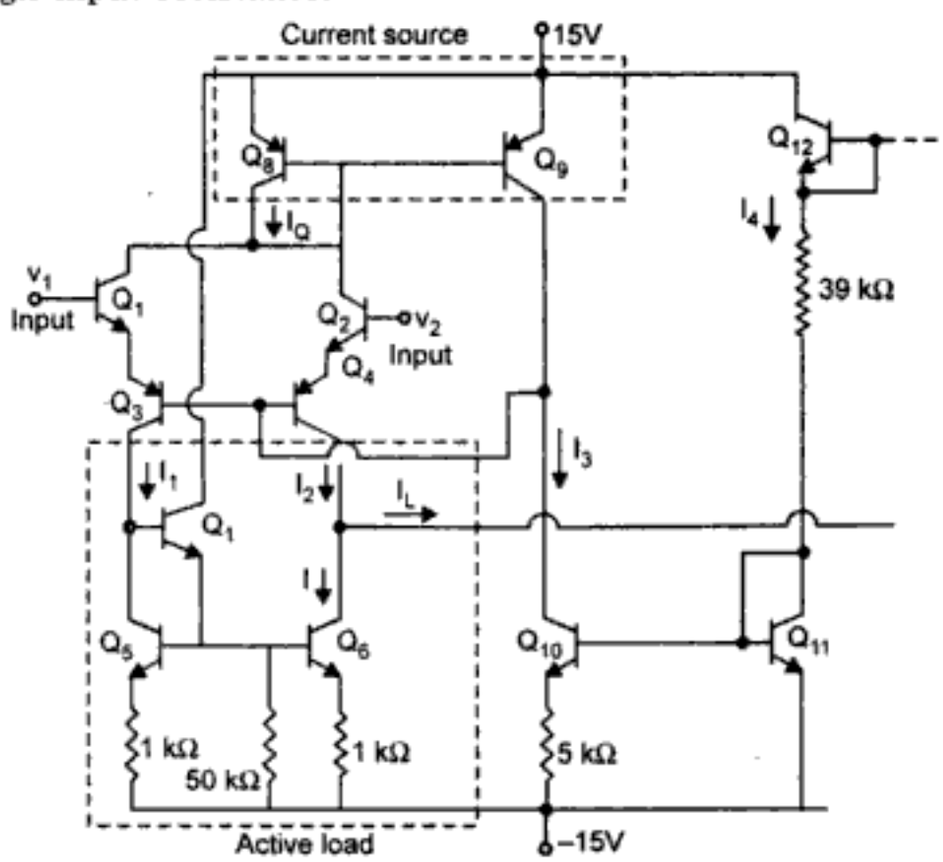


Fig. 2.29 (b) Active load ($Q_5 - Q_6 - Q_7$) of a low current differential amplifier μA741

Under the quiescent conditions, $I_1 = I_2 = I_Q/2$. Since I is always equal to I_1, the load current $I_L = I_2 - I = I_2 - I_1 = 0$. Now if v_1 is increased and v_2 is decreased, I_1 rises and I_2 falls from the quiescent value of $I_Q/2$. With this excitation, $I_L = I_2 - I_1$ changes from zero to a negative value. Thus the circuit behaves as a transconductance amplifier because I_L is proportional to $v_1 - v_2$.

2.4.7 Level Translator

There are two good reasons for using a level shifter in an IC op-amp. As we want an op-amp to operate down to dc, no coupling capacitor is used. Because of direct coupling, the dc level rises from stage to stage. The increase in dc level tends to shift the operating point of the

next stage. This, in turn, limits the output voltage swing and may even distort the output signal. It, therefore, becomes essential that the quiescent voltage of one stage is shifted before it is applied to the next stage. Another requirement to be satisfied is that the output should have quiescent voltage level of 0V for zero input signal.

The simplest type of a level shifter is shown in Fig. 2.30 (a). It may be noted that this is basically an emitter follower. Hence the level shifter also acts as a buffer to isolate the high gain stages from the output stage. The amount of shift obtained is

$$V_o - V_i = -V_{BE} \simeq -0.7 \text{ V} \tag{2.101}$$

If this shift is insufficient, the output can be taken at the junction of two resistors R_1 and R_2, as shown in Fig. 2.30 (b). The voltage shift is now increased by the drop across R_1. However, this arrangement has the disadvantage that signal voltage also gets attenuated by $R_2/(R_1 + R_2)$. This can be easily circumvented if R_2 is replaced by a current mirror I as shown in Fig. 2.30 (c). The shift in level now is

$$V_o - V_i = -(V_{BE} + I R_1) \tag{2.102}$$

and there is no ac attenuation due to high resistance of the current source.

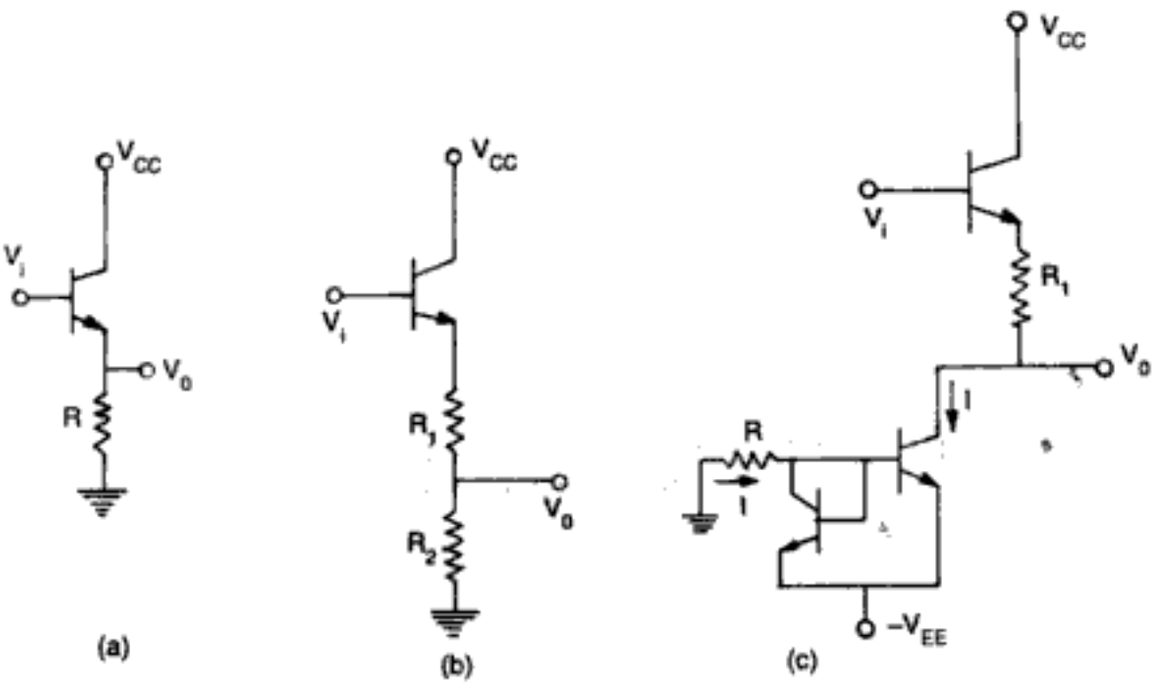


Fig. 2.30 (a)-(c) Level shifters using emitter follower buffer

Another voltage source commonly used in μA741 op-amp is shown in Fig. 2.30 (d). It can be seen that if base current is negligible compared to the current in R_3 and R_4, then the circuit behaves as a V_{BE} multiplier as,

$$V = \frac{V_{BE}}{R_4}(R_3 + R_4) = V_{BE}\left(1 + \frac{R_3}{R_4}\right)$$

This voltage source can also be used to replace R_1 in Fig. 2.30 (b).

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$$V_1 - V_2 = V_{BE3} + I_{C2} \times 5\ \text{k}\Omega$$
$$= 0.7\text{V} + 1.43 \times 5\ \text{k}\Omega = 7.85\ \text{V}.$$

2.4.8 Output Stage

The function of the last stage, that is, the output stage in an op-amp is to supply the load current and provide a low impedance output. A simple output stage is an emitter follower with complementary transistors as shown in Fig. 2.32 (a). It can be seen that for v_i positive, transistor Q_1 is ***on*** and supplies current to load R_L. And, if v_i is negative, Q_1 is cut off and Q_2 acts as a sink to remove current from the load R_L. There is, however, a limitation in this circuit. The output voltage v_o remains zero until the input v_i exceeds V_{BE} (cut in) = 0.5 *V*. This is called cross-over distortion. It can be eliminated by applying a bias voltage V slightly greater than 2 $V_{BE\,(\text{cut in})}$ = 1 V between the two bases, so that a small current flows in the transistors even in the quiescent state.

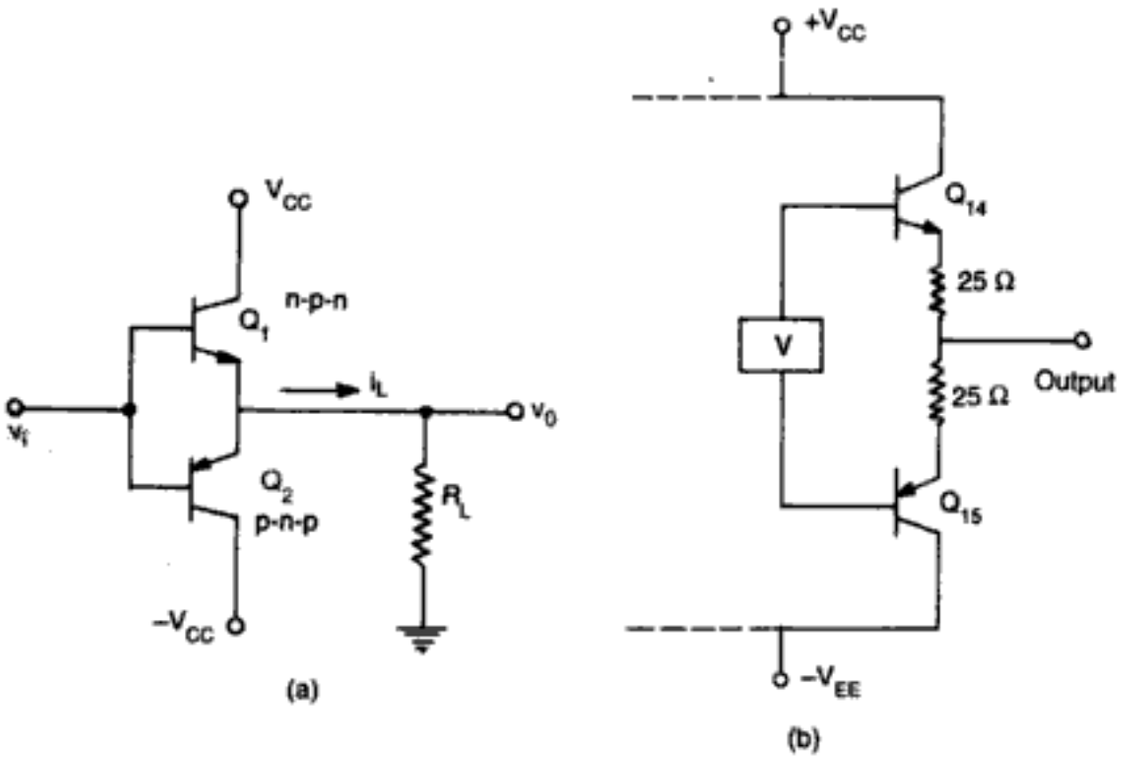

Fig. 2.32 (a) A complementary emitter follower output stage
(b) Output stage of μA 741

The output stage of μA 741 op-amp is shown in Fig. 2.32 (b). The block marked V is the V_{BE} multiplier of the type shown in Fig. 2.30 (d). It is designed to supply a voltage of about 1 V between the bases of the complementary pair of transistors Q_{14} and Q_{15}. The small emitter resistors (25Ω) stabilize the quiescent base current.

2.5 EXAMPLES OF IC OP-AMPS

We are now in a position to analyse the complete circuit of commercially available op-amps. Two such IC op-amps discussed are Motorola MC 1530 and Fairchild μA741.

2.5.1 Motorola MC1530 Op-Amp

The circuit of MC 1530 is shown in Fig. 2.33. It is easily seen that the circuit consists of four stages. Transistors Q_2 and Q_3 form the first diff-amp stage driven by the constant current source Q_1. The output of the first diff-amp drives the second diff-amp formed by Q_4 and Q_5. The single ended output of the second diff-amp drives the level shifter Q_6 (emitter follower). Q_7 and diode D_3 forms another constant current source of the type shown in Fig. 2.15. The diode connected transistor Q_1 of Fig. 2.15 is shown by diode D_3 here. The output stage of MC1530 uses Q_8, Q_9 and Q_{10} where Q_9 and Q_{10} are in totem-pole configuration.

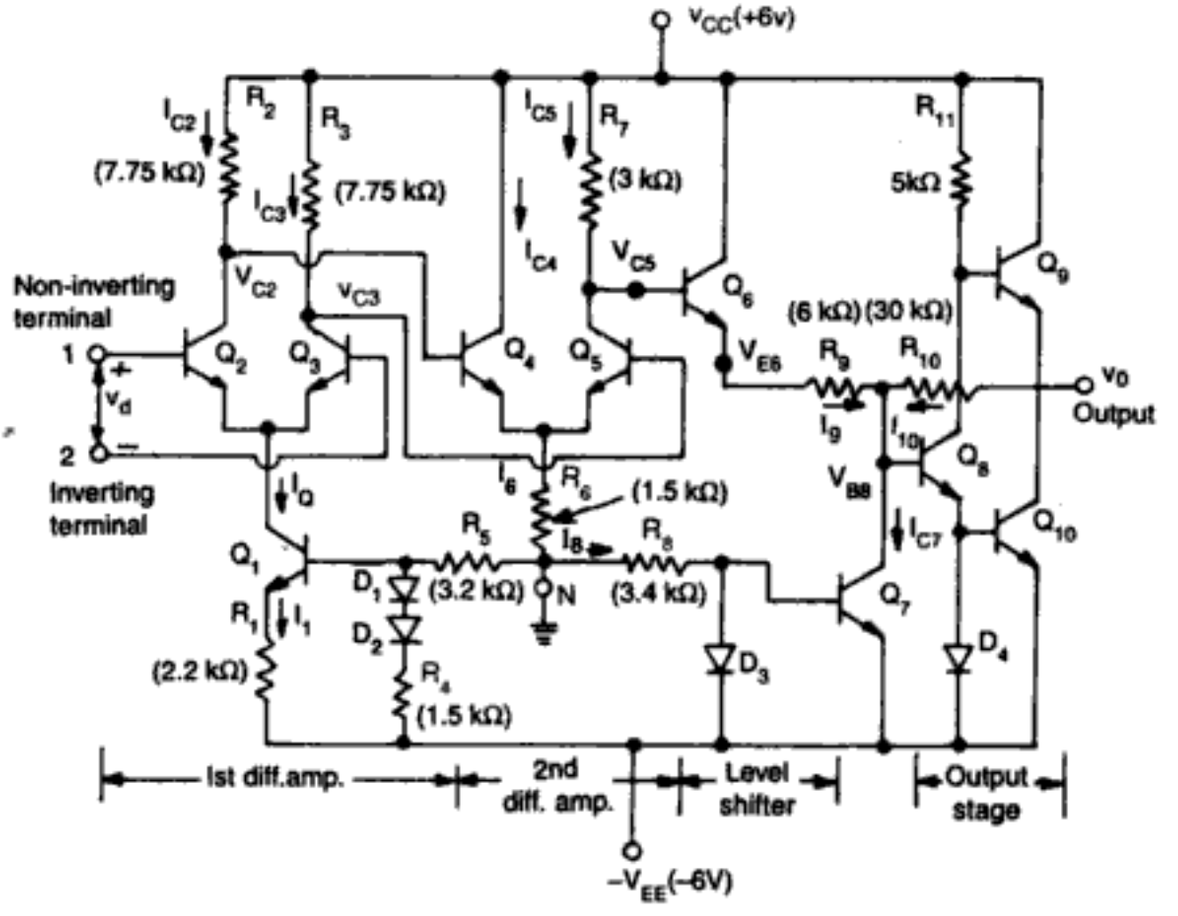

Fig. 2.33 Internal circuit of Motorola MC 1530

Example 2.13

From the circuit of Fig. 2.33 calculate,

(1) The collector current in each transistor and the output voltage under quiescent conditions.

(2) The open loop voltage gain.

Assume $h_{fe} = 100$ and $V_{BE} = V_D = 0.7\,V$

(1) The d.c. analysis is performed by assuming that both the inverting and non-inverting terminals are at ground potential. To determine the collector current in Q_2 and Q_3, first calculate the constant current I_Q. If the base current of Q_1 is neglected, then $I_Q = I_1$. The voltage V_{BN1} at the base of transistor Q_1 with respect to ground N is written using voltage divider rule as,

$$V_{BN1} = \frac{[-V_{EE} + V_D + V_D]\,R_5}{R_4 + R_5}$$

$$= \frac{(-6V + 1.4V)\,(3.2\,k\Omega)}{1.5\,k\Omega + 3.2\,k\Omega} = -3.13\,V$$

$$I_1 = \frac{V_{EE} + V_{BN1} - V_{BE1}}{R_1}$$

$$= \frac{6V - 3.13V - 0.7V}{2.2\,k\Omega} = 0.986\,mA$$

So $I_Q = 0.986$ mA

Under dc conditions, half of the I_Q flows through each of transistors Q_2 and Q_3. Therefore, $I_{C2} = I_{C3} = I_{Q2} = 0.493$ mA. The voltage at the collector of Q_2 and Q_3 is,

$$V_{C2} = V_{C3} = V_{CC} - R_2 I_{C2}$$

$$= 6V - (7.75\ k\Omega)\ (0.493\ mA) = 2.18\ V$$

So the voltage at the base if Q_4 and Q_5 is 2.18 V. The dc voltage at the emitter of Q_4 is,

$$V_{E4} = V_{C2} - V_{BE4} = 2.18V - 0.7V = 1.48\ V$$

So, $$I_6 = \frac{V_{E4}}{R_6} = \frac{1.48V}{1.5\,k\Omega} = 0.987\,mA$$

This current divides equally in transistors Q_4 and Q_5, so that

$$I_{C4} = I_{C5} = \frac{I_6}{2} = 0.494\,mA$$

$$V_{C5} = V_{CC} - I_{C5} R_7$$

$$= 6V - (0.494\ mA)\ (3\ k\Omega) = 4.52\ V$$

$$V_{E6} = V_{C5} - V_{BE6}$$

$$= 4.52V - 0.7V = 3.82\ V$$

Transistor Q_7 alongwith diode D_3 forms a current mirror of the type shown in Fig. 2.15. Hence,

$$I_{C7} = I_8 = \frac{V_{EE} - V_{D3}}{3.4} = 1.56 \text{ mA}$$

To calculate the current I_9, first calculate the voltage at the base of Q_8,

$$V_{B8} = V_{BE8} + V_{D4} - V_{EE}$$
$$= 0.7V + 0.7V - 6V = -4.60 \text{ V}$$

$$I_9 = \frac{V_{E6} - V_{B8}}{R_9} = \frac{3.82V + 4.6V}{6 \text{ k}\Omega}$$
$$= 1.40 \text{ mA}$$

$$I_{10} = I_{C7} - I_9 = 1.56 \text{ mA} - 1.40 \text{ mA} = 0.16 \text{ mA}$$

The voltage V_o at the output terminal is,

$$V_o = I_{10} R_{10} + V_{B8}$$
$$= (0.16 \text{ mA})\ (30 \text{ k}\Omega) - 4.60V = 0.20 \text{ V}$$
$$\approx 0 \text{ V (as expected)}$$

(2) In order to calculate the overall voltage gain, we first calculate the voltage gain of the differential amplifier stages. For this we must know the ac emitter resistance h_{ie} of the transistor used.

$$h_{ie} = \frac{h_{fe} V_T}{|I_C|}$$

where V_T is the volt equivalent of temperature = 26 mV at room temperature.

Since $I_{C2} = I_{C3} = I_{C4} = I_{C5} \approx 0.5 \text{ mA}$

So $$h_{ie} = \frac{(100)(26 \text{ mV})}{0.5 \text{ mA}} = 5.2 \text{ k}\Omega$$

Since emitter of $Q_4 - Q_5$ is at ground potential under ac operation the input resistance h_{ie} of Q_4 and Q_5 is effectively in parallel to collector circuit load (R_2 and R_3) of first diff-amp. The effective load of Q_2 and Q_3 is

$$R_{L2} = R_{L3} = 7.75 \text{ k}\Omega \| 5.2 \text{ k}\Omega$$
$$= 3.12 \text{ k}\Omega$$

The output of the first stage is double ended, its differential gain is given by Eq. (2.53) as

So, $$A_{V1} = \frac{(v_{C3} - v_{C2})}{v_d} = \frac{h_{fe} R_{L2}}{h_{ie}} = \frac{100 \times 3.12\ \text{k}\Omega}{5.2\ \text{k}\Omega} = 60$$

For the second stage, $h_{fe} = 100$, $h_{ie} = 5.2\ \text{k}\Omega$ and load $R_7 = 3\ \text{k}\Omega$ (neglecting loading on Q_5 of the emitter follower Q_6). The output of the second stage is single ended, so its differential gain is,

$$A_{V2} = \frac{v_{C5}}{v_{C3}} = -\frac{1}{2}\frac{h_{fe} R_7}{h_{ie}} = -\frac{100 \times 3\ \text{k}\Omega}{2 \times 5.2\ \text{k}\Omega} = -28.9$$

The third stage is the emitter follower, so, $A_{V3} \simeq 1$

The last output stage uses voltage shunt feedback network $R_9 - R_{10}$,

so $$A_{V4} \simeq \frac{R_{10}}{R_9} = -\frac{30}{6} = -5$$

Hence the overall op-amp gain is,

$$A_v = (60)\ (-28.9)\ (-5) = 8670$$

2.5.2 741 Op-Amp

741 op-amp has become an industry standard today. The pin configuration and the complete schematic circuit diagram for 741 is shown in Fig. 2.34 (a) and (b) respectively. Since this circuit is quite complex compared to MC1530, only the qualitative analysis is taken up.

In understanding an op-amp circuit as complex as this (20 transistors), first we identify the stages which provide signal gain. The input stage diff-amp consists of transistors $Q_1 - Q_3$ and $Q_2 - Q_4$. Transistors Q_{16} and Q_{17} provide the second stage voltage gain. Transistors Q_1Q_3 and Q_2Q_4 are in cascode (CE-CB) configuration. Two transistors in series (Q_1 feeds Q_3) provide high gain per stage needed to achieve the adequate open-loop gain in a two stage amplifier. The transistors Q_5, Q_6 and Q_7 form the active load for Q_3 and Q_4. Transistors Q_5 and Q_6 also function as a differential amplifier for the external offset nulling signal. The emitter current of transistors Q_5 and Q_6 can be

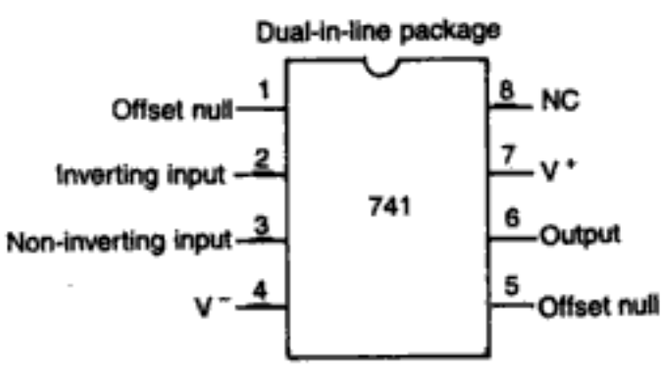

Fig. 2.34 (a) Pin configuration

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controlled by varying a 10 kΩ potentiometer that is externally connected between offset null terminals as shown by dotted line in Fig. 2.34(b). Bias currents for the input stage are provided by a complicated arrangement of current mirror pairs. Q_{12} generates a current in Q_{11}. This current is reflected over to Q_{10} (though reduced because of the emitter feedback due to R_4). This, in turn, generates a series current in Q_9 which is reflected across another mirror pair to Q_8. The bias current of Q_3 and Q_4 is effectively driven by the mirror pair Q_{10} and Q_{11}. The output of the first diff-amp is taken at the junction of Q_4 and Q_6 (point X) which acts as a complementary symmetry amplifier. The output at this point is proportional to the differential input signal. The output is now amplified by the second stage consisting of transistor Q_{16} and Q_{17} in Darlington connection.

The output of common-collector-amplifier formed by Q_{16} and R_9 drives the CE-amplifier composed of Q_{17}, R_8 and a constant current load Q_{13}. The output of CE-amplifier is a bias source for transistors Q_{18} and Q_{19}. Transistors Q_{12} and Q_{13} form a current mirror and supply current to transistors Q_{17}, Q_{18} and Q_{19}. The network consisting of transistors Q_{18}, Q_{19} and R_{10} is a fixed voltage level shifter shifting the voltage output of Q_{17} by a fixed amount on its way to the output complementary stage formed by Q_{14} and Q_{20}. The level shifter network is designed to bias the output stage in the linear region. The transistors Q_{18} and Q_{19} also separate the bases of Q_{14} and Q_{20} by two diode drops and thus temperature compensate currents in Q_{14} and Q_{20}. Transistor Q_{22} performs two functions. It serves as a buffer between Q_{17} and Q_{20} and also provides a negative feedback to Q_{16}. The final output is taken at the junction of R_6 and R_7. The output complementary pair operates so that depending upon the sign of the output, only one of the transistors Q_{14} or Q_{20} is conducting at any time. With no input signal, both devices are turned off, resulting in a low quiescent current drain in the output stage.

Transistors Q_{15}, Q_{21} and Q_{23} protect the circuit by limiting current to the output complementary stage. If the output (load) current exceeds the safe limit, the voltage drop across R_6 and R_7 increases. This turns on Q_{15} and Q_{21} which in turn makes Q_{23} on. This however shorts out, that is turns off the amplifier Q_{16}–Q_{17}. This reduces the emitter current in Q_{22} and in turn current in Q_{18} and Q_{19}. The reduction in the currents of Q_{18} and Q_{19} lowers the currents in Q_{14} and Q_{20}. The diode-connected transistor Q_{24} is a temperature compensating diode for transistor Q_{23}. Finally the internal 30-pF capacitor provides the high frequency roll-off to stabilize the circuit.

Example 2.14

For the op-amp circuit shown in Fig. 2.35

(1) Perform the dc analysis. Assume $\beta = 100$, $V_{BE} = 0.7$V. Note that the transistor Q_7 has four times the areas of transistors Q_3 and Q_4.
(2) Compute the overall voltage gain.

Solution

It can be seen that the circuit has the following four stages:

(i) Dual-input, differential-output
(ii) Dual-input, single-ended output
(iii) Level translater
(iv) Emitter follower

(1) For dc analysis, assume that the input terminals are shorted to ground.
The reference current I of the current minor $Q_3 - Q_4$ is obtained as

$$I = \frac{V_{EE} - V_{BE3}}{R}$$

$$= \frac{15\text{V} - 0.7\text{V}}{28.6\ \text{k}\Omega} = 0.5\ \text{mA}$$

Due to current mirror action,

$$I_{CQ4} = I = 0.5\ \text{mA}$$

and $$I_{CQ1} = I_{CQ2} = I_{CQ4}/2 = 0.25\ \text{mA}$$

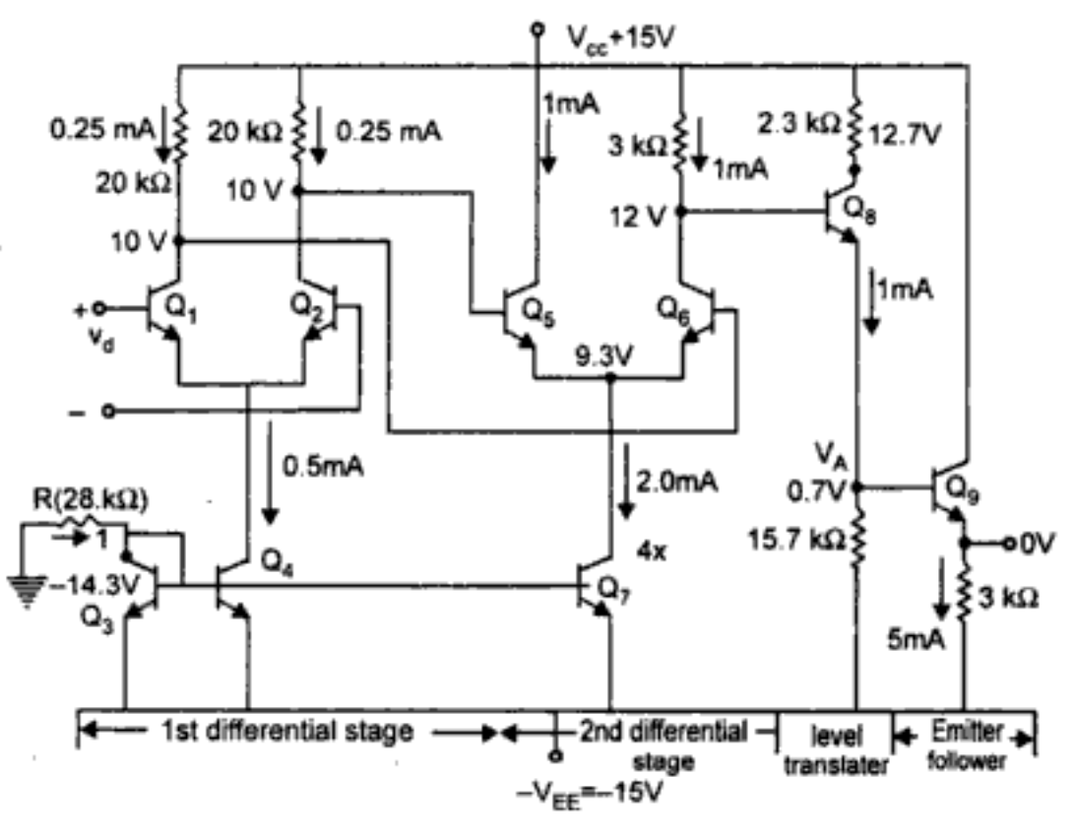

Fig. 2.35 Circuit for Example 2.14

Thus, each of Q_1 and Q_2 are biased at 0.25 mA. The collector voltages for Q_1 and Q_2 are

$$V_{CQ1} = V_{CQ2} = V_{CC} - I_{C1}R_{C1}$$

$$= 15\text{V} - 0.25\ \text{mA} \times 20\ \text{k}\Omega$$

$$= +\ 10\ \text{V}$$

Now, proceeding to the next differential stage, voltage at the emitter of Q_5 and Q_6 will be

$$V_{EQ5} = V_{EQ6} = 10\,V - 0.7\,V$$
$$= 9.3\ V$$

The differential pair $Q_5 - Q_6$ is biased by the current mirror transistor Q_7. Since the area of Q_7 is 4 times that of Q_3 and Q_4, the transistor Q_7 supplies a current $4 \times 0.5 = 2$ mA.

Thus, collector currents of Q_5 and Q_6 are

$$I_{CQ5} = I_{CQ6} = \frac{I_{CQ7}}{2} = 1\ mA$$

Hence, collector voltage of Q_6 is

$$V_{CQ6} = V_{CC} - I_{CQ6}R_{C6}$$
$$= 15\,V - 1mA \times 3\,k\Omega$$
$$= 12\ V$$

This causes a voltage at the emitter of *pnp* transistor Q_8 at

$$V_{EQ8} = 12.7\ V$$

The emitter current of Q_8 is

$$I_{EQ8} = \frac{15\,V - 12.7\,V}{2.3\,k\Omega} = 1\ mA$$

The voltage V_A at the collector of Q_8 or the base of Q_9 is

$$V_A = -15\,V + 1\ mA \times 15.7\,k\Omega$$
$$= 0.7\ V$$

Since the emitter of Q_9 will be 0.7 V below the base terminal, the voltage at the output terminal 6 is 0 V as is expected. The emitter current of Q_9 is

$$I_{EQ9} = [0 - (-15V)] / 3k\Omega$$
$$= 5\ mA$$

(2) A.C. Analysis. The ac emitter resistance of the transistor $Q_1 - Q_2$ is

$$h_{ie_{(Q_1 - Q_2)}} = \frac{h_{fe}V_T}{|I_C|} = \frac{100 \times 25\ mV}{.25\ mA} = 10\,k\Omega$$

The ac emitter resistance of transistor $Q_5 - Q_6$ is

$$h_{ie_{(Q_5 - Q_6)}} = \frac{100 \times 25\ mV}{1\ mA} = 2.5\,k\Omega$$

Since emitter of $(Q_5 - Q_6)$ is at ground potential under ac conditions, the effective load for $Q_1 - Q_2$ is

$$R_{L1} = R_{L2} = 20\,\text{k}\Omega \,\|\, 2.5\,\text{k}\Omega$$
$$= 2.2\ \text{k}\Omega$$

Voltage gain of the first differential stage is

$$A_{DM1} = \frac{h_{fe} R_{L2}}{h_{ie}} = \frac{100 \times 2.2\,\text{k}\Omega}{10\,\text{k}\Omega} = 22$$

Voltage gain of second stage which is differential input, single-ended is

$$A_{DM2} = -\frac{1}{2}\,\frac{h_{fe} R_{L6}}{h_{ie}}$$

Assuming no loading effect on this stage due to level translator stage,

$$A_{DM2} = -\frac{1}{2} \times \frac{100 \times 3\,\text{k}\Omega}{2.5\ \text{k}\Omega} = -60$$

The gain of the level translator stage is

$$A_3 \cong -\frac{R_L}{R_E} = -\frac{15.7\,\text{k}\Omega}{2.3\,\text{k}\Omega} = -6.82$$

The last stage is emitter follower, so its voltage gain $A_{V4} \cong 1$

So the overall voltage gain is

$$A_V = (22)\ (-60)\ (-6.82)\ (1)$$
$$= 9002$$

2.6 FET OPERATIONAL AMPLIFIER

The op-amp circuits discussed so far are bipolar op-amps. Op-amps using field transistors (FETs) in the input stage offer some very significant advantages over bipolar op-amps, especially in areas as input impedance, input bias and offset currents and slewing rate as shown in Table 2.1.

Table 2.1

Parameter	BJT	JFET	MOSFET
Input resistance	kΩ	$10^9\Omega$ (gigaohms)	$10^{12}\Omega$ (teraohms)
Input gate current	μA	1 nA	1 pA
Input offset current	20 nA	2 pA	0.5 pA
Slewing rate	1 V/μs	3 V/μs	10 V/μs

It is now possible to fabricate JFET/MOSFET and BJTs on the same chip using ion implantation techniques. Op-amps which use FET input stages and BJT for the remaining stages are termed as BIFET/BIMOS. By the mid 1980s, BIMOS circuits were produced commercially. Some of the FET IC op-amps available are discussed here briefly.

JFET Op-amps

An example of a FET input hybrid op-amp is the LH0022/42/52 (National semiconductor) series. This op-amp uses a pair of JFET transistors only for the input-stage differential amplifier and the rest of the circuit uses bipolar transistors. A simplified diagram of this op-amp is shown in Fig. 2.35. The input-stage differential amplifier consists of Q_1 through Q_4 in which Q_1 and Q_2 are n-channel JFETs operating in a common-drain or source-follower configuration. These JFETs drive Q_3 and Q_4 which operate in the common-base configuration. Thus the differential amplifier uses a compound JFET/bipolar transistor configuration. This provides very high input resistance and very low input current characteristics of JFETs and high-voltage gain that is obtainable from bipolar transistors. This compound differential amplifier drives an active load consisting of Q_5 through Q_7, operating as a current mirror. The rest of this op-amp is of conventional design as discussed for μA741. Here diodes D_1 and D_2 are used to provide a pre-bias across Q_{14} and Q_{20} to minimize cross-over distortion.

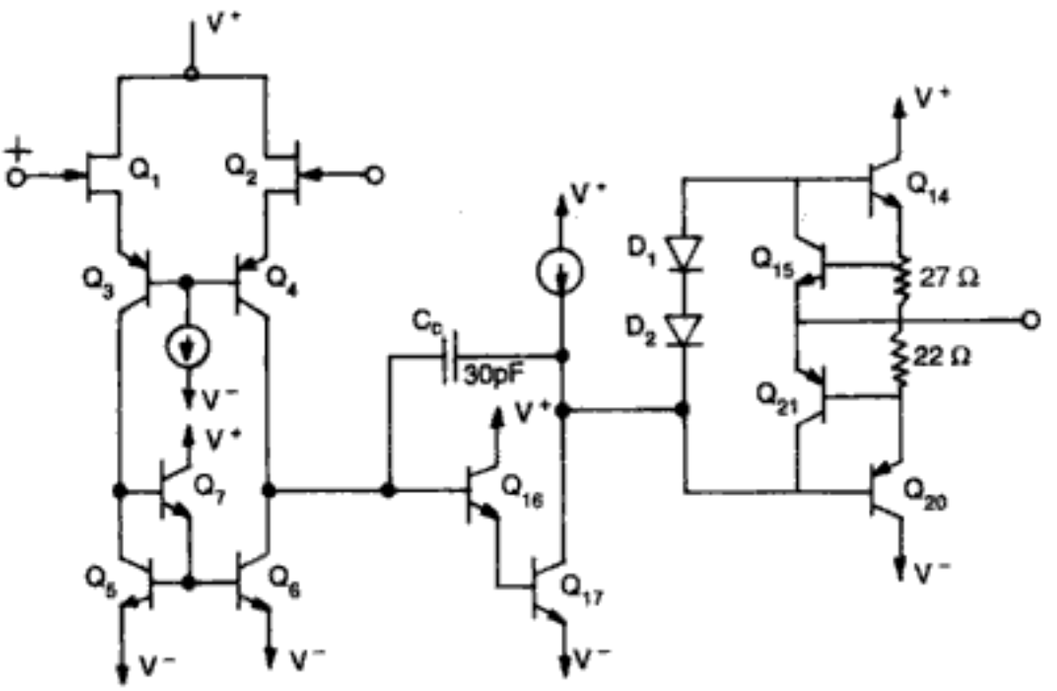

Fig. 2.35 Hybrid JFET-imput op-amp LHOO 22/42/52 series (National Semiconductor)

MOSFET Op-Amps

An interesting example of a monolithic MOSFET op-amp is the CA3130 (RCA) which contains both MOSFETs and bipolar transistors on the same chip. A simplified schematic diagram of this device is shown in Fig. 2.36.

The input stage is a differential amplifier consisting of a pair of p-channel enhancement-mode MOSFETs Q_6 and Q_7. This differential amplifier is biased by a 200 μA MOSFET current source, and it drives a current mirror active load using Q_9 and Q_{10}. Resistors R_5 and R_6 (1 kΩ) in the active load circuit are used together with an externally connected potentiometer (across pins 1 and 5) for offset voltage nulling. The quiescent voltage drop across these resistors in 100 μA × 1 kΩ = 100 mV, so that a ± 100 mV offset adjustment range is available. Diodes D_5 and D_8 are connected between the input terminal to protect the thin gate oxide of the input MOSFETs against excessive voltage spikes and static electricity discharge, which could cause breakdown of the oxide layer and result in irreversible damage to the transistors. The voltage gain of this first stage is only about 5, due to low transfer conductance of the MOSFETs.

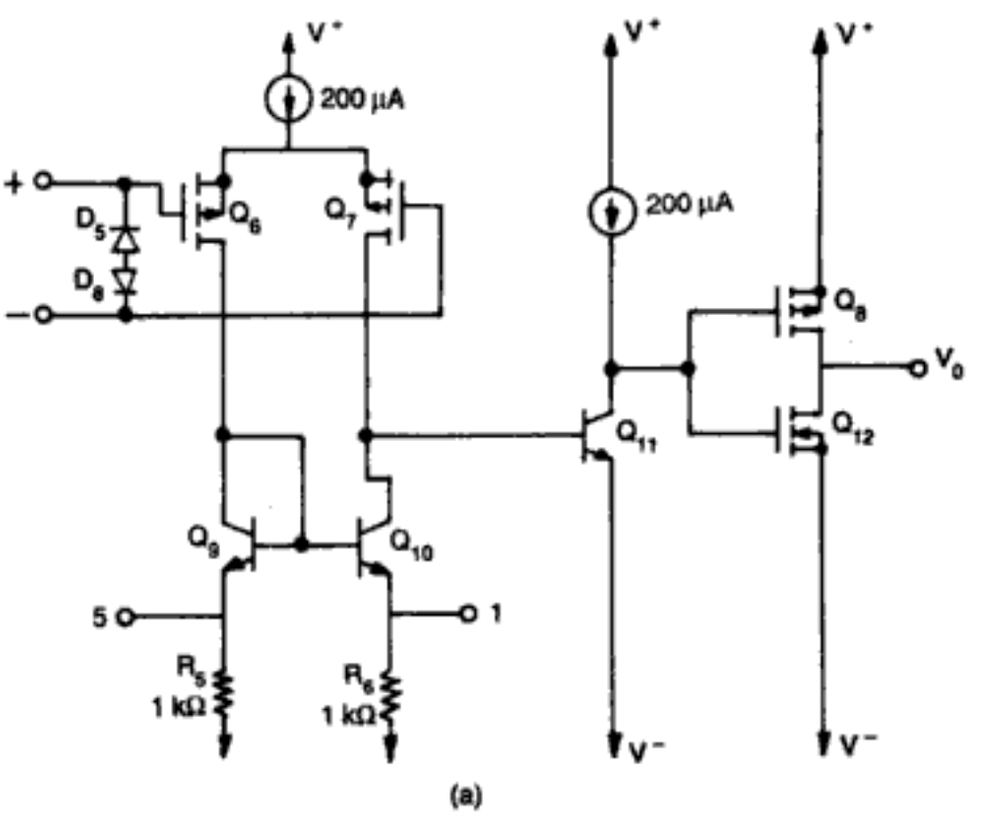

Fig. 2.36 MOSFET-input CMOS output op-amp: CH3130 (RCA Corporation) a simplified schematic diagram

The second stage consists of a bipolar transistor Q_{11} connected as a common-emitter amplifier, with a 200 μA MOSFET current source serving as the active load. As a result of the high dynamic impedance

seen looking into the MOSFET output stage, the voltage gain of the second stage is very large (≃ 6000). The output stage is a complementary pair of MOSFETs (CMOS) with Q_8 being the PMOS and Q_{12} being the NMOS transistor. The use of CMOS pair in the output stage provides significantly low drainage of current from the power supply.

Summary

1. An op-amp is available in three types of IC packages: metal can, dual-in-line and flat pack.
2. There are five basic terminals: two input terminals, one output terminal and two supply terminals.
3. In open loop mode, the output of the op-amp is at positive or negative saturation level. It does not operate linearly in this mode.
4. Negative feedback stabilizes the gain. Two feedback connections used are: inverting amplifier and non-inverting amplifier.
5. A special case of non-inverting amplifier is the voltage follower.
6. A differential amplifier amplifies the difference between two input signals.
7. An operational amplifier is a direct coupled high gain amplifier consisting of one or more differential amplifiers, followed by a level translator and an output stage.
8. For proper operation of the differential amplifier, matched components must be used. The diff-amp can be biased by using emitter bias (a combination of R_E and V_{EE}), a constant current bias or a current mirror.
9. A current mirror can be used as an active load because it has high ac resistance.
10. MOSFET op-amps offer very high input resistance (10^{12} Ω), low input current (~ 1pA) and high slewing rate (~ 10V/μs).

Review Questions

2.1. What is an op-amp?
2.2. What are the different linear IC packages?
2.3. A 741 op-amp is available in a 14-pin dual-in-line package. What is the terminal number for (i) inverting input (ii) non-inverting input (iii) output?
2.4. Explain with figures how two supply voltages V^+ and V^- are obtained from a single supply.
2.5. List six characteristics of an ideal op-amp.
2.6. Explain the meaning of open loop and closed loop operation of an op-amp.
2.7. Name the type of the feedback used if an external component is connected between the output terminal and the inverting input.

2.8. What is the input impedance of a non-inverting op-amp amplifier?
2.9. If the open loop gain of an op-amp is very large, does the closed loop gain depend upon the external components or the op-amp?
2.10. What is a practical op-amp? Draw its equivalent circuit.
2.11. Define common mode rejection ratio.
2.12. Explain why CMRR $\rightarrow \infty$ for an emitter coupled differential amplifier when $R_E \rightarrow \infty$.
2.13. Why is R_E replaced by a constant current bias circuit in a diff-amp?
2.14. List and explain the function of all the basic building blocks of an op-amp.
2.15. Explain methods for increasing the input resistance of an op-amp.
2.16. Explain the difference between constant current bias and current mirror.
2.17. Explain why active load is used?
2.18. What is a V_{BE} multiplier?
2.19. What is cross-over distortion and how it is eliminated?
2.20. Why is cascode configuration used in an op-amp?
2.21. Why are FET op-amps better than BJT op-amps?
2.22. What is meant by a BIMOS or BIFET amplifier?

PROBLEMS

2.1. In an op-amp of Fig. 2.4 (a), $v_2 = 0$. What must be the voltage at v_1 to give an output of 5 V if $A_{OL} = 50000$.
2.2. Design an inverting amplifier with a gain of – 5 and and an input resistance of 10 kΩ.
2.3. Design a non-inverting amplifier with a gain of 10.
2.4. For the circuit shown in Fig. P. 2.4, calculate the range of gain and input impedance.

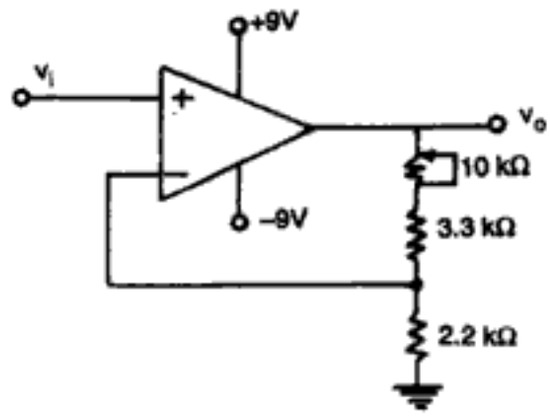

Fig. P. 2.4

2.5. Calculate the exact closed loop gain of the inverting amplifier of Fig. 2.5 (b) if $A_{OL} = 200{,}000$, $R_i = 2$ MΩ and $R_o = 75\Omega$.

2.6. For the circuit shown in Fig. P. 2.6, calculate the expression of v_o/v_i.

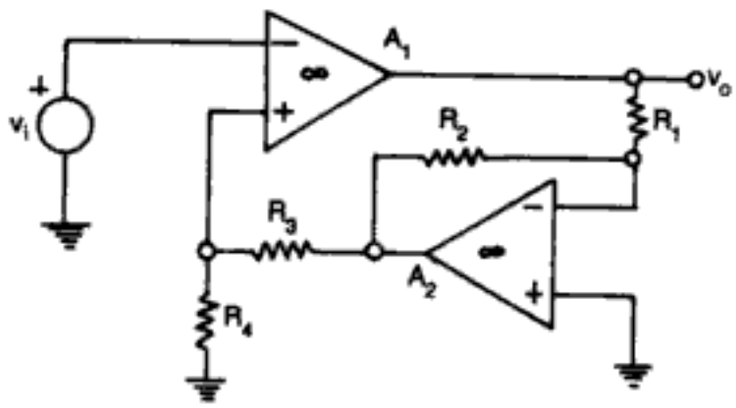

Fig. P. 2.6

2.7. In the circuit of Fig. P. 2.7 if $R_i = \infty$ show that the output admitance Y_{of} is given by

$$Y_{of} = \frac{1}{R_o}\left(1 - A_{OL}\frac{R}{R+R'}\right) + \frac{1}{R+R'}$$

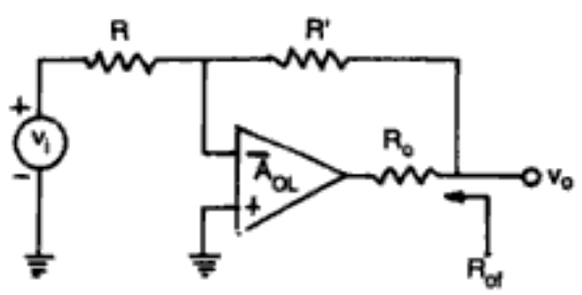

Fig. P. 2.7

2.8. Show that the input impedance for the non-inverting amp of Fig. P. 2.8 is

$$R_{if} = R_i\left(1 + \frac{Z_1}{Z_1 + Z_f} \cdot A_v\right)$$

where R_i the input resistance of op-amp is large and $R_o = 0$ and A_v is the gain without feedback.

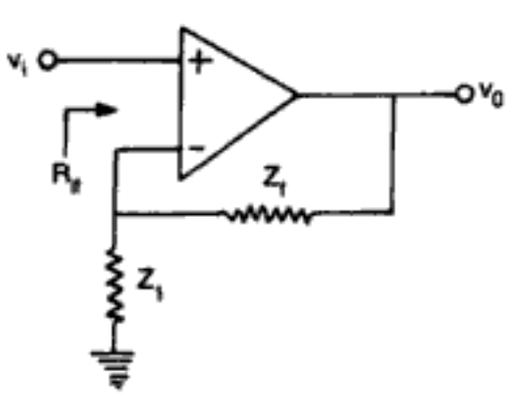

Fig. P. 2.8

2.9. Refer to Fig. P. 2.9

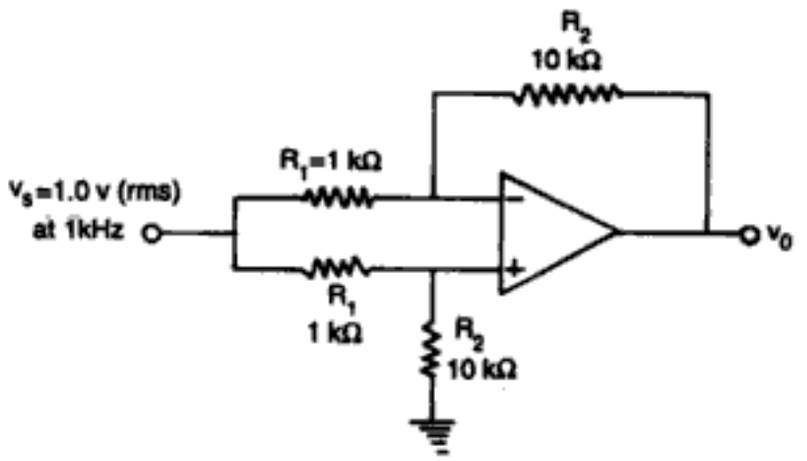

Fig. P. 2.9

(a) Find v_o if CMRR = 100 dB at 1kHz.
(b) Find v_o resulting from 1% mismatches between the two R_1 resistors.
(c) Find v_o resulting from 1% mismatch between two R_2 resistors.

2.10. Derive the expression for the output voltage v_o for the circuit shown in Fig. P. 2.10.

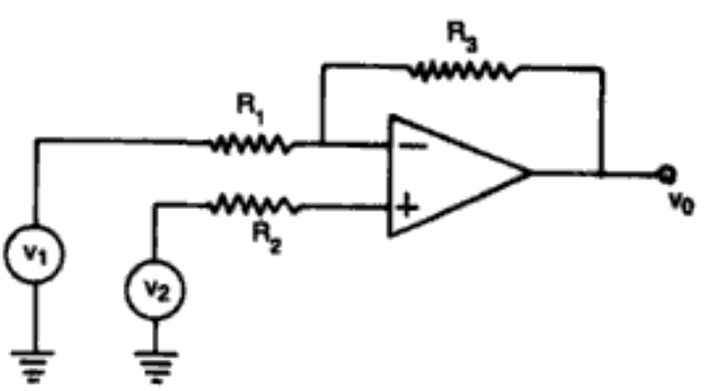

Fig. P. 2.10

2.11. Calculate the output voltage of the circuit in Fig. P. 2.11 if the input signal is a 5.5 mA current.

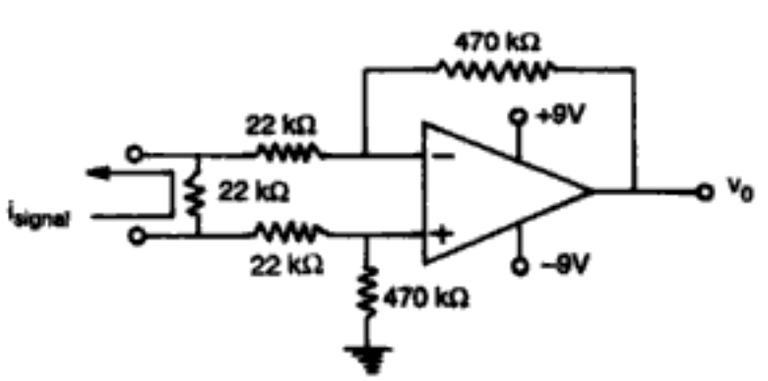

Fig. P. 2.11

2.12. What is the voltage at point A and B for the circuit shown in Fig. P. 2.12 if v_1 = 5 V and v_2 = 5.1 V.

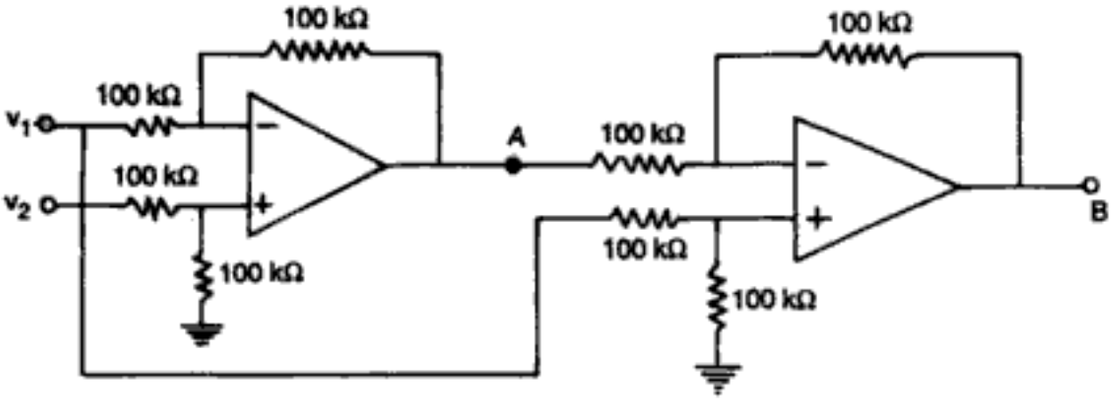

Fig. P. 212

2.13. For op-amp, CMRR = 10^5 and differential gain A_{DM} = 10^5. Calculate the common mode gain A_{CM} of the op-amp.

2.14. The CMRR of an op-amp is 10^4. Two sets of signals are applied to it. First set is V_1 = + 20 μV and V_2 = – 20 μV and second set is V_1 = 540 μV and V_2 = 500 μV. Calculate the percent difference in output voltage for the two sets of signals.

2.15. For the current mirror shown in Fig. P. 2.15, determine R so that I_o = 100 μA.

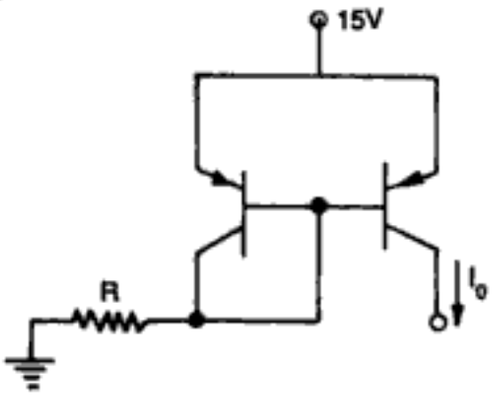

Fig. P. 2.15

2.16. In the circuit of Fig. P. 2.16, I_R = 50 μA, what is the ratio R_1/R_2 needed for I_o = 100 μA?

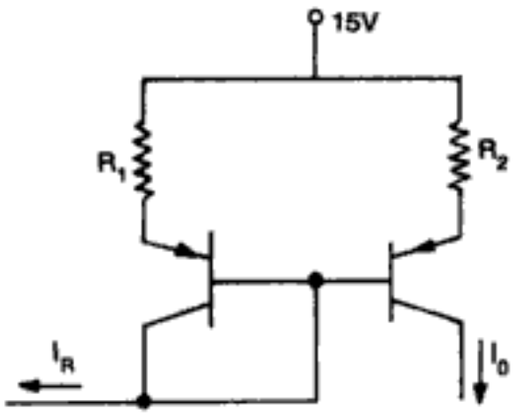

Fig. P. 2.16

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Procedure

(1) Connect the op-amp as an inverting amplifier as shown in Fig. E. 2.1 (a)

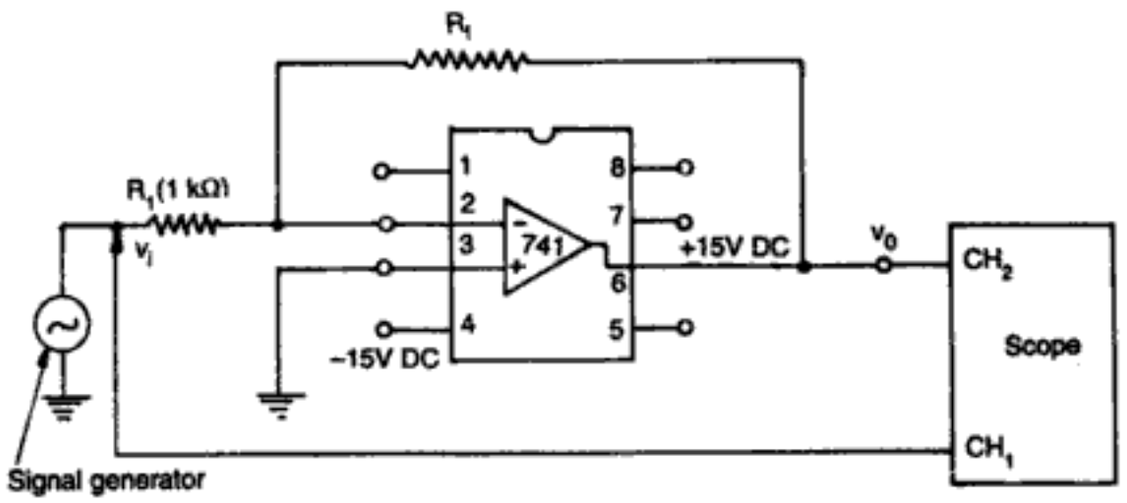

Fig. E. 2.1 (a) Inverting amplifier

(2) Connect a dual channel scope to simultaneously view v_0 and v_i. Adjust the signal generator to give 200 mV peak to peak sine wave at 100 Hz. Then measure and record the peak value of v_0 for R_f: 1 kΩ, 10 kΩ, 33 kΩ and 100 kΩ. Note the phase of v_0 with respect to v_i.

(3) Calculate the theoretical closed loop gain = R_f/R_1 for each value of R_f and compare it with the experimental value of v_0/v_i.

(4) Now connect the op-amp as a non-inverting amplifier as shown in Fig. E. 2.1 (b)

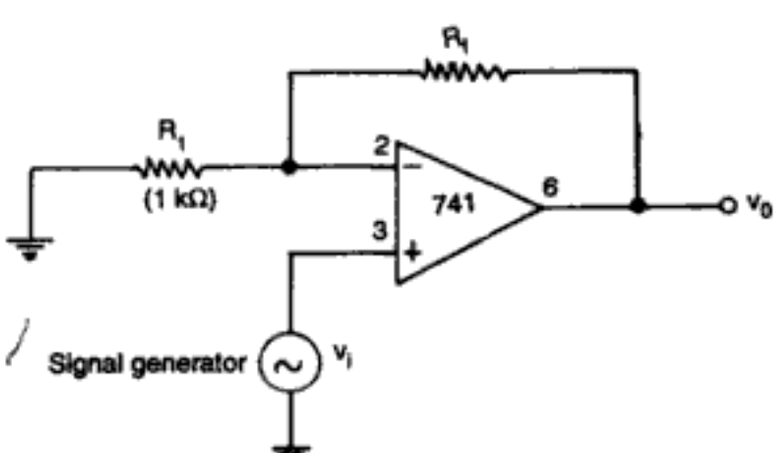

Fig. E. 2.1 (b) Non-inverting amplifier

(5) Repeat step 2.

(6) Calculate the theoretical gain = 1 + R_f/R_1 for each value of R_f and compare it with the experimental value of v_0/v_i.

(7) Next make a voltage follower circuit as shown in Fig. E. 2.1. (c)

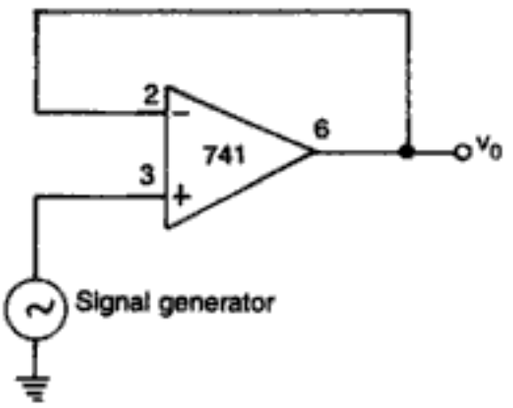

Fig. E. 2.1 (c) Voltage follower

(8) Measure and record the output voltage v_0 for different input settings: 2 V peak at 100 Hz, 1 V peak at 500 Hz and 5 V peak at 1 kHz. Note the phase of v_0 with respect to v_i in each case.
(9) Verify that the voltage gain of the voltage follower is always equal to 1.

COMPUTER ANALYSIS

Program 2.1

Inverting Op-Amp Amplifier

Fig C 2.1(a) shows an inverting op-amp amplifier with various terminals numbered for writing the PSPICE program. The PSPICE description is provided in program 2.1 listing. For circuit values of R_1 = 1 kΩ, R_f = 10 kΩ, the gain of the inverting amplifier is

$$A_V = -\frac{R_f}{R_1} = -10$$

D.C. Analysis

For input V_1 = 1 V, the output voltage V_0 should V_0 = – 10 (1V) = – 10 V.
From the result file, it can be seen that the output V_0 at node 5 is – 9.998 V which gives an error or 0.02% only.

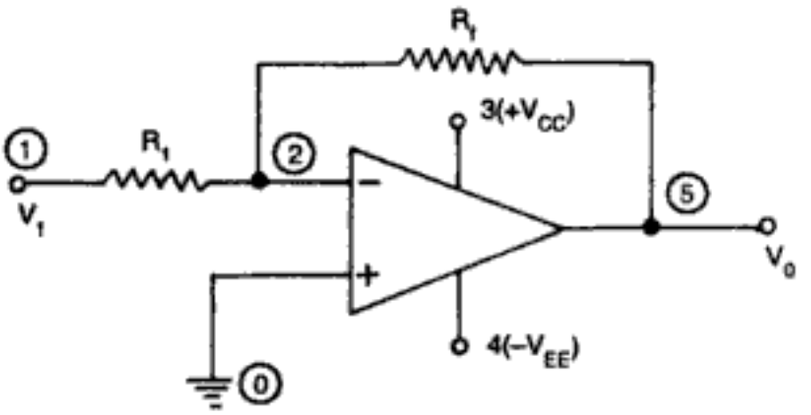

Fig. C 2.1 (a) Circuit for program 2.1

Transient Analysis

A sine wave signal of amplitude 0.1 V and frequency 1 kHz is applied at the input terminal. It can be seen from Fig. C 2.1 (b) that the output is a sine wave of amplitude 1 V, 1 kHz. The output waveform is 180° out of the phase with the input waveform as expected.

Program 2.1: Listing

Inverting Amplifier: DC and Transient (Output Voltage vs Time) Analysis

```
  * * * * Circuit Description
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
* * *
    R1 1 2 IK
    RF 2 5 10K
*   Op Amp Analysis
    X1 0 2 3 4 5 µA 741
    . LIB EVAL. LIB
*   Power Supplies
    VCC 3 0 DC 12V
    VEE 0 4 DC 12V
*   Input Signal  Source
    V1 1 0 DC 1V SIN(0  0.1V  1KHZ)
*   Output
    .DC V1  1  1  1
    .TRAN . 5us 5ms 0ms .01 ms
    .PROBE
    .PRINT DC V(5) V(1)
    .END
```

```
  * * * * DC Transfer Curves                    Temperature = 27.000 DEG C
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
* * *
    V1              V(5)            V(1)
    1.000E+00       -9.998E+00      1.000E+00
```

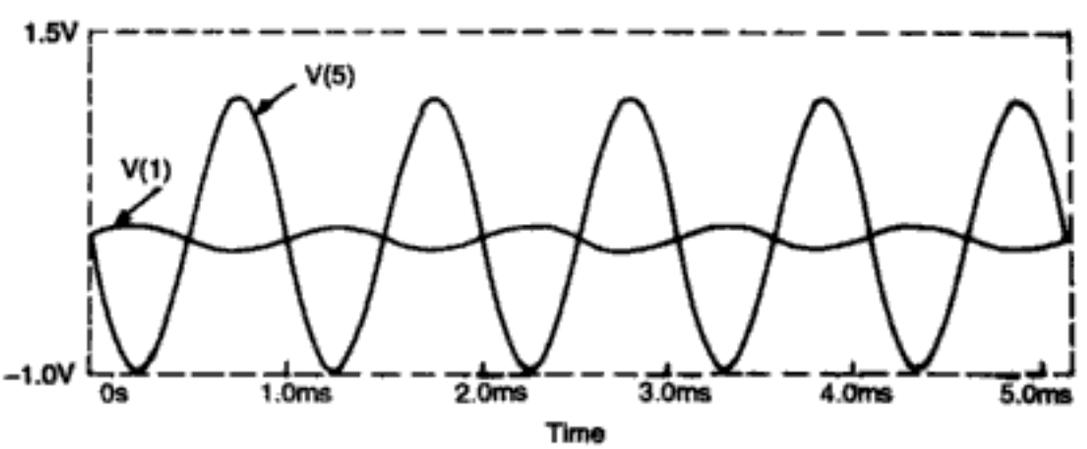

Fig. C 2.1 (b) Inverting Amplifier: Transient Analysis (Output Voltage Vs Time)

Program 2.2

Non-inverting op-amp Amplifier

The circuit of a non-inverting op-amp amplifier for writing the PSPICE program is shown in Fig. C 2.2 (a).

For the circuit values, R_1 = 1 kΩ and R_f = 9 kΩ, the voltage gain is

$$A_V = 1 + \frac{R_f}{R_1} = 1 + \frac{9\text{k}\Omega}{1\text{k}\Omega} = +10$$

$$= 10$$

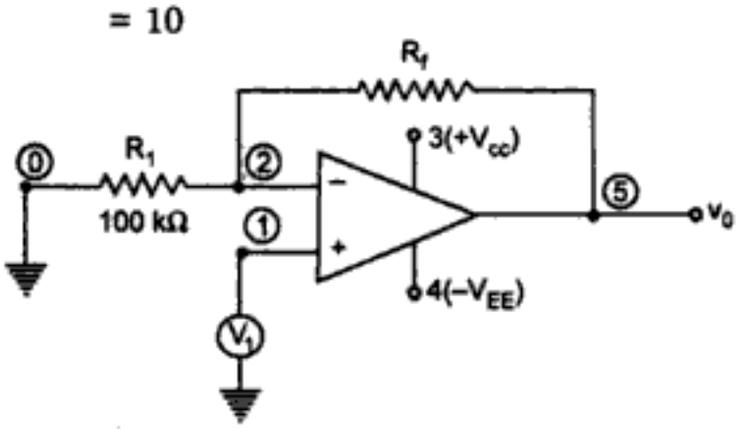

Fig. C 2.2 (a) Circuit for Program 2.2

D.C. Analysis

For input voltage V_1 = 1V, the output voltage at node 5, V(5) = 10V

Transient Analysis

For input voltage source of amplitude 0.1 V and frequency 1 kHz, the output voltage has an amplitude 1 V at 1 kHz as shown in Fig. C 2.2 (b). It may be noted that there is no phase shift for a non-inverting amplifier.

Program 2.2 Listing

Non-inverting Amplifier: DC and Transient (Output Voltage vs Time) Analysis

```
  * * * * Circuit Description
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
* * *
   R1  0  2  IK
   RF  2  5  9K
*  Op Amp Analysis
   X1  1  2  3  4  5  µA741
   . LIB  EVAL.LIB
*  Power Supplies
   VCC  3  0  DC  12V
   VEE  0  4  DC  12V
```

```
*   Input Signal Source
    V1  1  0  DC  1V  SIN (0 0.1V 1 KHZ)
*   Output
    .DC  V1  1  1  1
    .TRAN . 5us 5ms 0ms 0.01 ms
    .PRINT  DC  V(5)  V(1)
    .PROBE

  * * * *       DC Transfer Curves              Temperature = 27.000 DEG C
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *

* * *
        V1                          V(5)                        V(1)
    1.000E+00                   1.000E+01                   1.000E+00
```

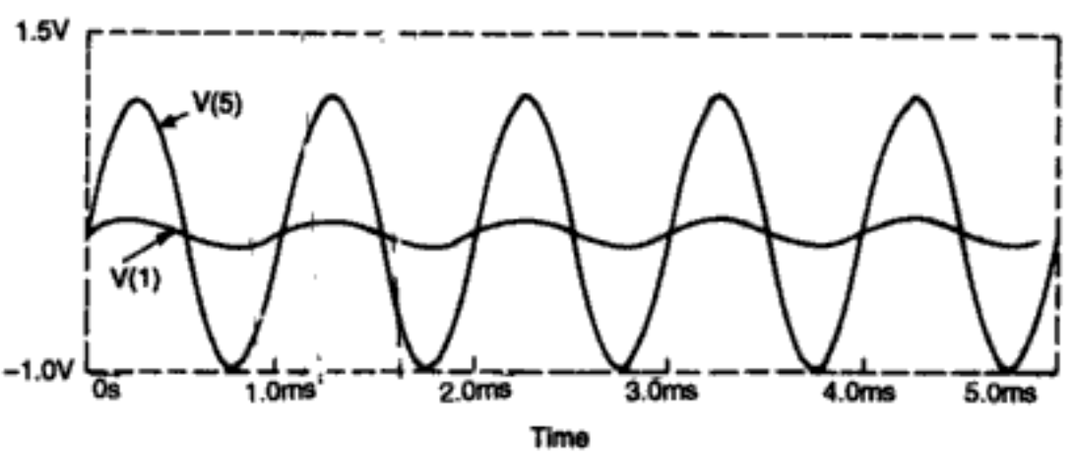

Fig. C 2.2 (b) Non-Inverting Amplifier: Transient Analysis (Output Voltage Vs Time)

Program 2.3 Voltage Follower

The circuit diagram of a voltage follower and its PSPICE description are shown in Fig. C 2.3(a) and program 2.3 listing respectively.

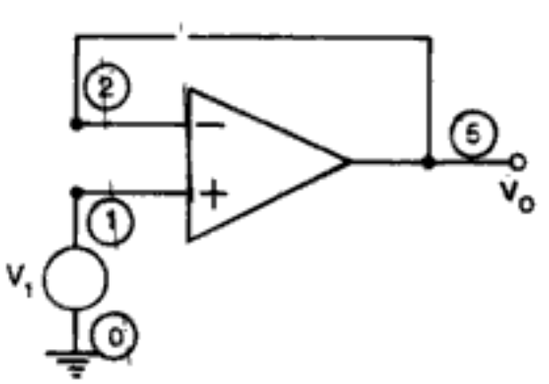

Fig. C 2.3 (a) Circuit for program 2.3

The voltage gain for both d.c. and a.c. input is found to be unity and without change in phase as expected. The transient analysis is shown in Fig. C 2.3 (b). It may be noted that waveforms at node 1 and 5 overlap each other indistinguishably.

Program 2.3 Listing

```
* Voltage Follower
  * * * * Circuit Description
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
* * *
    RF  2  5  IM
*   Op Amp Analysis
    X1  1  2  3  4  5  µA741
    . LIB  EVAL.LIB
*   Power Supplies
    VCC  3  0  DC  12V
    VEE  0  4  DC  12V
*   Input Signal  Source
    V1  1  0  DC  2V  SIN(0 .1V 1KHZ)
*   Output
    * DC  V1  2  2  2
    * TRAN 0.5us 5ms 0ms 0.01 ms
    * PRINT  DC  V(5)  V(1)
    * PROBE

 * * * *     DC Transfer Curves                Temperature = 27.000 DEG C
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
* * *
        V1                          V(5)                          V(1)
    2.000E+00                   2.000E+01                     2.000E + 00
```

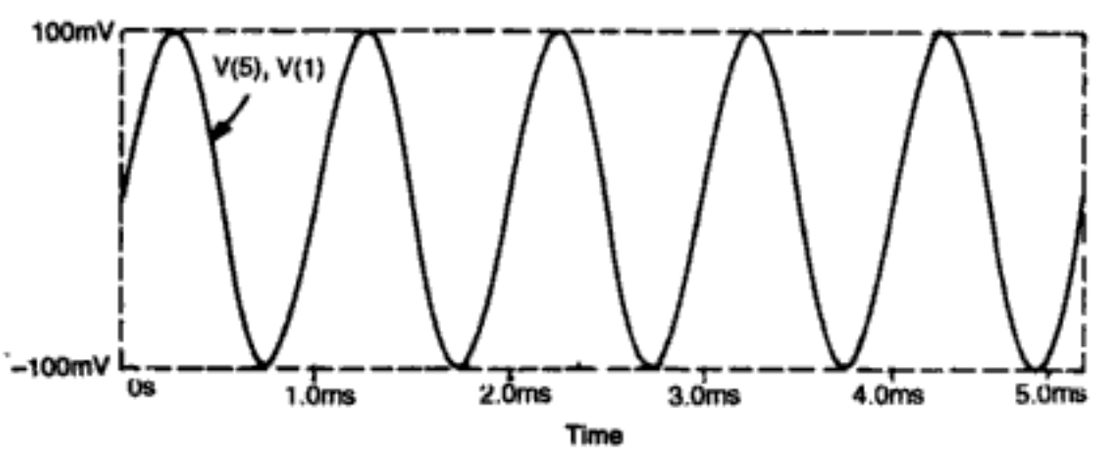

Fig. 2.3 (b) Transient Response of Voltage Follower

3

Operational Amplifier Characteristics

3.1 INTRODUCTION

Earlier we have used an ideal op-amp, and assumed that the op-amp responds equally well to both ac and dc input voltages. However, a practical op-amp does not behave this way. A practical op-amp has some dc voltage at the output even with both the inputs grounded. The factors responsible for this and the suitable compensating techniques are discussed. Also, under ac conditions the characteristics of an op-amp are frequency dependent. The limitations of an op-amp under ac conditions and methods of compensation are discussed.

3.2 DC CHARACTERISTICS

An ideal op-amp draws no current from the source and its response is also independent of temperature. However, a real op-amp does not work this way. Current is taken from the source into the op-amp inputs. Also the two inputs respond differently to current and voltage due to mismatch in transistors. A real op-amp also shifts its operation with temperature. These non-ideal dc characteristics that add error components to the dc output voltage are:

Input bias current
Input offset current
Input offset voltage
Thermal drift.

3.2.1 Input Bias Current

The op-amp's input is a differential amplifier, which may be made of BJT or FET. In either case, the input transistors must be biased into

their linear region by supplying currents into the bases by the external circuit. In an ideal op-amp, we assumed that no current is drawn from the input terminals. However, practically, input terminals do conduct a small value of dc current to bias the input transistors. The base currents entering into the inverting and non-inverting terminals are shown as I_B^- and I_B^+ respectively in Fig. 3.1 (a). Even though both the transistors are identical, I_B^- and I_B^+ are not exactly equal due to internal imbalances between the two inputs. Manufacturers specify input bias current I_B as the average value of the base currents entering into the terminals of an op-amp.

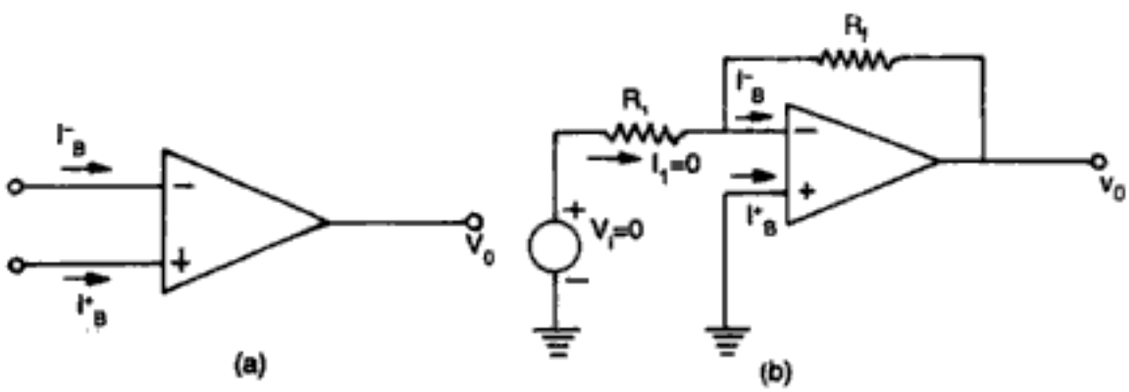

Fig. 3.1 (a) Input bias currents (b) inverting amplifier with bias currents

$$\text{So,} \qquad I_B = \frac{I_B^+ + I_B^-}{2} \tag{3.1}$$

For 741, a bipolar op-amp, the bias current is 500 nA or less. The FET input op-amp will have bias currents as low as 50 pA at room temperature.

Consider the basic inverting amplifier of Fig. 3.1 (b). If input voltage V_i is set to zero volt, the output voltage V_o should also be zero volt. Instead, we find that the output voltage is offset by,

$$V_o = (I_B^-)R_f \tag{3.2}$$

For a 741 op-amp, with a 1 MΩ feedback resistor,

$$V_o = 500 \text{ nA} \times \text{I MΩ} = 500 \text{ mV}$$

The output is driven to 500 mV with zero input because of the bias currents. In applications where signal levels are measured in millivolts, this is totally unacceptable. This effect can be compensated for as shown in Fig. 3.1 (c) where a compensation resistor R_{comp} has been added between the noninverting input terminal and ground. Current I_B^+ flowing through the compensating resistor R_{comp} develops a voltage V_1 across it. Then, by KVL, we get,

$$-V_1 + 0 + V_2 - V_o = 0$$

or

$$V_o = V_2 - V_1 \tag{3.3}$$

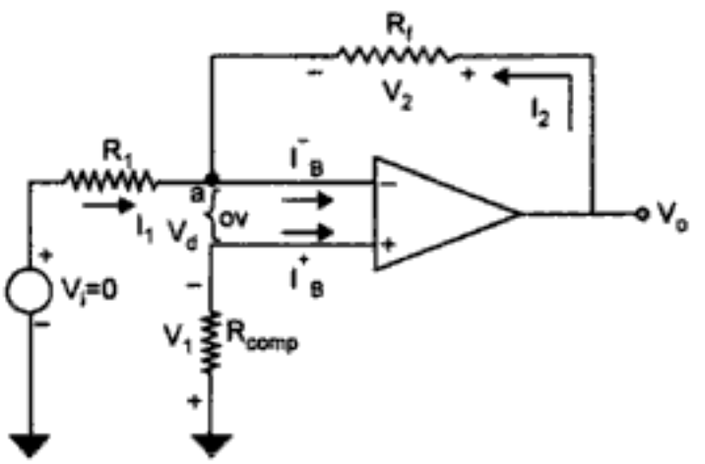

Fig. 3.1 (c) Bias current compensation

By selecting proper value of R_{comp}, V_2 can be cancelled with V_1 and the output V_o will be zero. The value of R_{comp} is derived as

$$V_1 = I_B^+ R_{comp}$$

or
$$I_B^+ = \frac{V_1}{R_{comp}} \tag{3.4}$$

The node 'a' is at voltage $(-V_1)$, because the voltage at the non-inverting input terminal is $(-V_1)$. So, with $V_i = 0$, we get,

$$I_1 = \frac{V_1}{R_1} \tag{3.5}$$

Also,
$$I_2 = \frac{V_2}{R_f} \tag{3.6}$$

For compensation, V_o should be zero for $V_i = 0$, that is, from Eq. (3.3) $V_2 = V_1$

So that,
$$I_2 = \frac{V_1}{R_f} \tag{3.7}$$

KCL at node 'a' gives,

$$I_B^- = I_2 + I_1 = \frac{V_1}{R_f} + \frac{V_1}{R_1} = V_1 \frac{(R_1 + R_f)}{R_1 R_f} \tag{3.8}$$

Assuming $I_B^- = I_B^+$ and using Eqs. (3.4) and (3.8) we get,

$$V_1 \frac{(R_1 + R_f)}{R_1 R_f} = \frac{V_1}{R_{comp}}$$

or, $$R_{comp} = \frac{R_1 R_f}{R_1 + R_f} = R_1 \parallel R_f \tag{3.9}$$

that is, to compensate for bias currents, the compensating resistor R_{comp} should be equal to the parallel combination of resistors tied to the inverting input terminal.

3.2.2 Input Offset Current

Bias current compensation will work if both bias currents I_B^+ and I_B^- are equal. Since the input transistors cannot be made identical, there will always be some small difference between I_B^+ and I_B^-. This difference is called the offset current I_{os} and can be written as

$$|I_{os}| = I_B^+ - I_B^- \tag{3.10}$$

The absolute value sign indicates that there is no way to predict which of the bias currents will be larger.

Offset current I_{os} for BJT op-amp is 200 nA and that for FET op-amp is 10 pA. Even with bias current compensation, offset current will produce an output voltage when the input voltage V_i is zero. Referring to Fig. 3.1 (c),

$$V_1 = I_B^+ R_{comp} \tag{3.11}$$

and $$I_1 = \frac{V_1}{R_1} \tag{3.12}$$

KCL at node 'a' gives,

$$I_2 = (I_B^- - I_1) = I_B^- - \left(I_B^+ \frac{R_{comp}}{R_1} \right) \tag{3.13}$$

Again

$$\begin{aligned} V_o &= I_2 R_f - V_1 \\ &= I_2 R_f - I_B^+ R_{comp} \\ &= \left(I_B^- - I_B^+ \frac{R_{comp}}{R_1} \right) R_f - I_B^+ R_{comp} \end{aligned} \tag{3.14}$$

Substituting Eq. (3.9) and after algebraic manipulation,

$$V_o = R_f [I_B^- - I_B^+] \tag{3.15}$$

So, $$V_o = R_f I_{os} \tag{3.16}$$

So even with bias current compensation and with the feedback resistor of 1 MΩ, a 741 BJT op-amp has an output offset voltage

$$V_o = 1 \text{ M}\Omega \times 200 \text{ nA} = 200 \text{ mV}$$

with a zero input voltage. It can be seen from Eq. (3.16) that the effect of offset current can be minimized by keeping feedback resistance small. Unfortunately, to obtain high input impedance, R_1 must be kept large. With R_1 large, the feedback resistor R_f must also be high so as to obtain reasonable gain.

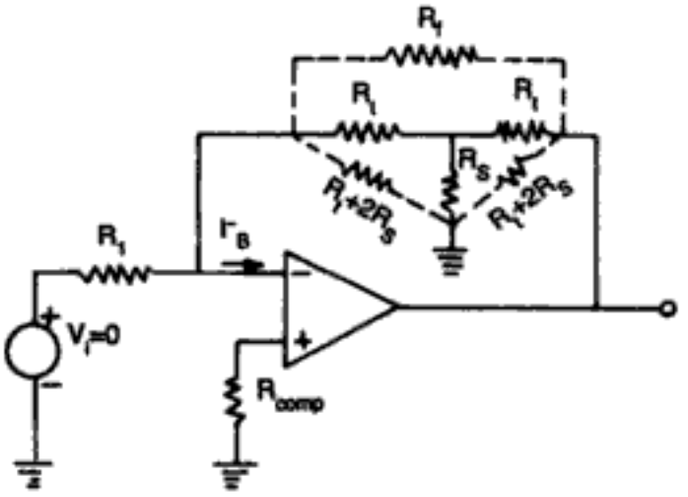

Fig. 3.1 (d) Inverting amplifier with T-feedback network

The T-feedback network in Fig. 3.1 (d) is a good solution. This will allow large feedback resistance, while keeping the resistance to ground (seen by the inverting input) low as shown in the dotted network. The T-network provides a feedback signal as if the network were a single feedback resistor. By T to π conversion,

$$R_f = \frac{R_t^2 + 2\,R_t R_s}{R_s} \tag{3.17}$$

To design a T-network, first pick

$$R_t << \frac{R_f}{2} \tag{3.18}$$

Then calculate $R_s = \dfrac{R_t^2}{R_f - 2R_t}$ (3.19)

Example 3.1

Design an inverting amplifier of the type shown in Fig. 3.1 (d) using 741 op-amp to get a gain of – 10 and an input impedance of 10 MΩ. That is, calculate R_t, R_s and R_1.

Solution

In Fig. 3.1 (d), to set input impedance R_i = 10 MΩ, pick R_1 = 10 MΩ

Since, $A_{CL} = -\dfrac{R_f}{R_1}$

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$$V_{oT} = \left(1 + \frac{R_f}{R_1}\right) V_{os} + R_f I_B \tag{3.24}$$

However, with R_{comp} in the circuit, the total output offset voltage will be given by

$$V_{oT} = \left(1 + \frac{R_f}{R_1}\right) V_{os} + R_f I_{os} \tag{3.25}$$

Many op-amps provide offset compensation pins to nullify the offset voltage. So one must refer to the manufacturer's specifications while using the offset null connections. Figure 3.3 (a) gives the connections for the 741 op-amp. The manufacturers recommend that a 10 kΩ potentiometer be placed across offset null pins 1 and 5 and the wiper be connected to the negative supply pin 4. The position of the wiper is adjusted to nullify the output offset voltage. However, when the given op-amp does not have these offset null pins, external balancing techniques are used. Figures 3.3 (b, c) show the balancing circuits used for inverting and non-inverting operational amplifiers.

Example 3.2

(a) For the non-inverting amplifier of Fig. 3.2 (b), $R_1 = 1$ kΩ and $R_f = 10$ kΩ. Calculate the maximum output offset voltage due to V_{os} and I_B. The op-amp is LM 307 with $V_{os} = 10$ mV and $I_B = 300$ nA, $I_{os} = 50$ nA.

(b) Calculate the value of R_{comp} needed to reduce the effect of I_B.

(c) Calculate the maximum output offset voltage if R_{comp} as calculated in (b) is connected in the circuit.

Solution

(a) $$V_{oT} = \left(1 + \frac{R_f}{R_1}\right) V_{os} + R_f I_B$$

$$= \left(1 + \frac{10\ \text{k}\Omega}{1\ \text{k}\Omega}\right) (10\ \text{mV}) + (10\ \text{k}\Omega)\ (300\ \text{nA})$$

$$= 110\ \text{mV} + 3\ \text{mV} = 113\ \text{mV}$$

(b) The value of R_{comp} needed is,

$$R_{comp} = 1\ \text{k}\Omega \,||\, 10\ \text{k}\Omega = 990\ \Omega$$

(c) With R_{comp} in the circuit,

$$V_{oT} = \left(1 + \frac{R_f}{R_1}\right) V_{os} + R_f I_{os}$$

$$= 110\ \text{mV} + 0.5\ \text{mV} = 110.5\ \text{mV}$$

It can be seen from this example that it is the input offset voltage which is more responsible for producing an output offset voltage compared to input bias current I_B or the input offset current I_{os}.

3.2.5 Thermal Drift

Bias current, offset current and offset voltage change with temperature. A circuit carefully nulled at 25°C may not remain so when the temperature rises to 35°C. This is called drift. Often, offset current drift is expressed in nA/°C and offset voltage drift in mV/°C. These indicate the change in offset for each degree celsius change in temperature.

There are very few circuit techniques that can be used to minimize the effect of drift. Careful printed circuit board layout must be used to keep op-amps away from source of heat. Forced air cooling may be used to stabilize the ambient temperature.

Example 3.3

A non-inverting amplifier with a gain of 100 is nulled at 25°C. What will happen to the output voltage if the temperature rises to 50°C for an offset voltage drift of 0.15 mV/°C?

Solution

Input offset voltage due to temperature rise = 0.15 mV/°C × (50°C – 25°C) = 3.75 mV. Since this is an input change, the output voltage will change by

$$V_o = V_{os} \times A_{CL}$$
$$= 3.75 \text{ mV} \times 100 = 375 \text{ mV}$$

This could represent a very major shift in the output voltage.

3.3 AC CHARACTERISTICS

We have discussed so far the dc characteristics such as bias current, offset current, offset voltage and thermal drift. These will affect the steady state (dc) response of the op-amp only. For small signal sinusoidal (ac) applications, one has to know the ac characteristics such as frequency response and slew-rate which will be discussed in this section.

3.3.1 Frequency Response

Ideally, an op-amp should have an infinite bandwidth. This means that, if its open-loop gain is 90 dB with dc signal its gain should remain the same 90 dB through audio and on to high radio frequencies. The practical op-amp gain, however, decreases (rolls-off) at higher frequencies.

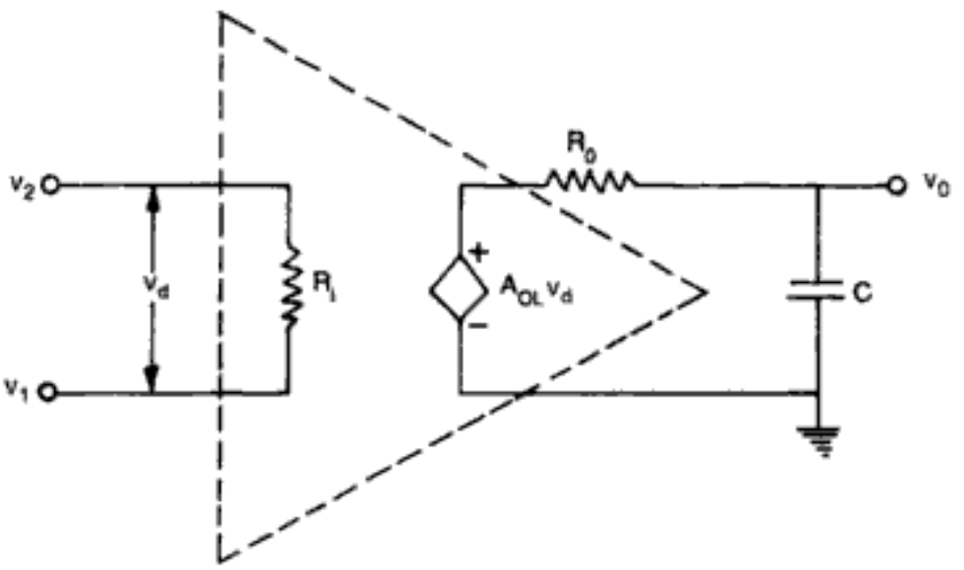

Fig. 3.4 (a) High frequency model of an op-amp with single corner frequency

What causes the gain of the op-amp to roll-off after a certain frequency is reached? Obviously, there must be a capacitive component in the equivalent circuit of the op-amp. This capacitance is due to the physical characteristics of the device (BJT or FET) used and the internal construction of op-amp. For an op-amp with only one break (corner) frequency, all the capacitor effects can be represented by a single capacitor C as shown in Fig. 3.4 (a). This figure represents the high frequency model of the op-amp with a single corner frequency. It may be observed that the high frequency model of Fig. 3.4 (a) is a modified version of the low frequency model with a capacitor C at the output. There is one pole due to R_oC and obviously one – 20 dB/decade roll-off comes into effect.

The open loop voltage gain of an op-amp with only one corner frequency is obtained from Fig. 3.4 (a) as

$$v_o = \frac{-jX_c}{R_o - jX_c} A_{OL} v_d \tag{3.26}$$

or,
$$A = \frac{v_o}{v_d} = \frac{A_{OL}}{1 + j\,2\pi f R_o C}$$

or,
$$A = \frac{A_{OL}}{1 + j(f/f_1)} \tag{3.27}$$

where
$$f_1 = \frac{1}{2\pi R_o C} \tag{3.28}$$

is the corner frequency or the upper 3-dB frequency of the op-amp. The magnitude and the phase angle of the open loop voltage gain are function of frequency and can be written as

$$|A| = \frac{A_{OL}}{\sqrt{1+(f/f_1)^2}} \tag{3.29}$$

$$\phi = -\tan^{-1}(f/f_1) \tag{3.30}$$

The magnitude and phase characteristics from Eq. (3.29) and (3.30) are shown in Fig. 3.4 (b, c). It can be seen that

(i) For frequency $f << f_1$, the magnitude of the gain is 20 log A_{OL} in dB.

(ii) At frequency $f = f_1$, the gain is 3 dB down from the dc value of A_{OL} in dB. This frequency f_1 is called corner frequency.

(iii) For $f >> f_1$, the gain rolls-off at the rate of –20 dB/decade or – 6 dB/octave.

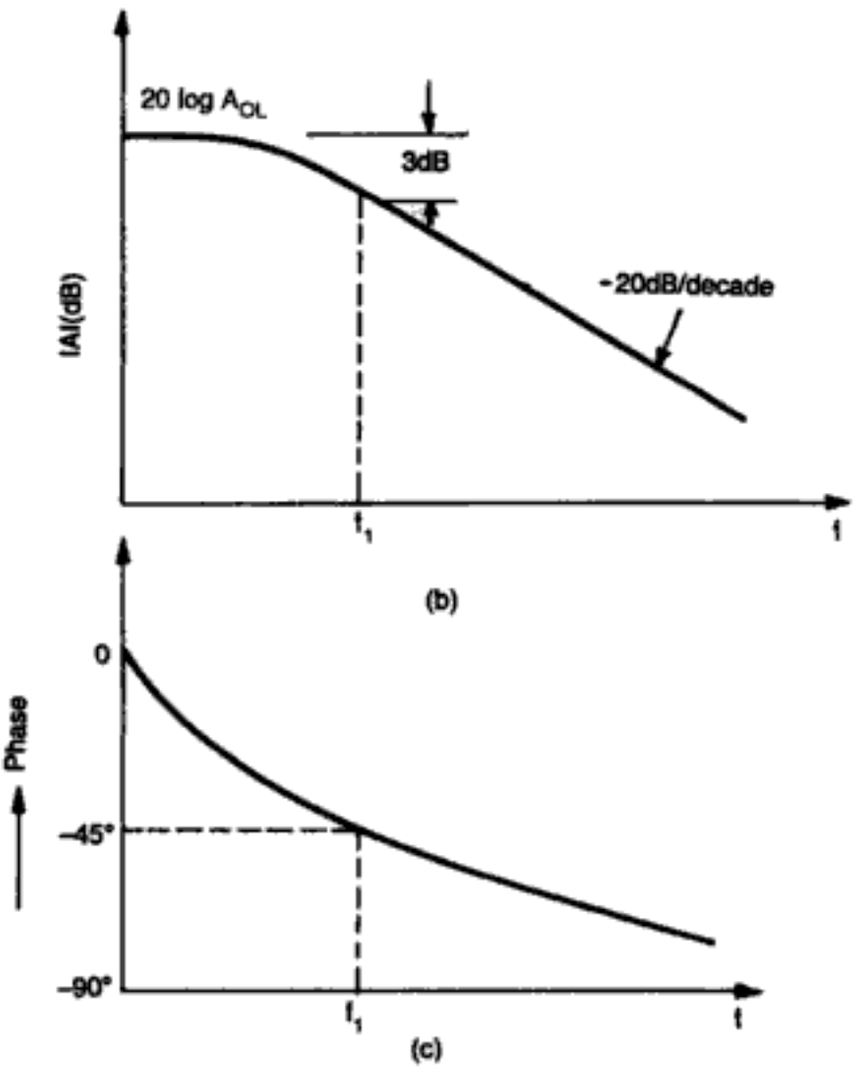

Fig. 3.4 (b) Open loop magnitude characteristics in semilog paper and (c) phase characteristics for an op-amp with single break frequency

It can further be seen from the phase characteristics that the phase angle is zero at frequency $f = 0$. At corner frequency f_1 the phase angle is – 45° (lagging) and at infinite frequency the phase angle is –90°. This shows that a maximum of 90° phase change can occur in an

op-amp with a single capacitor. It may be mentioned here, that zero frequency does not occur in log scale. From all practical purposes, zero frequency is taken as one decade below the corner frequency and infinite frequency is one decade above the corner frequency. The voltage transfer function is s-domain can be written as

$$A = \frac{A_{OL}}{1 + j(f/f_1)} = \frac{A_{OL}}{1 + j(\omega/\omega_1)}$$

$$= \frac{A_{OL} \cdot \omega_1}{j\omega + \omega_1} = \frac{A_{OL} \cdot \omega_1}{s + \omega_1}$$

A practical op-amp, however, has number of stages and each stage produces a capacitive component. Thus due to a number of RC pole pairs, there will be a number of different break frequencies. The transfer function of an op-amp with three break frequencies can be assumed as

$$A = \frac{A_{OL}}{\left(1 + j\frac{f}{f_1}\right)\left(1 + j\frac{f}{f_2}\right)\left(1 + j\frac{f}{f_3}\right)}; 0 < f_1 < f_2 < f_3 \qquad (3.31)$$

or,
$$A = \frac{A_{OL} \cdot \omega_1 \cdot \omega_2 \cdot \omega_3}{(s + \omega_1)(s + \omega_2)(s + \omega_3)} \qquad (3.32)$$

with $0 < \omega_1 < \omega_2 < \omega_3$.

For a typical op-amp, straight line approximation of open-loop gain vs frequency in logarithmic scale is shown in Fig. 3.5. The open loop

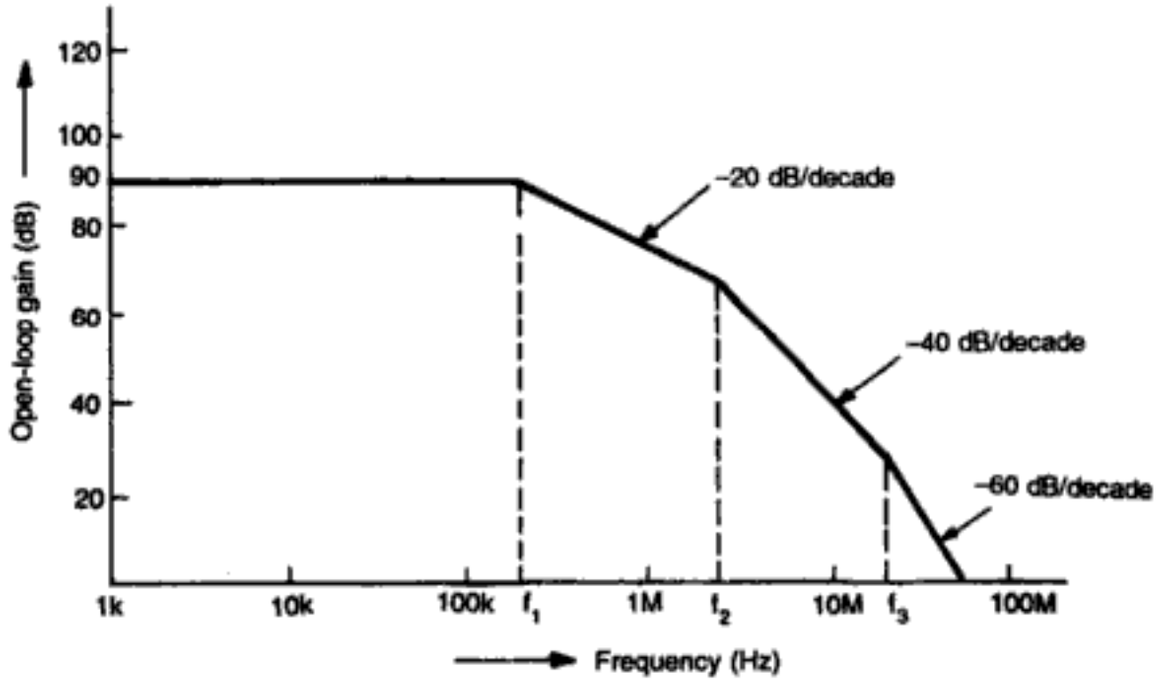

Fig. 3.5 Approximation of open loop gain vs frequency curve

frequency response is flat (90 dB) from low frequencies (including dc) to 200 kHz, the first break frequency. From 200 kHz to 2 MHz, the gain drops from 90 dB to 70 dB which is at a –20 dB/decade or –6 dB/octave rate. At frequencies from 2 MHz to 20 MHz, the roll-off rate is –40 dB/decade or –12 dB/octave. Accordingly, as frequency is increasing, cascading effect of RC pairs (poles) come into effect and roll-off rate increases successively by –20 dB/decade at each corner frequency. Each RC pole pair also introduces a lagging phase of maximum up to –90°.

3.3.2 Stability of an Op-Amp

Op-amps are rarely used in open loop configuration because of its high gain. Let us now consider the effect of feedback on op-amp frequency response. Consider an op-amp amplifier of Fig. 3.6. (a). It uses resistor feedback network and may be used as an inverting amplifier for $v_2 = 0$ and as non-inverting amplifier for $v_1 = 0$.

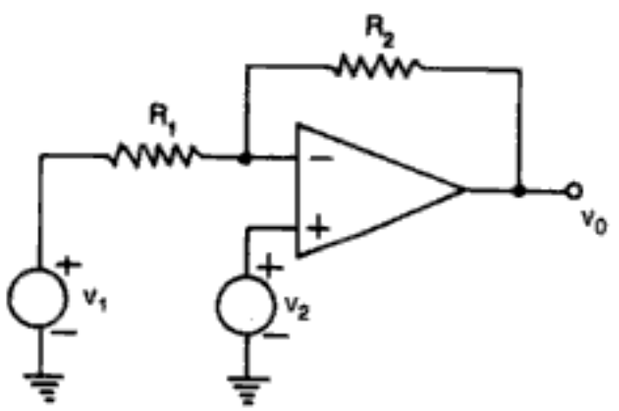

Fig. 3.6 (a) Resistive feedback provided in op-amp

From the negative feedback concepts, we may write the closed loop transfer function as

$$A_{CL} = \frac{A}{1 + A\beta} \tag{3.33}$$

where A is the open loop voltage gain and β is the feedback ratio. In Eq. (3.33), if characteristic equation $(1 + A\beta) = 0$, the circuit will become just unstable, that is, leads into sustained oscillation.

Rewriting the characteristic equation as, $1 - (-A\beta) = 0$ leads to

$$\text{loop gain, } -A\beta = 1 \tag{3.34}$$

Since $A\beta$ is a complex quantity, the magnitude condition become

$$|A\beta| = 1 \tag{3.35}$$

and phase condition is

$$\angle -A\beta = 0 \text{ (or multiple of } 2\pi)$$

or,
$$\angle A\beta = \pi \text{ (or odd multiple of } \pi) \tag{3.36}$$

In the given circuit, feedback network is a resistive network, so it does not provide any phase shift. Since op-amp is used in the inverting mode, it provides a phase shift of 180° at low frequencies. However, at high frequencies, due to each corner frequency, an additional phase shift of maximum –90° can take place in open loop gain A. So for two corner frequencies, a maximum of phase shift that can be associated with gain A is –180°. Thus at high frequencies, it is quite possible that for some value of β, the magnitude of $A\beta$ becomes unity when A has an additional phase shift of 180° which makes the total phase shift equal to zero. In this case, there is every possibility that the amplifier may begin to oscillate as both the magnitude and phase conditions laid down by Eqs. (3.35) and (3.36) are satisfied. This may be noted that oscillation is just the starting point of instability, or, to be more precise, it is just at the verge of instability. The instability means unbounded output; which can arise from Eq. (3.33), when

$$(1 + A\beta) < 1$$

or $$A\beta < 0 \qquad \text{i.e. negative}$$

and then $A_{CL} > A$, i.e. the closed loop gain increases and leads to instability. The phase contribution by the resistive feedback network is zero. At low frequency, the additional phase contribution of A is zero, so $A\beta > 0$ and obviously $A_{CL} < A$ and the system is stable. But at high frequencies, the system A having three corner frequencies or three RC pole pair, there is a chance of open loop gain A to contribute a maximum of $-270°$ phase shift and for which $A\beta$ may become negative and instability occurs at high frequencies. This is further elaborated in Fig. 3.6 (b).

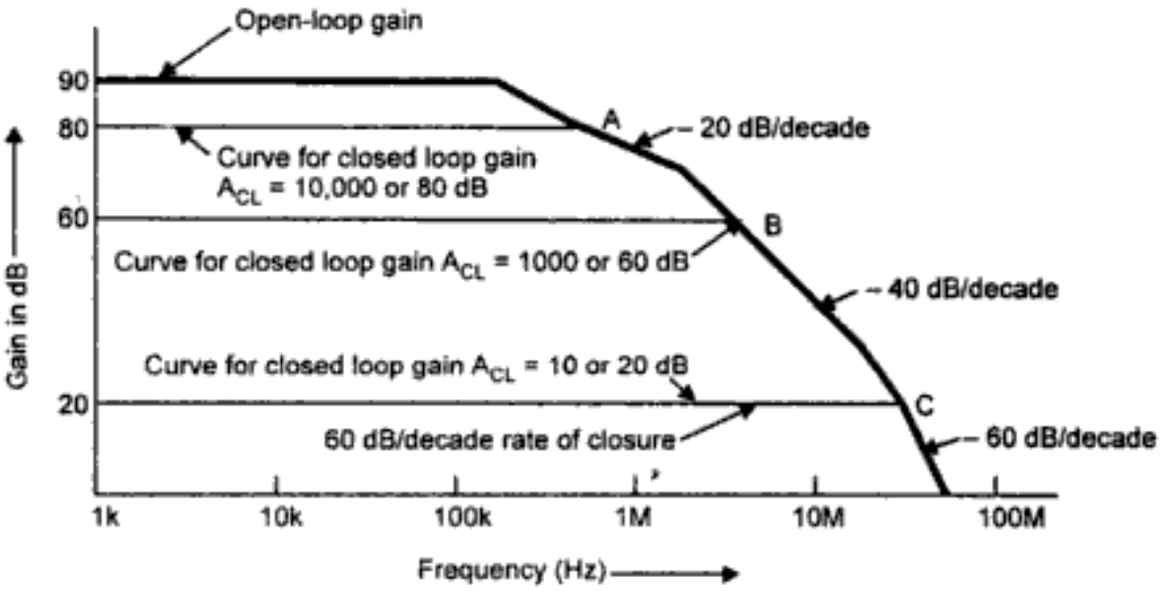

Fig. 3.6 (b) Effect of feedback on open loop gain vs frequency curve

Let us say that a closed loop gain of 80 dB ($|A_{CL}| = 10{,}000$) is desired. The projection of 80 dB curve to the open loop frequency response curve intersects it at a – 20 dB/decade rate of closure (point A)

as shown in Fig. 3.6 (b). The bandwidth is approximately 600 kHz and a maximum of –90° phase shift is added to open loop gain A. The amplifier will remain stable.

Now, if the feedback resistors are so chosen that the op-amp has a closed loop gain of 1,000 or 60 dB, the bandwidth is about 3.5 MHz. However, now the 60 dB projection on the open-loop curve intersects at a –40 dB/decade rate of closure (point B). The maximum phase shift that may get added to is now (– 90° – 90°), that is –180°. This circuit is likely to be unstable and should not be used without modification. Similarly, a closed loop gain of 20 dB causes a – 60 dB/decade rate of closure (point C). A maximum –270° phase shift is added to the open loop gain A to cause unstable operation. Thus, we may conclude that for stable operation, the rate of closure between the closed loop gain projection and the open-loop curve should not exceed –20 dB/decade. At higher frequencies for lower closed loop gains, the feedback becomes significant and regenerative and may result in sustained oscillations.

So far, we have discussed stability of an op-amp qualitatively. To provide a quantitative discussion about stability, let us rewrite the transfer function of an op-amp characterized by three poles, as,

$$A = -\frac{A_{OL}\,\omega_1\,\omega_2\,\omega_3}{(s+\omega_1)(s+\omega_2)(s+\omega_3)};\ 0 < \omega_1 < \omega_2 < \omega_3$$

Obviously the poles of the open-loop transfer function are at $-\omega_1$, $-\omega_2$ and $-\omega_3$. The closed loop poles, that is the poles of A_{CL} in Eq. (3.33) will be given by the roots of the characteristic equation

$$1 + A\beta = 0$$

Putting the value of A from Eq. (3.32) we get,

$$1 + \frac{\beta A_{OL}\,\omega_1\,\omega_2\,\omega_3}{(s+\omega_1)(s+\omega_2)(s+\omega_3)} = 0$$

or, $$(s + \omega_1)(s + \omega_2)(s + \omega_3) + \beta A_{OL}\,\omega_1\,\omega_2\,\omega_3 = 0$$

or, $$s^3 + s^2(\omega_1 + \omega_2 + \omega_3) + s(\omega_1\,\omega_2 + \omega_1\,\omega_3 + \omega_2\,\omega_3) + \omega_1\,\omega_2\,\omega_3 (1 + \beta A_{OL}) = 0 \qquad (3.37)$$

The roots of the cubic equation depend upon βA_{OL}, the dc loop gain and therefore, (βA_{OL}) becomes critical parameter that determines the new pole location. Further, βA_{OL} can take any value between zero for no feedback ($\beta = 0$) and A_{OL} for maximum feedback ($\beta = 1$). For variable β in the range $0 < \beta A_{OL} < \infty$, the root loci is shown in Fig. 3.7. When $\beta A_{OL} = 0$, the roots are at $-\omega_1$, $-\omega_2$ and $-\omega_3$ and lie on the negative real axis. For small values of βA_{OL} the roots still lie on the left half os s-plane with one real root and two complex conjugate roots (a, a′). If βA_{OL} is increased further beyond a critical value $(\beta A_{OL})_c$, the two roots will move to the right half of s-plane causing instability. We

will find out that critical value of βA_{OL} for which the closed loop system becomes just unstable. Rewriting Eq. (3.37) as

$$a_3 s^3 + a_2 s^2 + a_1 s + a_o = 0 \tag{3.38}$$

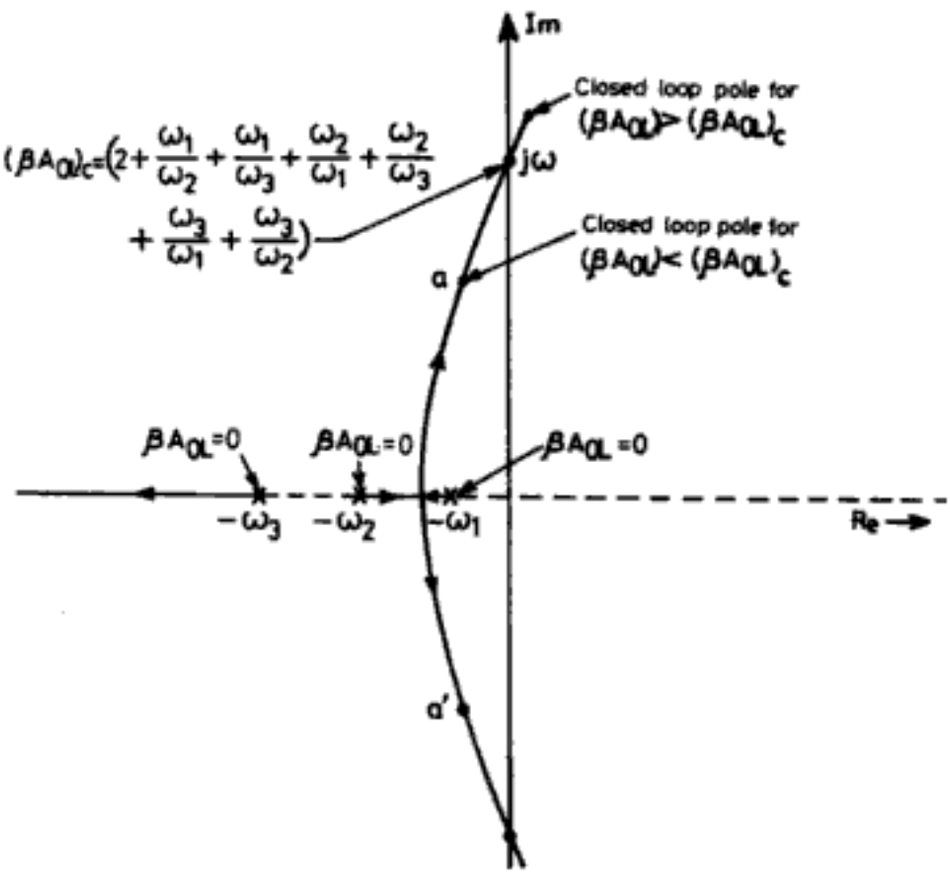

Fig. 3.7 Root loci as a function of βA_{OL}

where,

$$a_3 = 1$$
$$a_2 = \omega_1 + \omega_2 + \omega_3$$
$$a_1 = \omega_1 \omega_2 + \omega_1 \omega_3 + \omega_2 \omega_3$$
$$a_o = \omega_1 \omega_2 \omega_3 (1 + \beta A_{OL})$$

In order to find the critical value of βA_{oL}, apply Routh's stability criterion to Eq. (3.38). That is,

(i) All the coefficients a_3, a_2, a_1 and a_o should be positive.

(ii) $a_2 a_1 - a_3 a_o \leq 0$ (3.39)

Put $s = j\omega$ in Eq. (3.38)

$$a_3 (j\omega)^3 + a_2 (j\omega)^2 + a_1 (j\omega) + a_o = 0$$
$$(a_o - a_2 \omega^2) + j\omega(a_1 - a_3 \omega^2) = 0$$

Equating real and imaginary parts to zero, we get

$$a_o - a_2 \omega^2 = 0, \tag{3.40}$$
$$a_1 - a_3 \omega^2 = 0 \tag{3.41}$$

Thus, the frequency of oscillation is given by,

$$\omega_{osc} = \pm\sqrt{\frac{a_0}{a_2}} = \pm\sqrt{\frac{a_1}{a_3}} \tag{3.42}$$

Putting values of coefficients,

$$\omega_{osc} = \sqrt{\frac{a_1}{a_3}} = \sqrt{\omega_1\omega_2 + \omega_1\omega_3 + \omega_2\omega_3}$$

Also from Eq. (3.39), we get,

$$a_0 = \frac{a_2\, a_1}{a_3}$$

or $\omega_1\omega_2\omega_3\{1 + (\beta A_{OL})_c\} = (\omega_1 + \omega_2 + \omega_3)(\omega_1\omega_2 + \omega_1\omega_3 + \omega_2\omega_3)$

or, $$(\beta A_{OL})_c = 2 + \frac{\omega_1}{\omega_2} + \frac{\omega_1}{\omega_3} + \frac{\omega_2}{\omega_1} + \frac{\omega_2}{\omega_3} + \frac{\omega_3}{\omega_1} + \frac{\omega_3}{\omega_2} \tag{3.44}$$

It is obvious that $(\beta A_{OL})_c$ depends upon the ratio of open loop pole locations. The minimum value of $(\beta A_{OL})_c$ will occur when all the poles are located at the same place giving $(\beta A_{OL})_c = 8$.

As an example, if $A_{OL} = 10^5$ and $\omega_1 = \omega_2 = \omega_3 = 10^7$ rad/s, then the circuit will oscillate at a frequency of

$$\omega_{osc} = \omega_1\sqrt{3} = 10^7\sqrt{3} \text{ rad/s.}$$

On the other hand, if 10000 $\omega_1 = \omega_2 = \omega_3$, the critical loop gain is,

$$(\beta A_{OL})_c \simeq 2\frac{\omega_2}{\omega_1} \simeq 20000$$

and, $$\beta_c < \frac{20000}{A_{OL}} = \frac{20000}{100000} = 0.2$$

In the Fig. 3.6 (a), $\beta = R_1/(R_1 + R_2)$.

For, $\beta < 0.2$,

$$\frac{R_1 + R_2}{R_1} > \frac{1}{0.2} = 5$$

or, $$\frac{R_2}{R_1} \geq 4$$

This means that if op-amp is used as an inverting amplifier in Fig. 3.6 (a), the inverting gain magnitude should be greater than 4 and if used as non-inverting amplifier, the non-inverting gain should be greater than 5 for oscillation to sustain.

If it is desired that the amplifier should remain stable for any resistive network, that is, $0 < \beta < 1$, then A_{OL} must satisfy the most

stringent condition for $\beta = 1$, that is,

$$A_{OL} < \left(2 + \frac{\omega_1}{\omega_2} + \frac{\omega_1}{\omega_3} + \frac{\omega_2}{\omega_1} + \frac{\omega_2}{\omega_3} + \frac{\omega_3}{\omega_1} + \frac{\omega_3}{\omega_2}\right) \tag{3.45}$$

3.3.3 Frequency Compensation

In applications where one desires large bandwidth and lower closed loop gain, suitable compensation techniques are used. Two types of compensating techniques are used (i) External Compensation, (ii) Internal Compensation.

External Frequency Compensation

Some types of op-amps are made to be used with externally connected compensating components specially if they are to be used for relatively low closed loop gain. The compensating network alters the open-loop gain so that the roll-off rate is –20 dB/decade over a wide range of frequency.

The common methods for accomplishing this are:

Dominant-pole compensation
Pole-zero (lag) compensation

Dominant-pole Compensation: Suppose A is the uncompensated transfer function of the op-amp in open-loop condition as given by Eq. (3.32). Introduce a dominant pole by adding RC-network in series with op-amp as in Fig. 3.8 (a) or by connecting a capacitor C from a suitable high resistance point to ground. The compensated transfer function A' becomes

$$A' = \frac{v_o}{v_i}$$

$$= A \cdot \frac{\frac{-j}{\omega C}}{R - \frac{j}{\omega C}} = \frac{A}{1 + j\frac{f}{f_d}} \tag{3.46}$$

where, $$f_d = \frac{1}{2\pi RC}$$

using Eq. (3.31) we get,

$$A' = \frac{A_{OL}}{\left(1 + j\frac{f}{f_d}\right)\left(1 + j\frac{f}{f_1}\right)\left(1 + j\frac{f}{f_2}\right)\left(1 + j\frac{f}{f_3}\right)}$$

where $$f_d < f_1 < f_2 < f_3$$

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$$\frac{v_o}{v_2} = \frac{Z_2}{Z_1 + Z_2} = \frac{R_2}{R_1 + R_2} \frac{1 + j\dfrac{f}{f_1}}{1 + j\dfrac{f}{f_o}} \tag{3.47}$$

where $Z_1 = R_1$, $Z_2 = R_2 + \dfrac{1}{j\omega C_2}$, $f_1 = \dfrac{1}{2\pi R_2 C_2}$, $f_o = \dfrac{1}{2\pi(R_1 + R_2)C_2}$

The compensating network is designed to produce a zero at the first corner frequency f_1 of the uncompensated transfer function A. This zero will cancel the effect of the pole at f_1. The pole of the compensating network at $f_o = \omega_o/2\pi$ is selected so that the compensated transfer function A' passes through 0 dB at the second corner frequency f_2 of the uncompensated transfer function A in Eq. (3.31). The frequency can be found graphically by having A' pass through 0 dB at the frequency f_2 with a slope of –20 dB/decade as shown in Fig. 3.9 (b). Assuming that the compensating network does not load the amplifier, i.e. $R_2 >> R_1$, then the overall transfer function becomes.

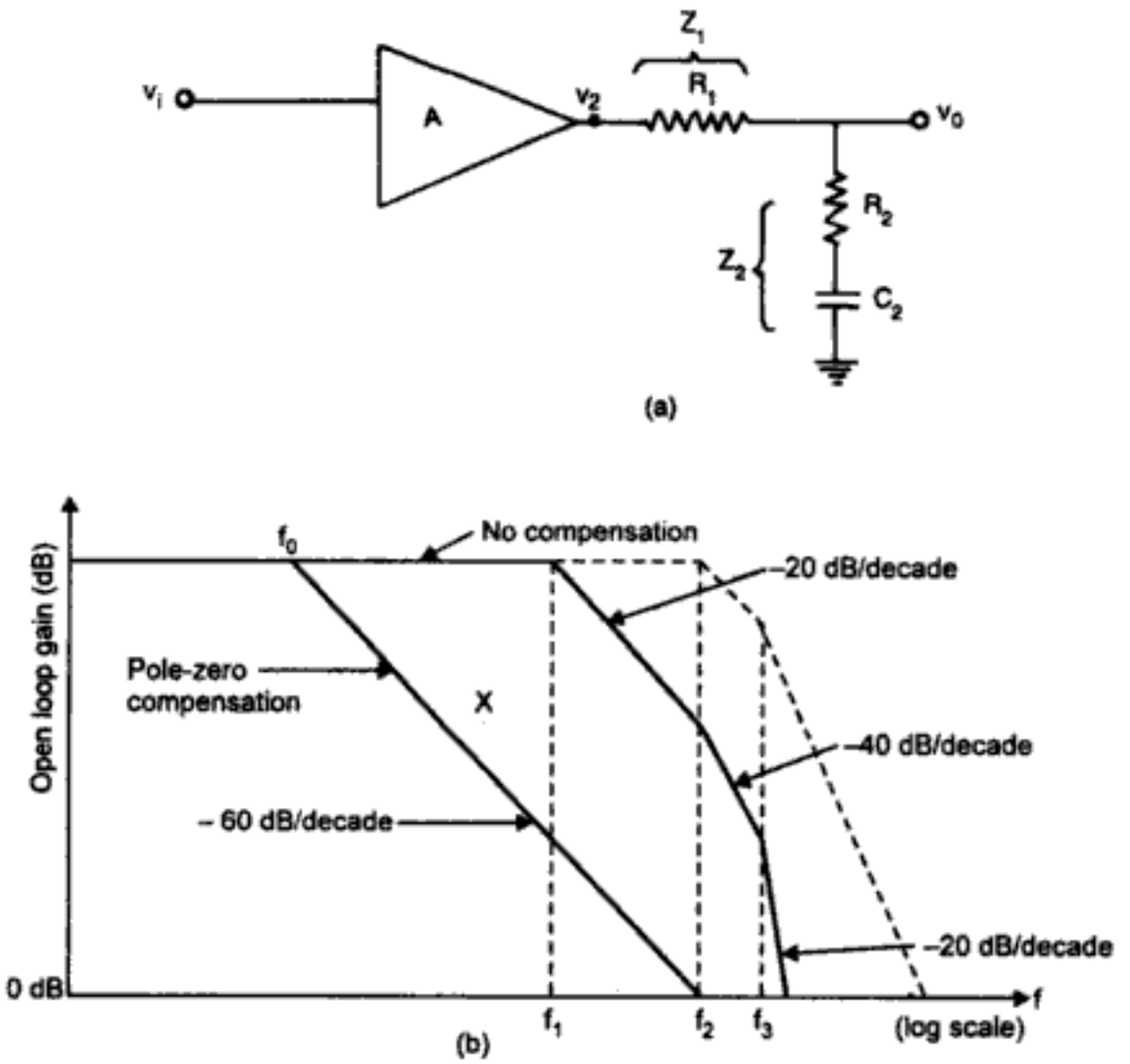

Fig. 3.9 (a) Pole-zero compensation (b) Open loop gain vs. frequency for pole-zero compensation

$$A' = \frac{v_o}{v_i} = \frac{v_o}{v_2} \cdot \frac{v_2}{v_i} = A \cdot \frac{R_2}{R_1 + R_2} \frac{1 + j\dfrac{f}{f_1}}{1 + j\dfrac{f}{f_o}}$$

$$= \frac{A_{OL}}{\left(1 + j\dfrac{f}{f_1}\right)\left(1 + \dfrac{f}{f_2}\right)\left(1 + j\dfrac{f}{f_3}\right)} \cdot \frac{R_2}{R_1 + R_2} \frac{1 + j\dfrac{f}{f_1}}{1 + j\dfrac{f}{f_o}}$$

$$= \frac{A_{OL}}{\left(1 + j\dfrac{f}{f_o}\right)\left(1 + j\dfrac{f}{f_2}\right)\left(1 + j\dfrac{f}{f_3}\right)} \tag{3.48}$$

with $0 < f_o < f_1 < f_2 < f_3$

and note that $R_2 >> R_1$, so that $\dfrac{R_2}{R_1 + R_2} \approx 1$.

Consider again the frequency response (Bode plot) for the uncompensated op-amp having three poles at frequencies f_1, f_2 and f_3. Now select R_2 and C_2 so that the zero of the compensating network is equal to the pole at the frequency f_1 (lowest). If there had been no pole added by the compensating network, the response would have changed to that of the dotted curve. However, because of the predominance of the pole of the compensating network at f_o, the rate of closure will be – 20 dB/decade throughout as shown in the curve *X* of Fig. 3.9 (b). The pole at f_o should be selected so that the –20 dB/decade fall should meet the 0-dB line at f_2 which is the second pole of *A*.

A comparison of dominant pole and pole-zero compensation technique is shown in Fig. 3.10. The dominant pole is selected so that the compensated transfer function goes through 0-dB at the first pole f_1 of the uncompensated system. In pole-zero compensation, the zero is chosen at f_1 and pole is selected so that the modified transfer function goes through 0-dB at the second pole f_2 of uncompensated transfer function. The improvement in bandwidth is clearly shown in Fig. 3.10 and is given by $(f_2 - f_1)$.

With either type of compensation, the value of the compensating capacitance is too large to be easily built into standard integrated circuit and as a result, many IC op-amps have internal connections brought out to allow attachment of an external compensating network. However, recently, several op-amps have become available with built-in lag compensation which is accomplished by making use of Miller effect to generate large capacitance needed from fixed small capacitance which can be built into the IC.

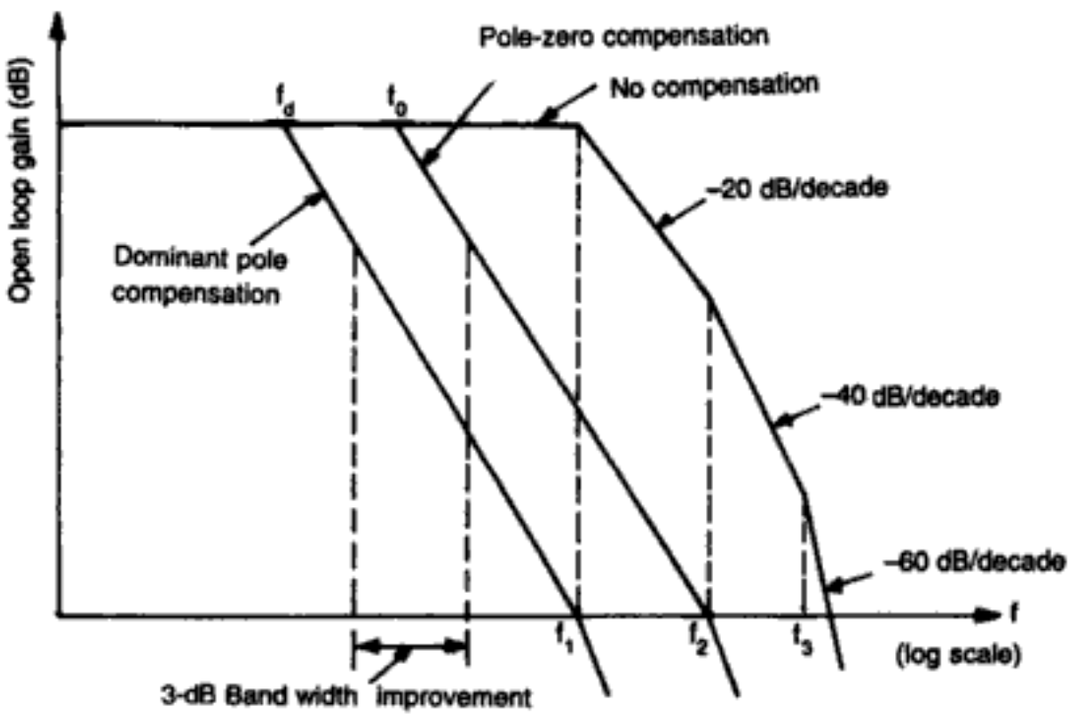

Fig. 3.10 Comparison of dominant pole and pole-zero techniques

Internally Compensated Operational Amplifier

Sometimes, the relatively broad bandwidth of the uncompensated op-amp is not needed. For example, in the instrumentation circuit, the op-amp required is to amplify relatively slow changing signals and therefore it does not require good high-frequency response. In this and similar applications, internally compensated op-amps can be used. They are sometimes called compensated op-amps. Also they are stable regardless of the value of closed-loop gain and without externally connected compensating components. The type 741 op-amp is compensated and has an open-loop gain vs frequency response as shown in Fig. 3.11. The op-amp IC 741 contains a capacitance C_1 of 30 pF (see Fig. 2.22 (a)) that internally shunts off signal current and thus reduces the available output signal at higher frequencies. This internal capacitance, which is an internal compensating component, causes the open-loop gain to roll-off at –20 dB/decade rate and thus assures for a stable circuit. The 741 op-amp has a 1 MHz gain-bandwidth product. This means that the product of the coordinates, gain and frequency of any point on the open-loop gain vs frequency curve is about 1 MHz. If 741 op-amp is wired for a closed-loop gain of 10^4 or 80 dB, its bandwidth is 100 Hz as can be seen by projecting to the right from 10^4 in the curve of Fig. 3.11. For gain of 10^2, the bandwidth increases to 10 kHz and for gain 1, the bandwidth is 1 MHz. For 741 op-amp, unity gain-bandwidth product is specified as 1 MHz in the data sheet. This simply means that op-amp 741 has 1 MHz bandwidth with unity gain as seen in Fig. 3.11. Some internally compensated op-amps are Fairchild's μA 741, National Semiconductor's LM741, LM107 and LM112 and Motorola's MC1558.

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Figure 3.15 gives the data sheet for a Fairchild μA741 op-amp. 741 series are available in models 741, 741A, 741C and 741E. The schematic diagram and electrical parameters for all these models are the same with only the values of the parameters differing from one model to another. We will consider specifications for 741C op-amp.

From the data sheet it can be seen that:

1. 741 is internally frequency compensated op-amp.
2. 741 is a monolithic IC fabricated using planar epitaxial process.
3. It is useful for integrator, summer, voltage follower and other feedback applications.
4. Absolute maximum ratings are specified for supply voltage, internal power dissipation, differential input voltage, input voltage, storage and operating temperature ranges, soldering pin temperature and output short circuit duration.
5. 741 is available in all three packages viz 8-pin metal can, 10-pin flat pack and 8 or 14 pin DIP. The pin diagrams for all these packages are shown in the data sheet.
6. For 741C, two sets of electrical specifications are available, one set is applicable at room temperature (25°C) and other set applies to the commercial temperature range (0° to + 70°C). As we are interested only in showing the significance of the parameters listed, we limit the discussion to only one model, that is 741C at 25°C.

The various electrical parameters supplied in the data sheet are as follows:

Input offset voltage: It is the voltage that must be applied between the input terminals of an op-amp to nullify the output. Since this voltage could be positive or negative its absolute value is listed on the data sheet. For 741C, the maximum value is 6 mV.

Input offset current: The algebraic difference between the currents into the (–) input and (+) input is referred to as input offset current. It is 200 nA maximum for 741C.

Input bias current: The average of the currents entering into the (–) input and (+) input terminals of an op-amp is called input bias current. Its value is 500 nA for 741C.

Input resistance: This is the differential input resistance as seen at either of the input terminals with the other terminal connected to ground. For the 741C, the input resistance is 2 MΩ.

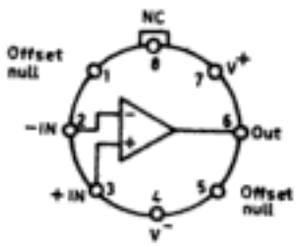
Input capacitance: It is the equivalent capacitance that can be measured at either of the input terminal with the other terminal connected to ground. A typical value of C_i is 1.4 pF.

Offset voltage adjustment range: special feature of the 741 family op-amp is the provision of offset voltage null capability. For

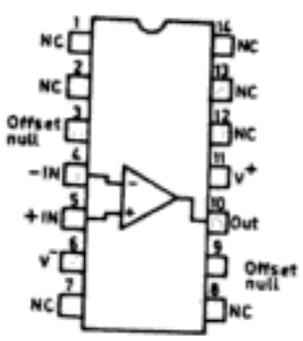
General Description: The μA741 is a high performance monolithic operational amplifier constructed using the planer epitaxial process. High common mode voltage range and absence of latch-up tendencies make the μA741 ideal for use as voltage follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier and general feedback applications.

*No frequency compensation required
*Short circuit protection
*Offset voltage null capability
*Large common mode and differential voltage ranges
*Low power consumption
*No latch-up

8 Pin Mini Metal Can
(top view)



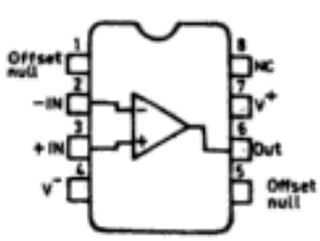
10 Pin DIP
(top view)



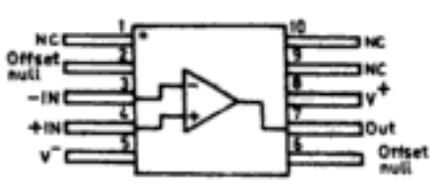
Absolute Maximum Ratings

Supply voltage	
μA741A, μA741, μA741E	± 22 V
μA741C	± 18 V
Internal Power Dissipation	
Metal Can	500 m W
Molded and Hermetic DIP	670 m W
Mini DIP	310 m W
Flatpack	570 m W
Differential Input Voltage	± 30 V
Input Voltage	± 15 V
Operating temperature Range	
Military (μA741A, μA741)	− 55 °C to 125 °C
Commercial (μA741E, μA741C)	0 °C to 70 °C

8 Pin Mini DIP
(top view)



10 Pin Flatpak
(top view)



μA741C

Electrical Characteristics V_s = ±15 V, T_A = 25°C unless otherwise specified

CHARACTERISTICS (see definitions)		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_s \leq 10$ kΩ		20		mV
Input Offset Current			20	200	nA	
Input Bias Current			80	500	nA	
Input Resistance		0.3	2.0		MΩ	
Input Capacitance			1.4		pF	
Offset Voltage Adjustment Range			± 15		mV	
Input Voltage Range		± 12	± 13		V	
Common Mode Rejection Ratio		$R_s \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio		$R_s \leq 10$ kΩ		30	150	μV/V
Large Singal Voltage Gain		$R_L \geq$ kΩ		20,000	200,000	
		V_{out} = ± 10V				
Output Voltage Swing		$R_L \geq 10$ kΩ	± 12	± 14		V
		$R_L \geq 2$ kΩ	± 10	± 13		V
Output Resistance			75		Ω	
Output Short Circuit Current			25		mA	
Supply Current			1.7	2.8	mA	
Power Consumption			50	85	mW	
Transient Response	Rise Time	V_{in} = 200 mV,				
(unity Gain)		R_L = 2kΩ			0.3	μs
	Overshoot	C_L = 100 pF			6.0	%
Slew Rate		$R_L \geq 2$ kΩ			0.5	V/μs

Fig. 3.15 Data Sheet of μA 741

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12. Internally compensated op-amps are also available but give smaller bandwidth.
13. Large signal output (> 1V) is limited by the speed at which the op-amp can charge compensating capacitor. This is called slew rate and is expressed in volts per micro-second.
14. The manufacturers supply data sheets for the ICs they produce. The data sheet gives pin diagrams, equivalent circuits, absolute maximum ratings, electrical characteristics and typical applications of the device.

Review Questions

3.1. List the non-ideal dc characteristics of an op-amp.
3.2. Why do we use R_{comp} resistor?
3.3. Why is R_{comp} not needed in differential amplifier?
3.4. How is input offset voltage compensated for?
3.5. What produces more offset voltage at the output: input offset current or input bias current?
3.6. Define thermal drift.
3.7. List the parameters that are important for ac applications.
3.8. What does the term roll-off mean?
3.9. What is Bode plot?
3.10. What problem can occur with an amplifier with a steep gain roll-off?
3.11. Why are low closed loop gains avoided with uncompensated op-amps?
3.12. If an op-amp is specified as being compensated, what does this mean?
3.13. If closed loop gain of an op-amp is increased, what happens to bandwidth.
3.14. If the gain-bandwidth product of an op-amp is 2 MHz, what is its bandwidth when connected as a voltage follower?
3.15. Define slew rate. What causes the slew rate?
3.16. How is the slew rate measured?
3.17. What is the effect of operation frequency on the maximum unclipped output signal capability of an op-amp.
3.18. List and explain the parameters given in manufacturer's data sheet of an op-amp.
3.19. The dc open loop gain of an op-amp is 100,000. What will be the open loop gain at its break frequency?
3.20. The transient response rise time (*unity gain*) of an op-amp is 0.07 μs. Find the small signal band width.
3.21. What is the difference between the open loop and closed loop gain of an op-amp.
3.22. Does increasing the compensating capacitor increase or decease unity-gain band-width.

3.23. How fast can the output of an op-amp change by 10 V, if its slew rate is 1V/μs.

3.24. Find the maximum frequency for a sine wave output voltage of 10 V peak with an op-amp whose slew rate is 1V/μs.

PROBLEMS

3.1. A 741 op-amp is used as an inverting amplifier shown in Fig. 3.2 (c) with R_1 = 1 kΩ and R_f = 100 kΩ. What is the maximum output offset voltage caused by the input offset voltage V_{os}. For 741, V_{os} = 6 mV.

3.2. Repeat Problem 3.1, if op-amp used is LM 307 with V_{os} = 10 mV; R_1 = 100 Ω and R_f = 4.7 kΩ.

3.3. In an inverting amplifier of the type shown in Fig. 3.2 (c), R_1 = 100 kΩ, R_f = 10 MΩ. Calculate (i) maximum output offset voltage caused by the input offset voltage V_{os}; (ii) maximum output offset voltage caused by the input bias current I_B. The op-amp used is 741 with V_{os} = 6 mV; I_B = 500 nA.

3.4. In problem 3.3, calculate the value of R_{comp} needed to eliminate the effect of input bias current.

3.5. In an inverting amplifier R_1 = 1 kΩ, R_f = 100 kΩ. The op-amp has the following specifications:

$$\frac{\Delta V_{os}}{\Delta T} = 30\ \mu V/°C \text{ max}$$

$$\frac{\Delta I_{os}}{\Delta T} = 0.3\ nA/°C \text{ max}$$

Assume that the amplifier is nulled at 25°C. Calculate the value of the error voltage and the output voltage V_o at 35°C, if (i) V_i = 1 mV dc; (ii) V_i = 5 mV dc.

3.6. Repeat Problem 3.5, for a non-inverting amplifier.

3.7. The LM312 op-amp is used as an inverting amplifier with the following specifications:

$$\frac{\Delta V_{os}}{\Delta T} = 30\ \mu V/°C;\ \frac{\Delta I_{os}}{\Delta T} = 10\ nA/°C$$

$$R_1 = 1\ k\Omega;\ R_f = 4.7\ k\Omega.$$

Assume that the amplifier is nulled at 25°C. A sine wave of 10 mV peak amplitude at 100 Hz is applied. Draw the output voltage waveform at 25°C and 45°C.

3.8. Repeat Problem 3.7 for a non-inverting amplifier.

3.9. (a) An op-amp has a slew rate of 2 V/μs. What is the maximum frequency of an output sinusoid of peak value 5 V at which distortion sets in due to the slew rate limitation.

(b) If a sinusoid of 10 V peak is specified, what is the full power bandwidth?

3.10. An op-amp has a slew rate of 2V/μs. Find the rise time for an output voltage of 10 V amplitude resulting from a rectangular pulse input if the op-amp is slew rate limited.

Experiment 3.1

To measure (a) input bias current, (b) input offset current and (c) input offset voltage of the given op-amp.

Procedure

(a) Set up the circuit shown in Fig. E. 3.1 (a) to measure I_B^- (inverting input bias current) and Fig. E. 3.1 (b) to measure I_B^+ (non-inverting input bias current). Select a large resistor (in MΩ) and measure the output voltage. Calculate $I_B^- = V_o/R_f$ and $I_B^+ = V_o R$.

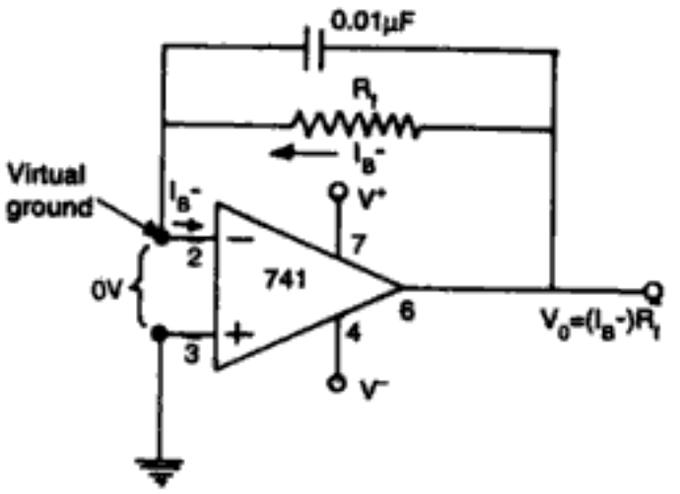

Fig. E.3.1 (a) Measurement of inverting input bias current

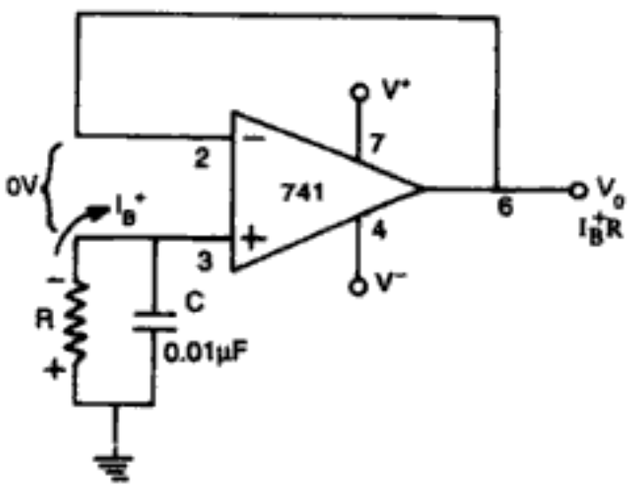

Fig. E. 3.1 (b) Measurement of non-inverting input bias current

(b) Offset current may be measured by the circuit shown in Fig. E.3.1 (c). The use of the equal resistors cancel the effect of the bias current. The offset current $I_{os} = V_o/R_f$.

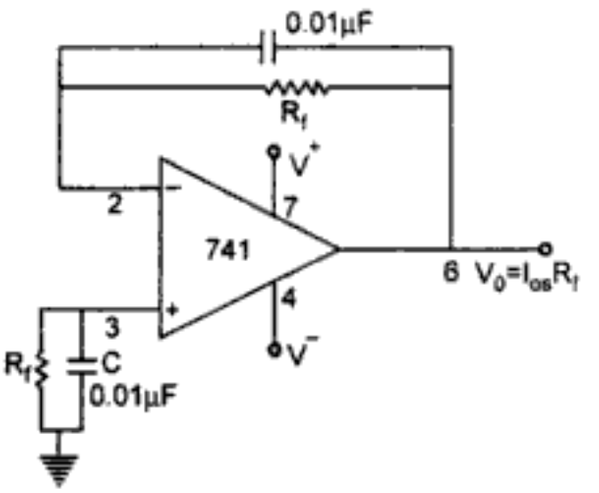

Fig. E. 3.1 (c) Offset current measurement

(c) To measure input offset voltage, set up the circuit shown in Fig. E. 3.1 (d). The effect of the bias current is compensated by R_{comp}. The output voltage is given by,

$$V_o = \left(1 + \frac{R_f}{R_1}\right) V_{os} + I_{os} R_f$$

$$\simeq \left(1 + \frac{R_f}{R_1}\right) V_{os}$$

The value of V_{os}, so obtained gives typically 98 percent accuracy.

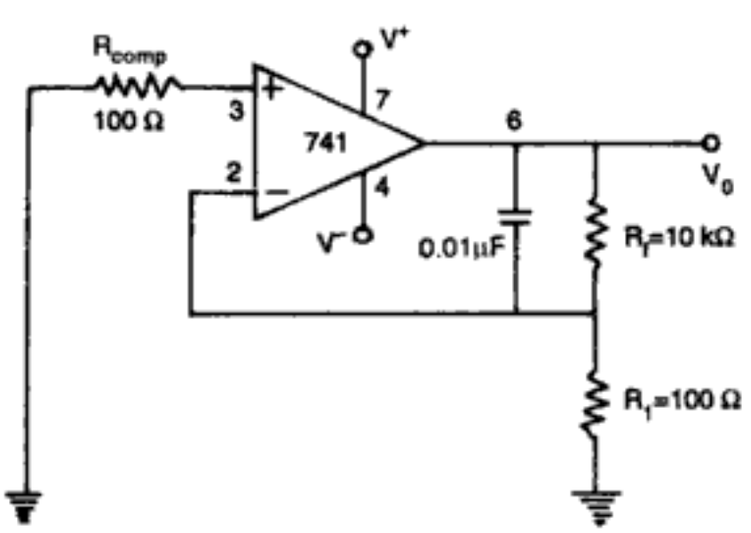

Fig. E.3.1 (d) Offset voltage measurement

Experiment 3.2

To measure the slew rate of the 741C op-amp.

Procedure

1. Connect the op-amp as shown in Fig. E.3.2.

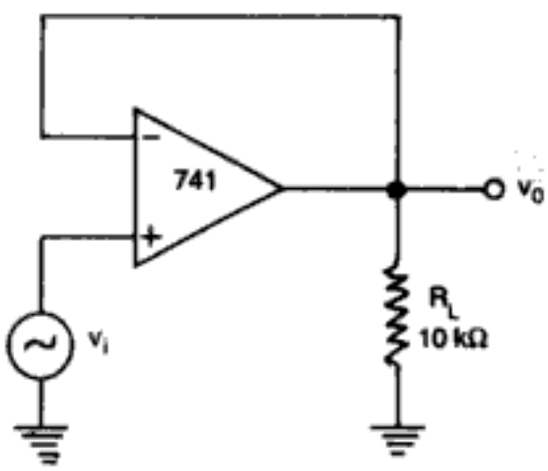

Fig. E. 3.2 Voltage follower to measure slew rate

2. Adjust the input sine-wave signal generator so that the output is 1 V peak sine wave at 1 kHz.
3. Slowly increase the input signal frequency until the output gets just distorted.
4. Calculate slew rate, $SR = \frac{2\pi f V_m}{10^6}$ V/μs where V_m = peak output amplitude in volts and f = frequency in Hz.
5. Now give a square-wave input and repeat step 2.
6. Increase the input frequency slowly until the output is just barely a triangular wave. The slew rate,

$$SR = \frac{\Delta v_o}{\Delta t} \text{ V/μs}$$

where, Δv_o = change in the output voltage amplitude in volts.
Δt = time required for Δv_o in μs.

4

Operational Amplifier Applications

4.1 INTRODUCTION

We have already discussed the electronics of op-amp, its dc and ac characteristics, parameter limitations and various configurations. Now we take a look at the applications of an op-amp. As we shall see, op-amp has countless applications and forms the basic building block of linear and non-linear analog systems. In linear circuits, the output signal varies with the input signal in a linear manner. Some of the linear applications discussed in this chapter are: adder, subtractor, voltage to current converter and current to voltage converter, instrumentation amplifier, analog computation, power amplifier etc.

There is another class of circuits with highly non-linear input to output characteristics. Rectifier, peak detector, clipper, clamper, sample and hold circuit, log and antilog amplifier, multiplier are the various non-linear circuits discussed. These non-linear circuits are very useful in industrial instrumentation, communication and general signal processing.

4.2 BASIC OP-AMP APPLICATIONS

Scale Changer/Inverter

In the basic inverting amplifier of Fig. 4.1, if the ratio $R_f/R_1 = K$, where K is a real constant, then the closed loop gain $A_{CL} = -K$. The circuit thus could be used to multiply by a constant factor if R_f and R_1 are selected as precision resistors. For $R_f = R_1$, $A_{CL} = -1$ and the circuit is called an inverter, i.e., the output is 180° out of phase with respect to input though the magnitudes are same.

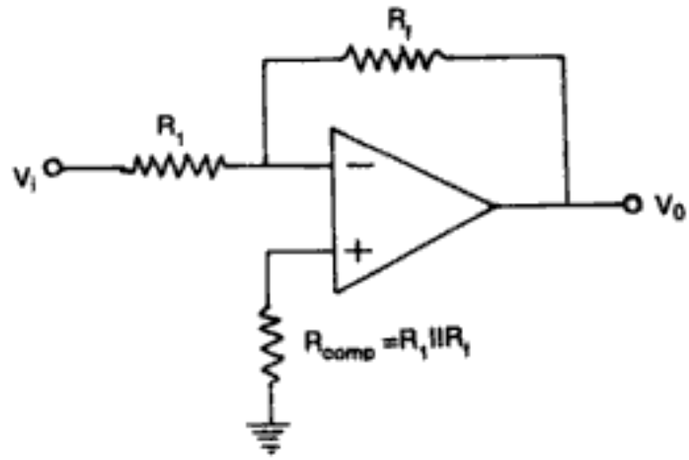

Fig. 4.1 Scale changer for ($R_f/R_1 = K$) and phase inverter for ($R_f/R_1 = 1$)

Summing Amplifier

Op-amp may be used to design a circuit whose output is the sum of several input signals. Such a circuit is called a summing amplifier or a summer. An inverting summer or a non-inverting summer may be obtained as discussed now.

Inverting Summing Amplifier

A typical summing amplifier with three input voltages V_1, V_2 and V_3, three input resistors R_1, R_2, R_3 and a feedback resistor R_f is shown in Fig. 4.2 (a). The following analysis is carried out assuming that the op-amp is an ideal one, that is, $A_{OL} = \infty$ and $R_i = \infty$. Since the input bias current is assumed to be zero, there is no voltage drop across the resistor R_{comp} and hence the non-inverting input terminal is at ground potential.

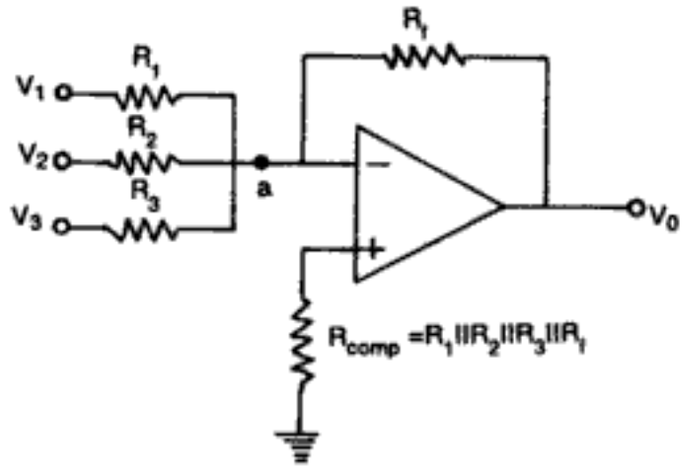

Fig. 4.2 (a) Inverting summing amplifier

The voltage at node 'a' is zero as the non-inverting input terminal is grounded. The nodal equation by KCL at node 'a' is

$$\frac{V_1}{R_1}+\frac{V_2}{R_2}+\frac{V_3}{R_3}+\frac{V_o}{R_f}=0$$

or,
$$V_o=-\left(\frac{R_f}{R_1}V_1+\frac{R_f}{R_2}V_2+\frac{R_f}{R_3}V_3\right) \tag{4.1}$$

Thus the output is an inverted, weighted sum of the inputs. In the special case, when $R_1 = R_2 = R_3 = R_f$, we have

$$V_o=-(V_1+V_2+V_3) \tag{4.2}$$

in which case the output V_o is the inverted sum of the input signals. We may also set

$$R_1 = R_2 = R_3 = 3R_f$$

in which case

$$V_o=-\left(\frac{V_1+V_2+V_3}{3}\right) \tag{4.3}$$

Thus the output is the average of the input signals (inverted). In a practical circuit, input bias current compensating resistor R_{comp} should be provided as discussed in Sec. 3.2.1. To find R_{comp}, make all inputs $V_1 = V_2 = V_3 = 0$. So the effective input resistance $R_i = R_1 \| R_2 \| R_3$. Therefore, $R_{comp} = R_i \| R_f = R_1 \| R_2 \| R_3 \| R_f$.

Example 4.1

Design an adder circuit using an op-amp to get the output expression as

$$V_o=-(0.1\ V_1+V_2+10\ V_3)$$

where V_1, V_2, and V_3 are the inputs.

Solution

The output in Fig. 4.2 (a) is

$$V_o=-[(R_f/R_1)\ V_1+(R_f/R_2)V_2+(R_f/R_3)V_3]$$

say
$$R_f = 10\ \text{k}\Omega,\ R_1 = 100\ \text{k}\Omega,\ R_2 = 10\ \text{k}\Omega,\ R_3 = 1\ \text{k}\Omega$$

Then the desired output expression is obtained.

Non-inverting Summing Amplifier

A summer that gives a non-inverted sum is the non-inverting summing amplifier of Fig. 4.2 (b). Let the voltage at the (–) input terminal be V_a. The voltage at (+) input terminal will also be V_a. The nodal equation at node 'a' is given by

$$\frac{V_1-V_a}{R_1}+\frac{V_2-V_a}{R_2}+\frac{V_3-V_a}{R_3}=0$$

from which we have,

$$V_a = \frac{\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}} \tag{4.4}$$

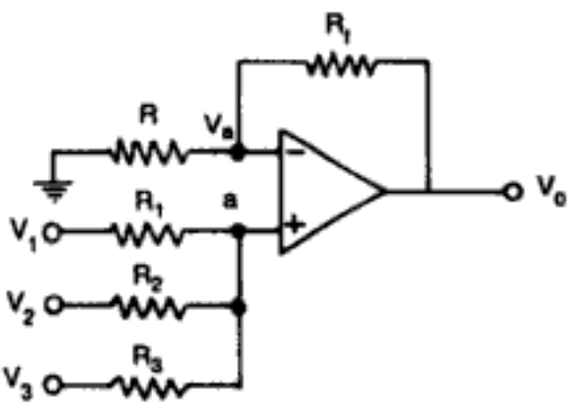

Fig. 4.2 (b) Noninverting summing amplifier

The op-amp and two resistors R_f and R constitute a non-inverting amplifier with

$$V_o = \left(1 + \frac{R_f}{R}\right) V_a \tag{4.5}$$

Therefore, the output voltage is,

$$V_o = \left(1 + \frac{R_f}{R}\right) \frac{\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}} \tag{4.6}$$

which is a non-inverted weighted sum of inputs.

Let $R_1 = R_2 = R_3 = R = R_f/2$, then $V_o = V_1 + V_2 + V_3$

Subtractor

A basic differential amplifier can be used as a subtractor as shown in Fig. 4.3 (a). If all resistors are equal in value, then the output voltage can be derived by using superposition principle. To find the output V_{o1} due to V_1 alone, make $V_2 = 0$. Then the circuit of Fig. 4.3 (a) becomes a non-inverting amplifier having input voltage $V_1/2$ at the non-inverting input terminal and the output becomes

$$V_{o1} = \frac{V_1}{2}\left(1 + \frac{R}{R}\right) = V_1 \tag{4.7}$$

Similarly the output V_{o2} due to V_2 alone (with V_1 grounded) can be written simply for an inverting amplifier as

$$V_{o2} = -V_2 \tag{4.8}$$

Thus the output voltage V_o due to both the inputs can be written as

$$V_o = V_{o1} + V_{o2} = V_1 - V_2 \tag{4.9}$$

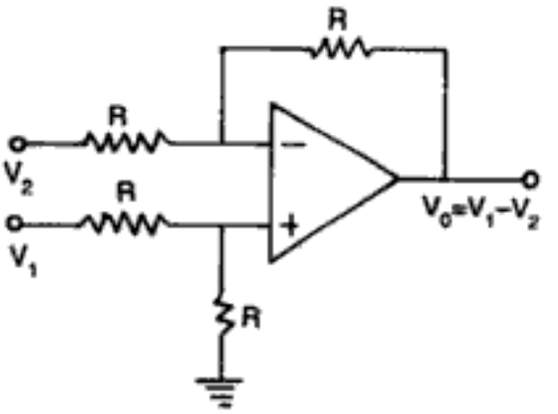

Fig. 4.3 (a) Op-amp as subtractor

Adder-Subtractor

It is possible to perform addition and subtraction simultaneously with a single op-amp using the circuit shown in Fig. 4.3 (b).

The output voltage V_o can be obtained by using superposition theorem. To find output voltage V_{o1} due to V_1 alone, make all other input voltages V_2, V_3 and V_4 equal to zero. The simplified circuit is shown in Fig. 4.3 (c). This is the circuit of an inverting amplifier and its output voltage is,

$$V_{o1} = -\frac{R}{R/2}\frac{V_1}{2} = -V_1 \tag{4.10}$$

(by Thevenin's equivalent circuit at inverting input terminal).

Similarly, the output voltage V_{o2} due to V_2 alone is,

$$V_{o2} = -V_2 \tag{4.11}$$

Now, the output voltage V_{o3} due to the input voltage signal V_3 alone applied at the (+) input terminal can be found by setting V_1, V_2 and V_4 equal to zero. The circuit now becomes a non-inverting amplifier as shown in Fig. 4.3 (d). The voltage V_a at the non-inverting terminal is

$$V_a = \frac{R/2}{R + R/2} V_3 = V_3/3 \tag{4.12}$$

So, the output voltage V_{o3} due to V_3 alone is

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Therefore,

$$A_{CL} = \frac{V_o}{V_i} = -\frac{R_f}{R_1}\frac{s}{s + 1/R_1C} \tag{4.24}$$

It is seen from Eq. (4.24) that the lower 3dB frequency is,

$$f_L = \frac{1}{2\pi R_1 C} \tag{4.25}$$

In the mid-band range of frequencies, capacitor C behaves as a short circuit and therefore, Eq. (4.24) becomes,

$$A_{CL} = -\frac{R_f}{R_1} \tag{4.26}$$

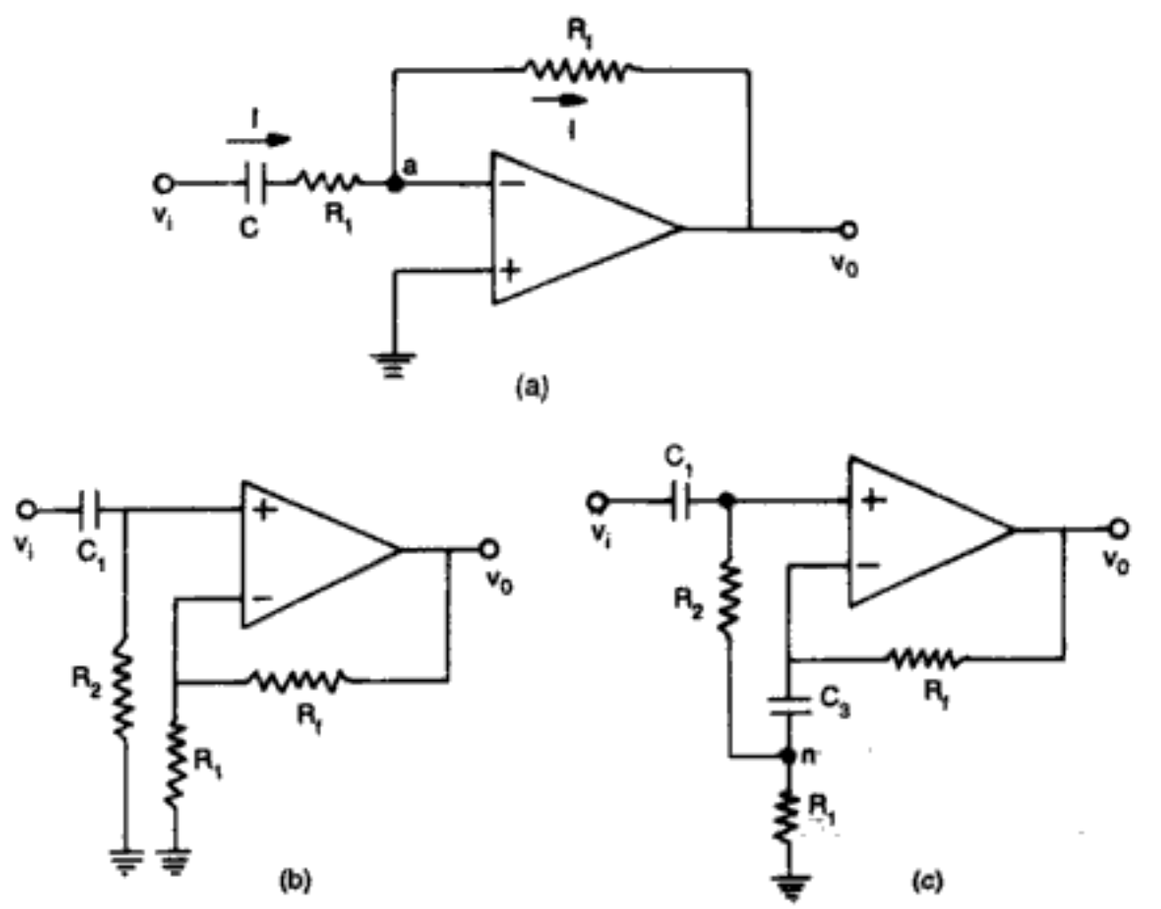

Fig. 4.6 (a) Inverting ac amplifier (b) Non-inverting ac amplifier (c) High input impedance noninverting ac amplifier

Non-inverting AC Amplifier

The circuit is shown in Fig. 4.6 (b). Here a resistor R_2 is added to provide a dc return to ground. However, this reduces the overall input impedance of the amplifier, which now becomes approximately R_2. This problem of low input impedance is eliminated by connecting

a capacitor C_3 as in Fig. 4.6 (c). Capacitor C_3 is large enough to act as short circuit to ac signals. The non-inverting terminal and the node 'n' will be almost at the same potential so that R_2 carries almost no current. Hence the circuit will have an extremely high input impedance.

AC Voltage Follower

The circuit of a practical ac voltage follower is shown in Fig. 4.7. The circuit is used as a buffer to connect a high impedance signal source to a low impedance load which may even be capacitive. The capacitor C_1 and C_2 are chosen high so that they are short circuit at all frequencies of operation. Resistors R_1 and R_2 provide a path for dc input current into the non-inverting terminal. C_2 acts as a bootstrapping capacitor and connects the resistance R_1 to the output terminal for ac operation. Hence the input resistance that the source sees is approximately $R_1/(1 - A_{CL})$ [from Miller's theorem] where A_{CL} is the gain of the voltage follower which is close to unity (0.9997). Thus very high input impedance can be obtained.

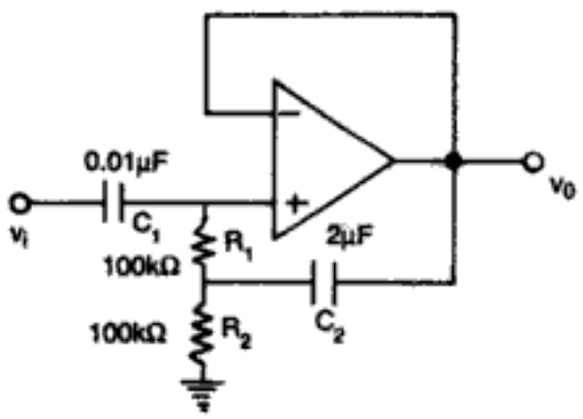

Fig. 4.7 AC voltage follower

4.5 *V* TO *I* AND *I* TO *V* CONVERTER

Voltage to Current Converter (Transconductance Amplifier)

In many applications, one may have to convert a voltage signal to a proportional output current. For this, there are two types of circuits possible.

V-I Converter with floating load
V-I Converter with grounded load

Figure 4.8 (a) shows a voltage to current converter in which load Z_L is floating. Since voltage at node 'a' is v_i, therefore,

$$v_i = i_L R_1 \qquad (\text{as } I_B^- = 0)$$

or, $$i_L = \frac{v_i}{R_1} \tag{4.27}$$

That is the input voltage v_i is converted into an output current of v_i/R_1. It may be seen that the same current flows through the signal source and load and, therefore, signal source should be capable of providing this load current.

A voltage-to-current converter with grounded load is shown in Fig. 4.8 (b). Let v_1 be the voltage at node 'a'. Writing KVL, we get

$$i_1 + i_2 = i_L \tag{4.28}$$

or, $$\frac{v_i - v_1}{R} + \frac{v_o - v_1}{R} = i_L$$

or, $$v_i + v_o - 2v_1 = i_L R$$

Therefore, $$v_1 = \frac{v_i + v_o - i_L R}{2} \tag{4.29}$$

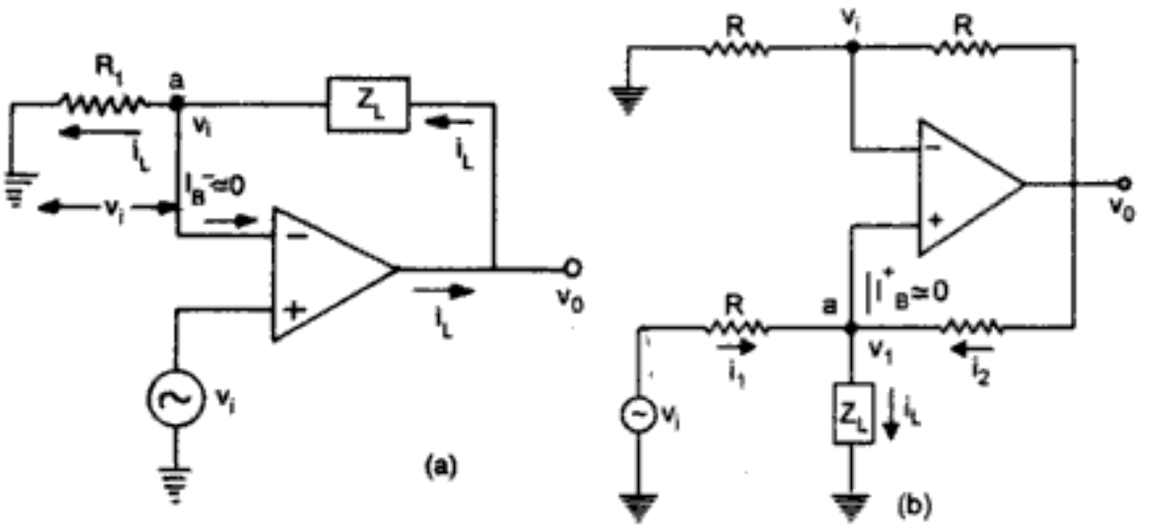

Fig. 4.8 Voltage to current converter with (a) floating load (b) grounded load

Since the op-amp is used in non-inverting mode, the gain of the circuit is $1 + R/R = 2$. The output voltage is,

$$v_o = 2v_1 = v_i + v_o - i_L R$$

that is, $$v_i = i_L R$$

or, $$i_L = \frac{v_i}{R} \tag{4.30}$$

As the input impedance of a non-inverting amplifier is very high, this circuit has the advantage of drawing very little current from the source. A voltage to current converter is used for low voltage dc and ac voltmeter, LED and zener diode tester.

Current to Voltage Converter (Transresistance Amplifier)

Photocell, photodiode and photovoltaic cell give an output current that is proportional to an incident radiant energy or light. The current through these devices can be converted to voltage by using a current-to-voltage converter and thereby the amount of light or radiant energy incident on the photo-device can be measured.

Figure 4.9. shows an op-amp used as I to V converter. Since the (–) input terminal is at virtual ground, no current flows through R_s and current i_s flows through the feedback resistor R_f. Thus the output voltage $v_o = -i_s R_f$. It may be pointed out that the lowest current that this circuit can measure will depend upon the bias current I_B of the op-amp. This means that μA741 (I_B = 3 nA) can be used to detect lower currents. The resistor R_f is sometimes shunted with a capacitor C_f to reduce high frequency noise and the possibility of oscillations.

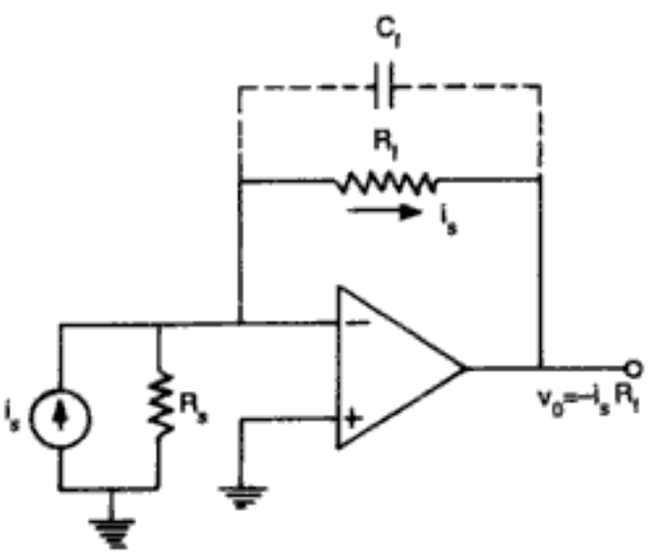

Fig. 4.9 Current to voltage converter

4.6 OP-AMP CIRCUITS USING DIODES

The major limitation of ordinary diode is that it cannot rectify voltages below V_γ (~ 0.6 V), the cut-in voltage of the diode. A circuit that acts like an ideal diode can be designed by placing a diode in the feedback loop of an op-amp as in Fig. 4.10 (a). Here the cut-in voltage is divided by the open loop gain A_{OL} (~ 10^4) of the op-amp so that V_γ is virtually eliminated. When the input $v_i > V_\gamma/A_{OL}$ then v_{oA}, the output of the op-amp exceeds V_γ and the diode D conducts. Thus the circuit acts like a voltage follower for input $v_i > V_\gamma/A_{OL}$ (i.e., $0.6/10^4$ = 60 μV) and the output v_o follows the input voltage v_i during the positive half cycle as shown in Fig. 4.10 (b). When v_i is negative or less than V_γ/A_{OL}, the diode D is ***off*** and no current is delivered to the load R_L except for

small bias current of the op-amp and the reverse saturation current of the diode. This circuit is called the precision diode and is capable of rectifying input signals of the order of millivolt. Some typical applications of a precision diode discussed are:

Half-wave rectifier
Full-wave rectifier
Peak-value detector
Clipper
Clamper

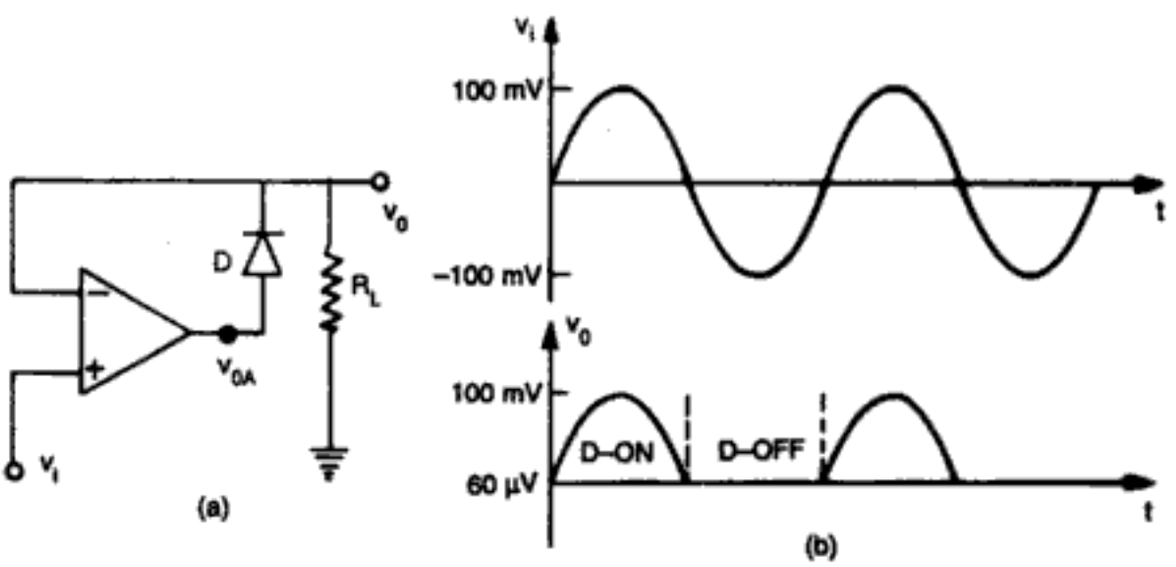

Fig. 4.10 (a) Precision diode (b) Input and output waveforms

4.6.1 Half-Wave Rectifier

An inverting amplifier can be converted into an idea half-wave rectifier by adding two diodes as shown in Fig. 4.11 (a). When v_i is positive, diode D_1 conducts causing v_{OA} to go to negative by one diode drop (~ 0.6 V). Hence diode D_2 is reverse biased. The output voltage v_o is zero, because, for all practical purposes, no current flows through R_f and the input current flows through D_1.

For negative input, i.e., $v_i < 0$, diode D_2 conducts and D_i is ***off***. The negative input v_i forces the op-amp output v_{OA} positive and causes D_2 to conduct. The circuit then acts like an inverter for $R_f = R_1$ and output v_o becomes positive.

The input, output waveforms are shown in Fig. 4.11 (b). The op-amp in the circuit of Fig. 4.11 (a) must be a high speed op-amp since it alternates between open loop and closed loop operations. The principal limitation of this circuit is the slew rate of the op-amp. As the input passes through zero, the op-amp output v_{oA} must change from 0.6 V to – 0.6 V or vice-versa as quickly as possible in order to switch over the conduction from one diode to the other.

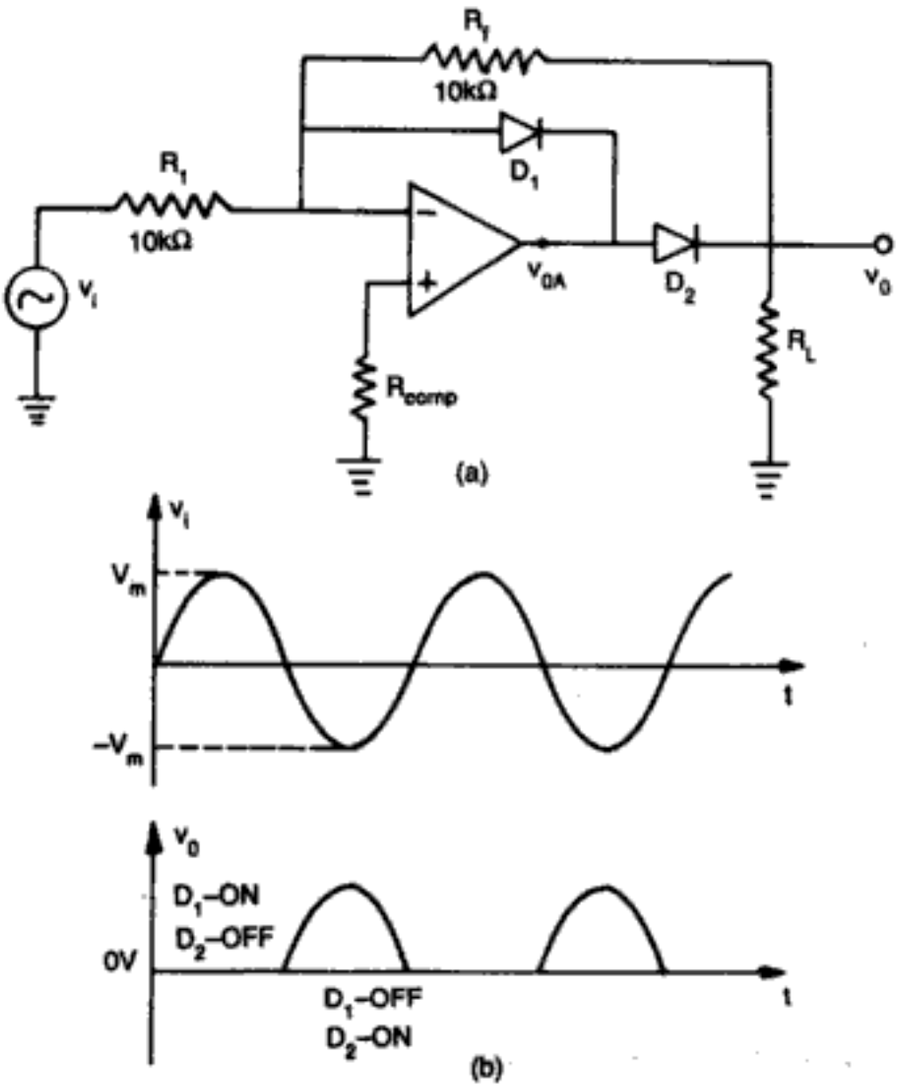

Fig. 4.11 (a) Ideal half-wave rectifier (b) Input/output waveforms

4.6.2 Full-wave Rectifier

A full wave rectifier or absolute value circuit is shown in Fig. 4.12 (a). For positive input, i.e. $v_i > 0$, diode D_1 is ***on*** and D_2 is ***off***. Both the op-amps A_1 and A_2 act as inverter as shown in equivalent circuit in Fig. 4.12 (b). It can be seen that $v_o = v_i$.

For negative input, i.e. $v_i < 0$, diode D_1 is ***off*** and D_2 is ***on***. The equivalent circuit is shown in Fig. 4.12 (c). Let the output voltage of op-amp A_1 be v. Since the differential input to A_2 is zero, the inverting input terminal is also at voltage v.

KCL at node 'a' gives

$$\frac{v_i}{R} + \frac{v}{2R} + \frac{v}{R} = 0$$

or

$$v = -\frac{2}{3} v_i \tag{4.31}$$

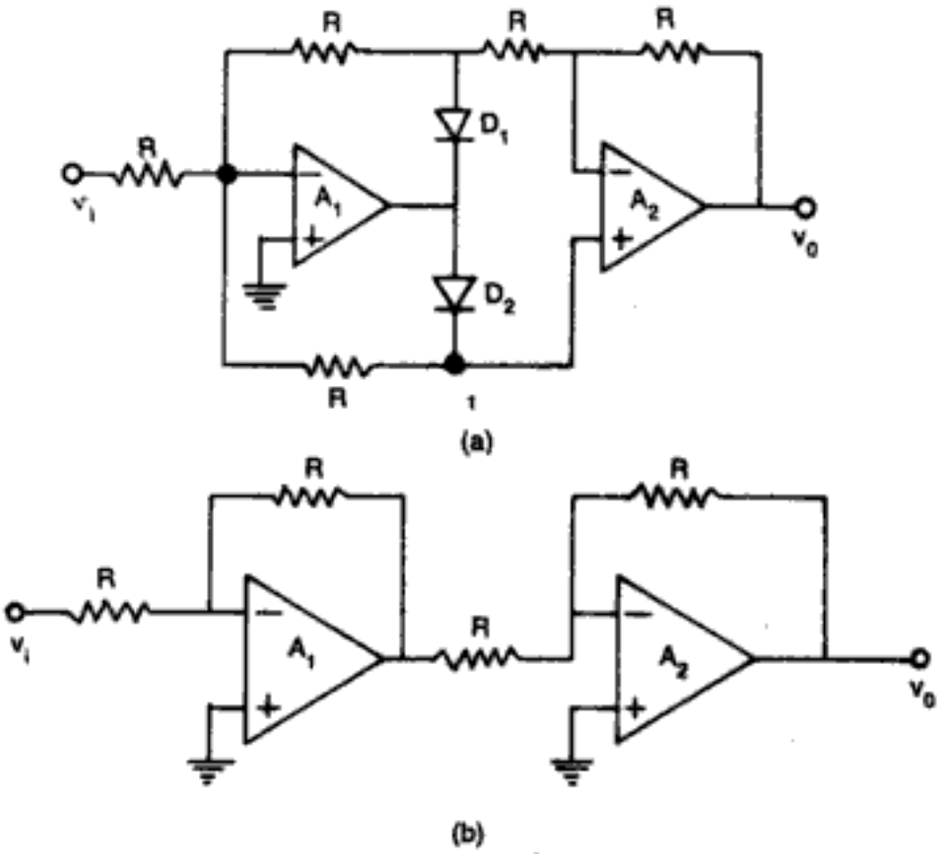

Fig. 4.12 (a) Precision full wave rectifier (b) Equivalent circuit for $v_i > 0$

The equivalent circuit of Fig. 4.12 (c) is a non-inverting amplifier as shown in Fig. 4.12 (d). The output v_o is,

$$v_o = \left(1 + \frac{R}{2R}\right)\left(-\frac{2}{3}v_i\right) = v_i \tag{4.32}$$

Hence for $v_i < 0$, the output is positive. The input and output waveforms are shown in Fig. 4.12 (e).

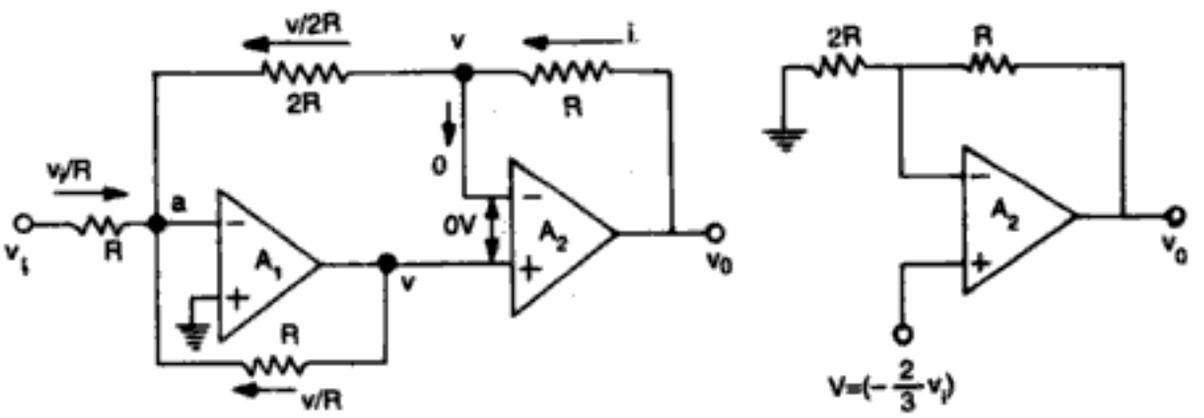

Fig. 4.12 (c) Equivalent circuit for $v_i < 0$ (d) Equivalent circuit of (c)

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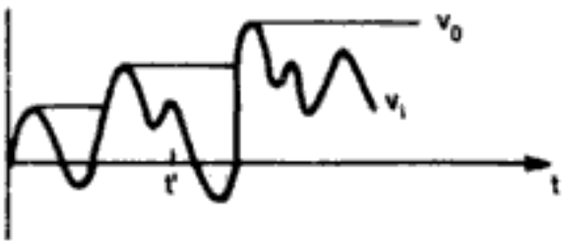

Fig. 4.13 (b) Output v_0 corresponding to arbitrary input v_i

4.6.4 Clipper

A precision diode may also be used to clip-off a certain portion of the input signal to obtain a desired output waveform.

Figure 4.14 (a) shows a positive clipper. The clipping level is determined by the reference voltage V_{ref} and could be obtained from the positive supply voltage V^+. The input and output waveforms are shown in Fig. 4.14 (b). It can be seen that the portion of the output voltage for $v_o > V_{ref}$ are clipped off.

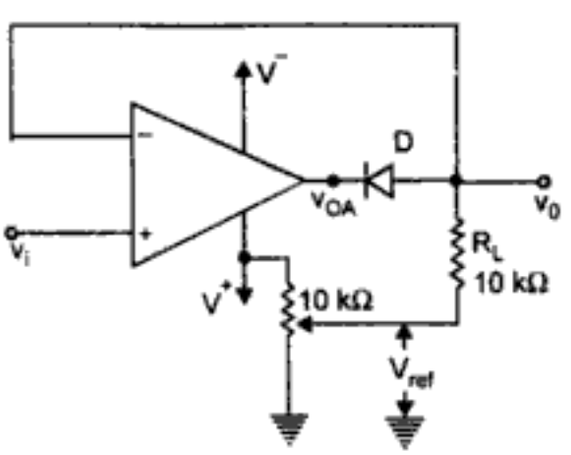

Fig. 4.14 (a) Positive clipper circuit

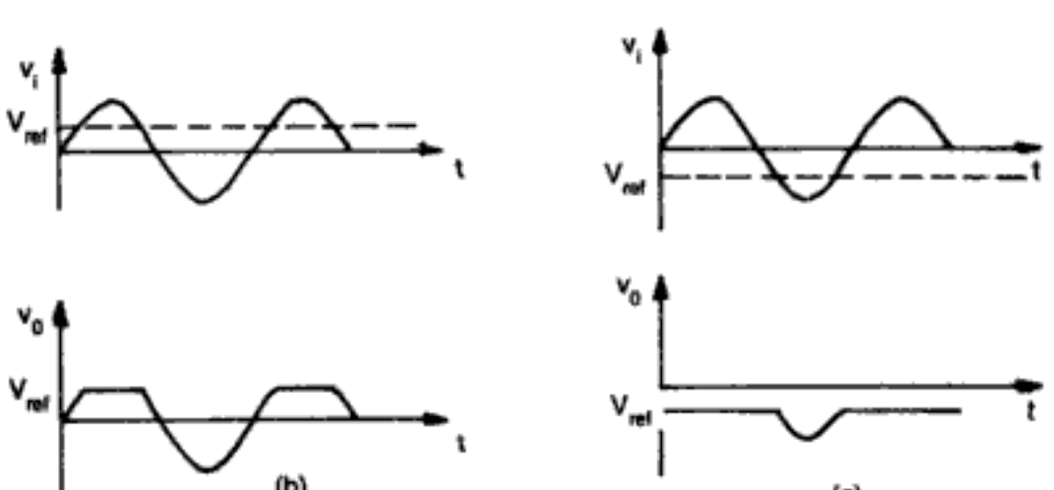

Fig. 4.14 Input and output waveforms for (b) positive V_{ref} (c) Negative V_{ref}

For input voltage $v_i < V_{ref}$, diode D conducts. The op-amp works as a voltage follower and output v_o follows input v_i till $v_i \leq V_{ref}$. When v_i is greater than V_{ref}, the output v_{oA} of the op-amp is large enough of drive D into cut-off. The op-amp operates in the open-loop and output voltage $v_o = V_{ref}$. However, if V_{ref} is made negative, then the entire output waveform above V_{ref} will get clipped off as shown in fig. 4.14 (c).

The positive clipper of Fig. 4.14. (a) can be easily converted into a negative clipper by simply reversing diode D and changing the polarity of the reference voltage V_{ref} as shown in Fig. 4.15 (a). The negative clipper clips off the negative parts of the input signal below the reference voltage. The circuit diagram of a negative clipper and the expected waveforms for negative V_{ref} and positive V_{ref} are shown in Fig. 4.15 (b and c).

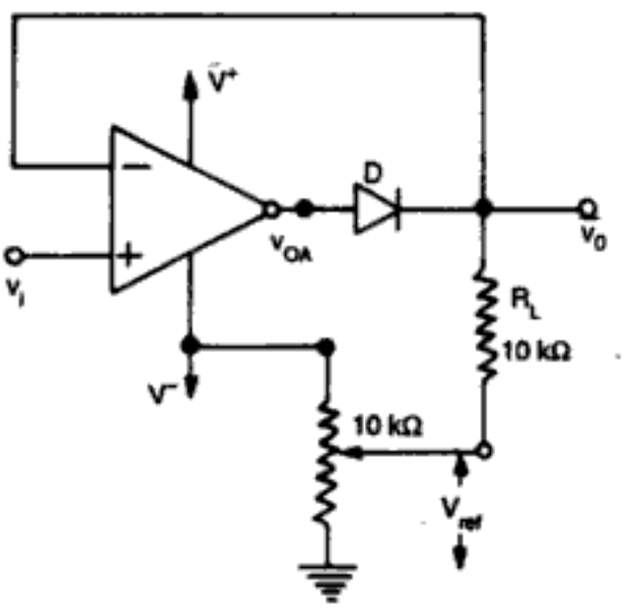

Fig. 4.15 (a) Negative clipper circuit

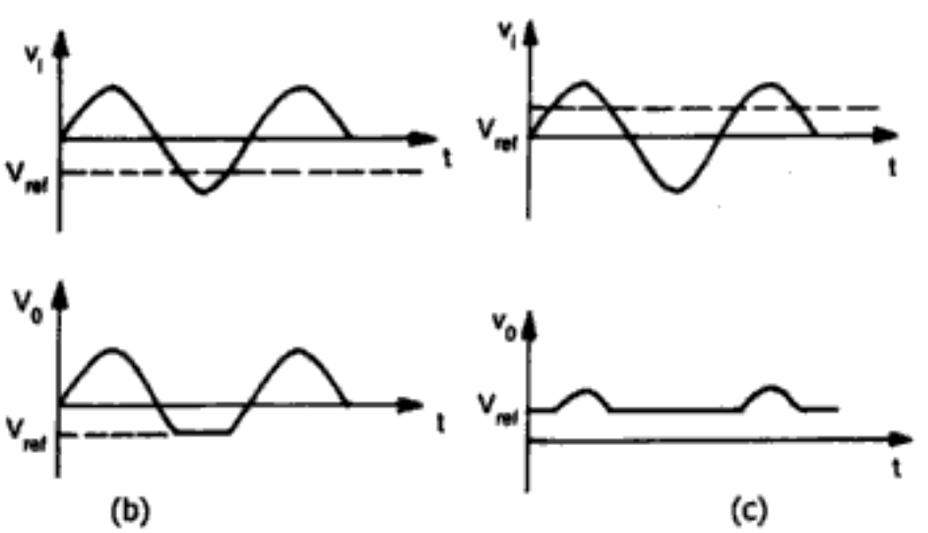

Fig. 4.15 (b, c) Input-output waveforms for negative and positive V_{ref}

4.6.6 Clamper

The clamper is also known as dc inserter or restorer. The circuit is used to add a desired dc level to the output voltage. In other words, the output is clamped to a desired dc level. If the clamped dc level is positive, it is called positive clamper. Similarly if the clamped dc level is negative, the clamper is called negative clamper.

Figure 4.16 (a) shows a clamper with a variable positive dc voltage applied at the (+) input terminal. This circuit clamps the peaks of the input waveform and therefore is also called a peak clamper. The output voltage in the circuit is the net result of ac and dc input voltages applied to the (–) and (+) input terminals respectively. Let us first see the effect of V_{ref} applied at the (+) input terminal. For positive V_{ref}, the voltage v' is also positive, so that the diode D is forward biased. The circuit operates as a voltage follower and therefore output voltage $v_o = + V_{ref}$.

Now consider the ac input signal $v_i = V_m \sin \omega t$ applied at the (–) input terminal. During the negative half cycle of v_i, diode D conducts. The capacitor C_1 charges through diode D to the negative peak voltage V_m. However, during the positive half cycle of v_i, diode D is reverse biased. The capacitor retains its previous voltage V_m. Since this voltage V_m is in series with the ac input signal, the output voltage now will be $v_i + V_m$. The total output voltage is, therefore,

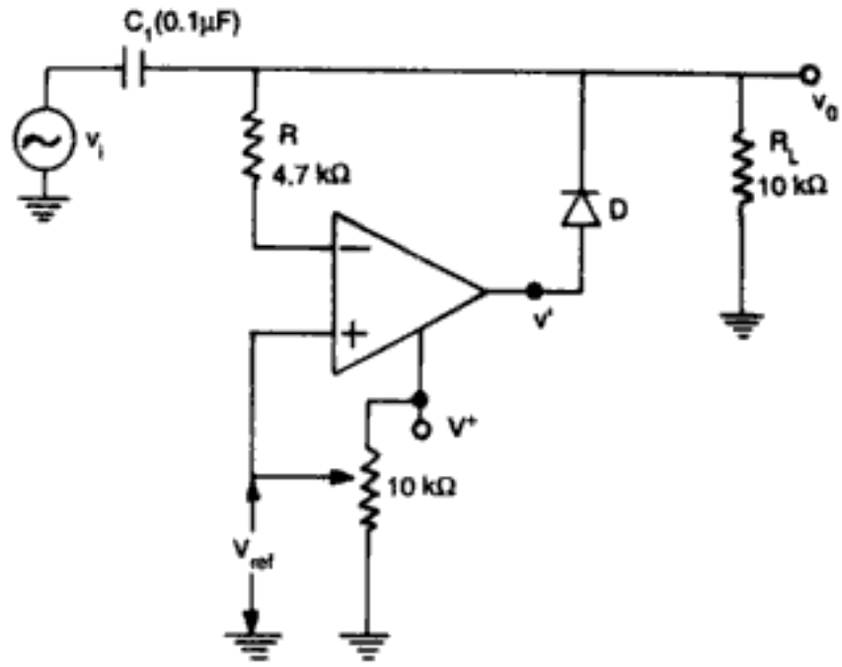

Fig. 4.16 (a) Peak clamper circuit

$V_{ref} + v_i + V_m$. The input and output waveforms are shown in Fig. 4.16 (b). It is possible to obtain negative peak clamping by reversing the diode D and using a negative reference voltage $-V_{ref}$. The expected waveforms are shown in Fig. 4.16 (c). The resistor R is used for

protecting the op-amp against excessive discharge currents from capacitor C_1 especially when the dc supply voltages are switched off.

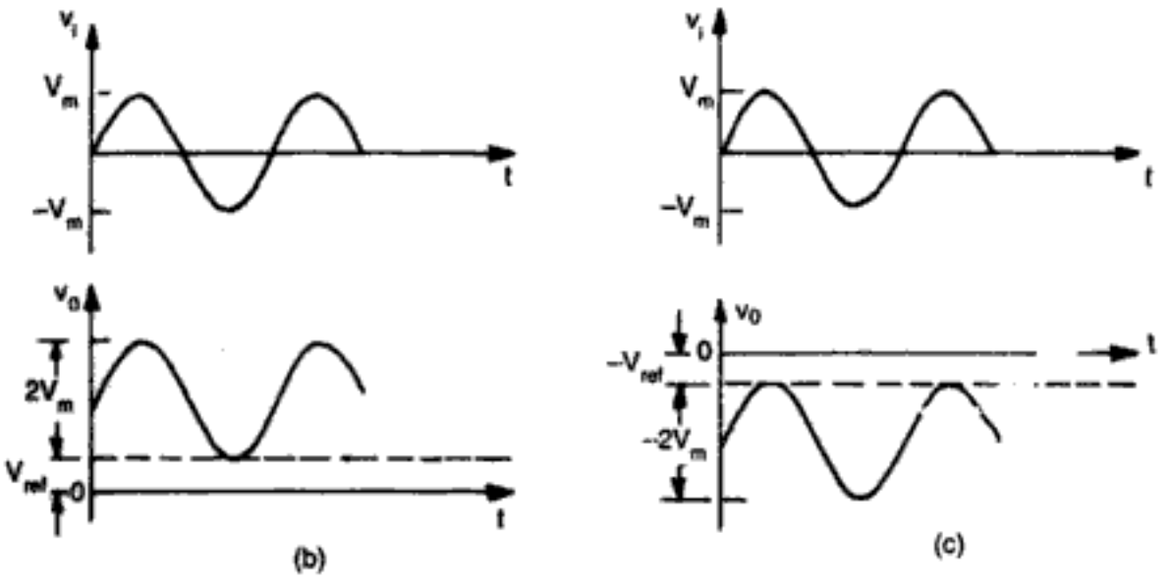

Fig. 4.16 (b) Waveforms for + V_{ref} (c) Waveforms for – V_{ref}

4.7 SAMPLE AND HOLD CIRCUIT

A sample and hold circuit samples an input signal and holds on to its last sampled value until the input is sampled again. This type of circuit is very useful in digital interfacing and analog to digital and pulse code modulation systems. One of the simplest practical sample and hold circuit configuration is shown in Fig. 4.17 (a). The *n*-channel E-MOSFET works as a switch and is controlled by the control voltage v_c and the capacitor C stores the charge. The analog signal v_i to be

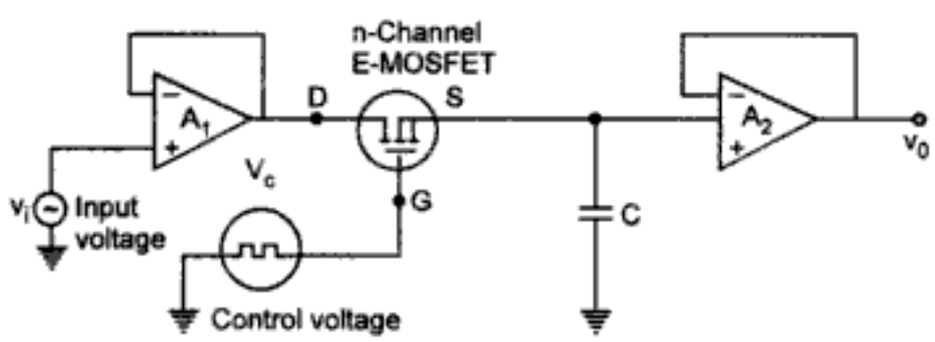

Fig. 4.17 (a) Sample and hold circuit

sampled is applied to the drain of E-MOSFET and the control voltage v_c is applied to its gate. When v_c is positive, the E-MOSFET turns ***on*** and the capacitor C charges to the instantaneous value of input v_i with a time constant $[(R_o + r_{DS}\ (\textit{on})]\ C$. Here R_o is the output resistance of the voltage follower A_1 and r_{DS} (***on***) is the resistance of the MOSFET

when ***on***. Thus the input voltage v_i appears across the capacitor C and then at the output through the voltage follower A_2. The waveforms are as shown in Fig. 4.17 (b).

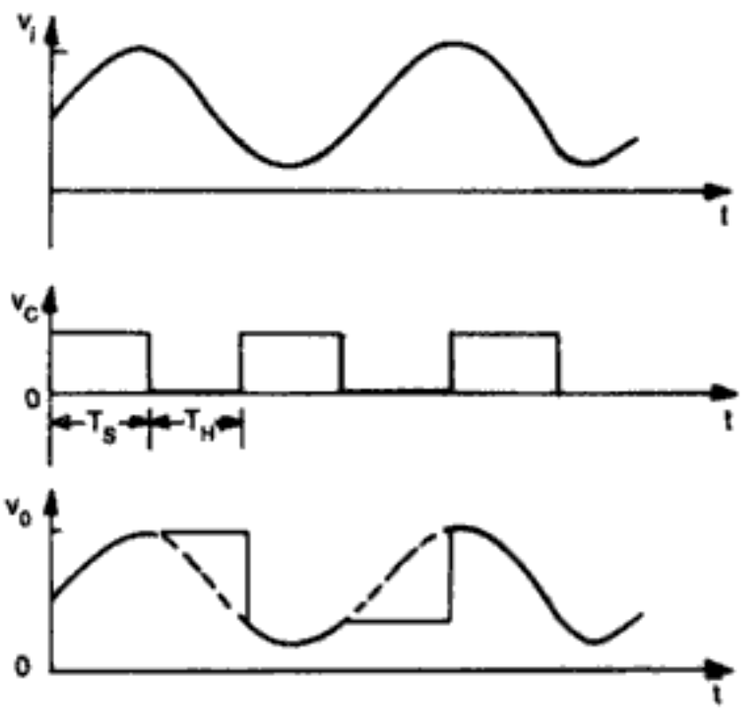

Fig. 4.17 (b) Input and output waveforms

During the time when control voltage v_c is zero, the E-MOSFET is ***off***. The capacitor C is now facing the high input impedance of the voltage follower A_2 and hence cannot discharge. The capacitor holds the voltage across it. The time period T_S, the time during which voltage across the capacitor is equal to input voltage is called sample period. The time period T_H of v_c during which the voltage across the capacitor is held constant is called hold period. The frequency of the control voltage should be kept higher than (at least twice) the input so as to retrieve the input from output waveform. A low leakage capacitor such as Polystyrene, Mylar, or Teflon should be used to retain the stored charge.

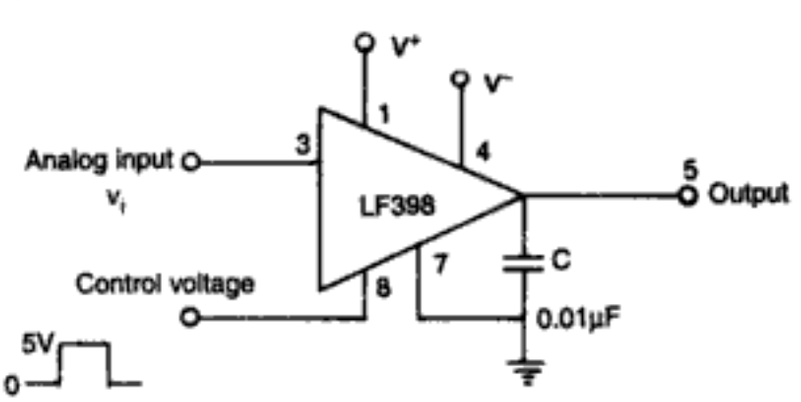

Fig. 4.17 (c) Typical connection diagram

Specially designed sample and hold ICs of make Harris semiconductor HA2420, National semiconductor such as LF198, LF398 are also available. A typical connection diagram of the LF398 is shown in Fig. 4.17 (c). It may be noted that the storage capacitor C is connected externally.

4.8 LOG AND ANTILOG AMPLIFIER

There are several applications of log and antilog amplifiers. Antilog computation may require functions such as ln x, log x or sinh x. These can be performed continuously with log-amps. One would like to have direct dB display on digital voltmeter and spectrum analyser. Log-amp can easily perform this function. Log-amp can also be used to compress the dynamic range of a signal.

Log Amplifier

The fundamental log-amp circuit is shown in Fig. 4.18 (a) where a grounded base transistor is placed in the feedback path. Since the collector is held at virtual ground and the base is also grounded, the transistor's voltage-current relationship becomes that of a diode and is given by,

$$I_E = I_s (e^{qV_E/kT} - 1) \tag{4.33}$$

Since, $I_C = I_E$ for a grounded base transistor,

$$I_C = I_s (e^{qV_E/kT} - 1) \tag{4.34}$$

I_s = emitter saturation current $\approx 10^{-13}$ A
k = Boltzmann's Constant
T = absolute temperature (in °K)

Therefore, $$\frac{I_C}{I_s} = (e^{q V_E/kT} - 1) \tag{4.35}$$

or, $$e^{q V_E/kT} = \frac{I_C}{I_s} + 1$$

$$\approx \frac{I_C}{I_s} \qquad [\text{as } I_s = 10^{-13} \text{ A}, I_C >> I_s]$$

Taking natural log on both sides, we get

$$V_E = \frac{kT}{q} \ln\left(\frac{I_C}{I_s}\right) \tag{4.36}$$

Also in Fig. 4.18 (a), $I_C = \frac{V_i}{R_1}$

$$V_E = -V_o$$

so,
$$V_o = -\frac{kT}{q}\ln\left(\frac{V_i}{R_1 I_s}\right) = -\frac{kT}{q}\ln\left(\frac{V_i}{V_{ref}}\right) \quad (4.37)$$

where
$$V_{ref} = R_1 I_s$$

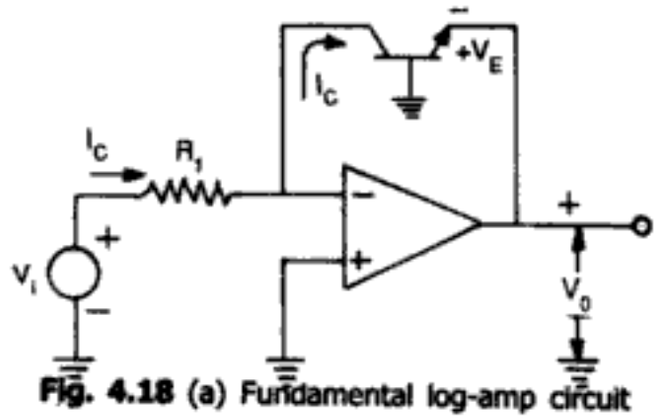

Fig. 4.18 (a) Fundamental log-amp circuit

The output voltage is thus proportional to the logarithm of input voltage. Although the circuit gives natural log (ln), one can find $\log_{10}$ by proper scaling

$$\log_{10} X = 0.4343 \ln X \quad (4.38)$$

The circuit, however, has one problem. The emitter saturation current I_s varies from transistor to transistor and with temperature. Thus a stable reference voltage V_{ref} cannot be obtained. This is eliminated by the circuit given in Fig. 4.18 (b). The input is applied to one log-amp, while a reference voltage is applied to another log-amp. The two transistors are integrated close together in the same silicon wafer. This provides a close match of saturation currents and ensures good thermal tracking.

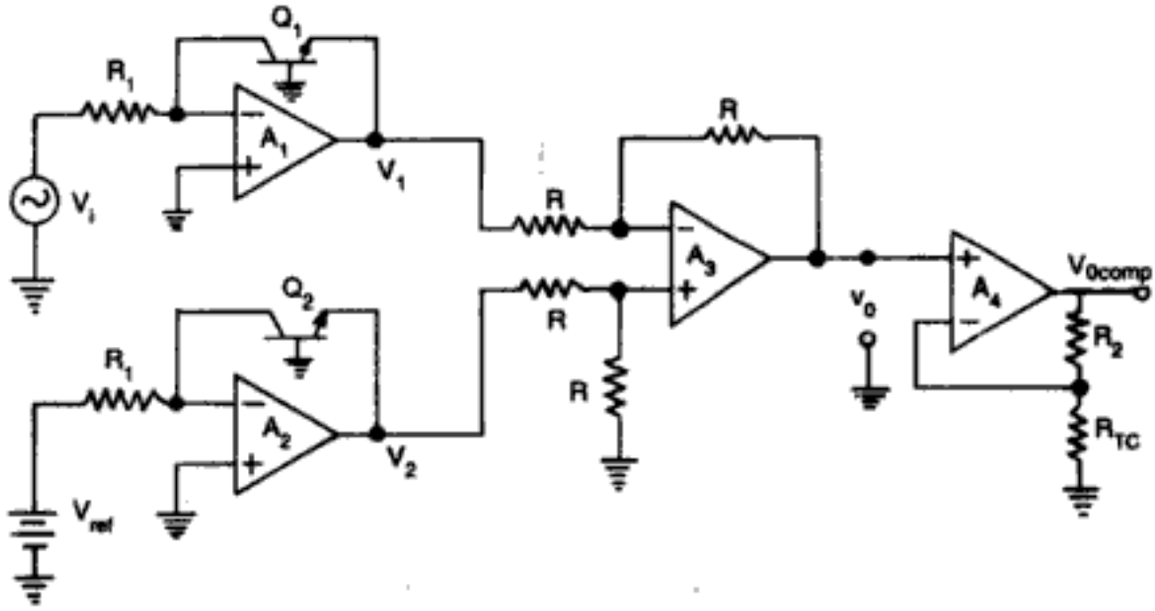

Fig. 4.18 (b) Log-amp with saturation current and temperature compensation

Assume, $$I_{s1} = I_{s2} = I_s \tag{4.39}$$

and then, $$V_1 = -\frac{kT}{q} \ln\left(\frac{V_i}{R_1 I_s}\right) \tag{4.40}$$

and $$V_2 = -\frac{kT}{q} \ln\left(\frac{V_{ref}}{R_1 I_s}\right) \tag{4.41}$$

Now, $$V_o = V_2 - V_1 = \frac{kT}{q}\left[\ln\left(\frac{V_i}{R_1 I_s}\right) - \ln\left(\frac{V_{ref}}{R_1 I_s}\right)\right] \tag{4.42}$$

or, $$V_o = \frac{kT}{q} \ln\left(\frac{V_i}{V_{ref}}\right) \tag{4.43}$$

Thus reference level is now set with a single external voltage source. Its dependence on device and temperature has been removed. The voltage V_o is still dependent upon temperature and is directly proportional to T. This is compensated by the last op-amp stage A_4 which provides a non-inverting gain of $(1 + R_2/R_{TC})$. Now, the output voltage is,

$$V_{o\ comp} = \left(1 + \frac{R_2}{R_{TC}}\right)\frac{kT}{q} \ln\left(\frac{V_i}{V_{ref}}\right) \tag{4.44}$$

where R_{TC} is a temperature-sensitive resistance with a positive coeffecient of temperature (sensistor) so that the slope of the equation becomes constant as the temperature changes.

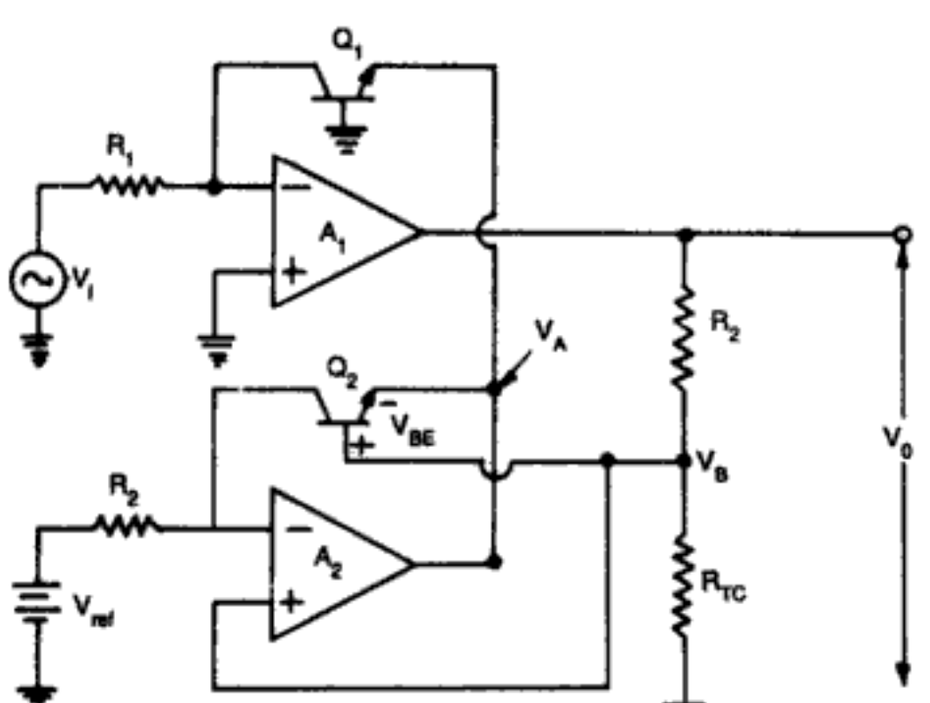

Fig. 4.18 (c) Log-amp using two op-amps only

The circuit in Fig. 4.18. (b) requires four op-amps, and becomes expensive if FET op-amps are used for precision. The same output (with an inversion) can be obtained by the circuit of Fig. 4.18 (c) using two op-amps only.

Antilog Amplifier

The circuit is shown in Fig. 4.19. The input V_i for the antilog-amp is fed into the temperature compensating voltage divider R_2 and R_{TC} and then to the base of Q_2. The output V_o of the antilog-amp is fed back to the inverting input of A_1 through the resistor R_1. The base to emitter voltage of transistors Q_1 and Q_2 can be written as

$$V_{Q1\ B\text{–}E} = \frac{kT}{q} \ln\left(\frac{V_o}{R_1 I_s}\right) \tag{4.45}$$

and

$$V_{Q2\ B\text{–}E} = \frac{kT}{q} \ln\left(\frac{V_{ref}}{R_1 I_s}\right) \tag{4.46}$$

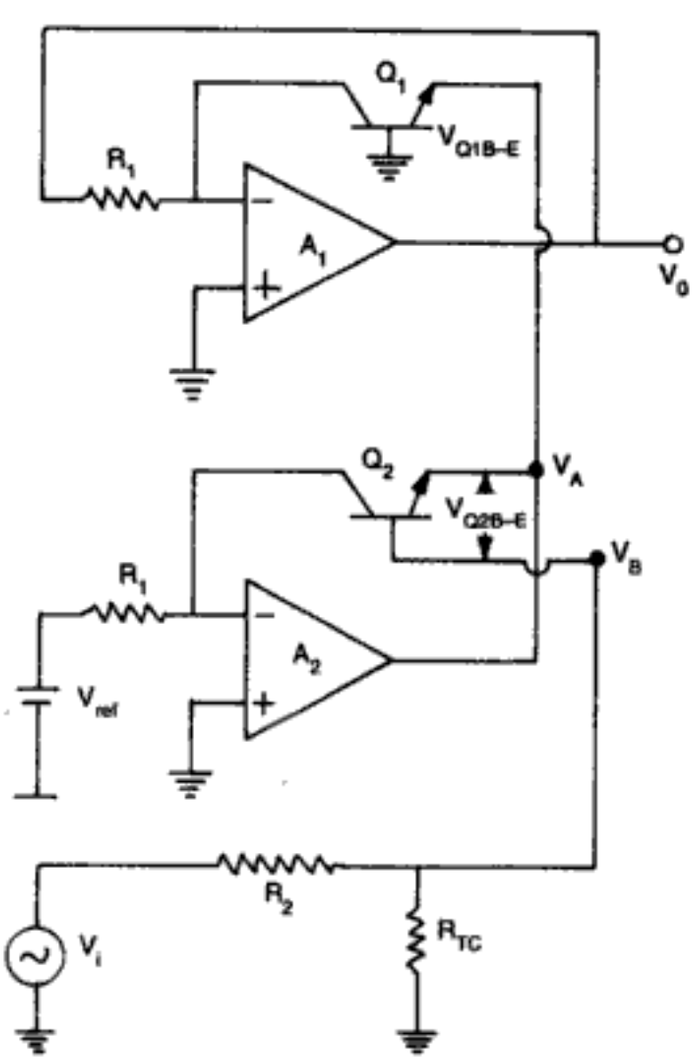

Fig. 4.19 Antilog amplifier

Since the base of Q_1 is tied to ground, we get

$$V_A = -V_{Q1\ B\text{-}E} = -\frac{kT}{q}\ln\left(\frac{V_o}{R_1 I_s}\right) \tag{4.47}$$

The base voltage V_B of Q_2 is

$$V_B = \left(\frac{R_{TC}}{R_2 + R_{TC}}\right)V_i \tag{4.48}$$

The voltage at the emitter of Q_2 is

$$V_{Q2\ E} = V_B + V_{Q2\ E\text{-}B}$$

or,
$$V_{Q2\ E} = \left(\frac{R_{TC}}{R_2 + R_{TC}}\right)V_i - \frac{kT}{q}\ln\left(\frac{V_{ref}}{R_1 I_s}\right) \tag{4.49}$$

But the emitter voltage of Q_2 is V_A, that is,

$$V_A = V_{Q2\ E}$$

or,
$$-\frac{kT}{q}\ln\frac{V_o}{R_1 I_s} = \frac{R_{TC}}{R_2 + R_{TC}}V_i - \frac{kT}{q}\ln\frac{V_{ref}}{R_1 I_s} \tag{4.50}$$

or,
$$\frac{R_{TC}}{R_2 + R_{TC}}V_i = -\frac{kT}{q}\left(\ln\frac{V_o}{R_1 I_s} - \ln\frac{V_{ref}}{R_1 I_s}\right)$$

or,
$$-\frac{q}{kT}\frac{R_{TC}}{R_2 + R_{TC}}V_i = \ln\left(\frac{V_o}{V_{ref}}\right) \tag{4.51}$$

Changing natural log, i.e., ln to $\log_{10}$ using Eq. (4.38) we get

$$-0.4343\left(\frac{q}{kT}\right)\left(\frac{R_{TC}}{R_2 + R_{TC}}\right)V_i = 0.4343 \times \ln\left(\frac{V_o}{V_{ref}}\right) \tag{4.52}$$

or,
$$-K'V_i = \log_{10}\left(\frac{V_o}{V_{ref}}\right)$$

or,
$$\frac{V_o}{V_{ref}} = 10^{-K'V_i}$$

or,
$$V_o = V_{ref}\,(10^{-K'V_i}) \tag{4.53}$$

where
$$K' = 0.4343\left(\frac{q}{kT}\right)\left(\frac{R_{TC}}{R_2 + R_{TC}}\right) \tag{4.54}$$

Hence an increase of input by one volt causes the output to decrease by a decade. The 755 log/antilog amplifier IC chip is available as a

functional module which may require some external components also to be connected to it.

4.9 MULTIPLIER AND DIVIDER

Multiplier

There are a number of applications of analog multiplier such as frequency doubling, frequency shifting, phase angle detection, real power computation, multiplying two signals, dividing and squaring of signals. A basic multiplier schematic symbol is shown in Fig. 4.20 (a). Two signal inputs (v_x and v_y) are provided. The output is the product of the two inputs divided by a reference voltage V_{ref}.

$$v_o = \frac{v_x v_y}{V_{ref}} \tag{4.55}$$

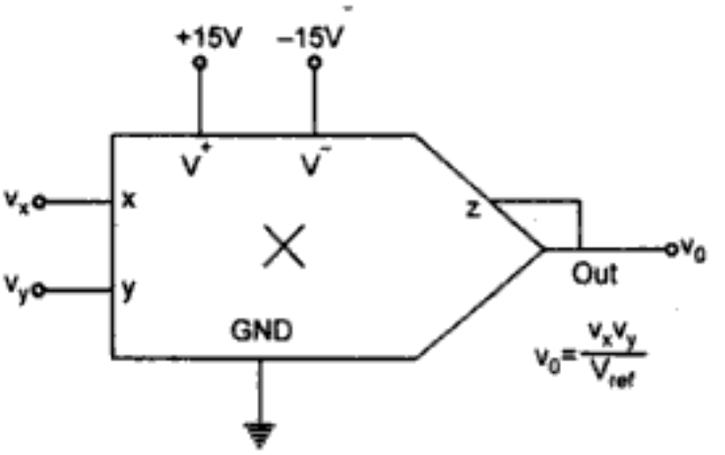

Fig. 4.20 (a) Multiplier schematic symbol

Normally, V_{ref} is internally set to 10 volts. So,

$$v_o = \frac{v_x v_y}{10}$$

As long as

$$v_x < V_{ref}$$

and $$v_y < V_{ref}$$

the output of the multiplier will not saturate.

If both inputs are positive, the IC is said to be a one quadrant multiplier. A two quadrant multiplier will function properly if one input is held positive and the other is allowed to swing both positive and negative. If both inputs may be either positive or negative, the IC is called a four quadrant multiplier.

There can be several ways to make a circuit which will multiply according to Eq. (4.55). One commonly used technique is log-antilog method. The log-antilog method relies on the mathematical relationship

that the sum of the logarithm of two numbers equals the logarithm of the product of those numbers.

$$\ln v_x + \ln v_y = \ln (v_x v_y) \tag{4.56}$$

Figure 4.20 (b) is a block diagram of a log-antilog multiplier IC. Log -amps require the input and reference voltages to be of the same polarity. This restricts log-antilog multipliers to one quadrant operation. A technique that provides four quadrant multiplication is transconductance multiplier. Some of the multiplier IC chips available are AD533 and AD534. We now discuss two applications of multiplier IC.

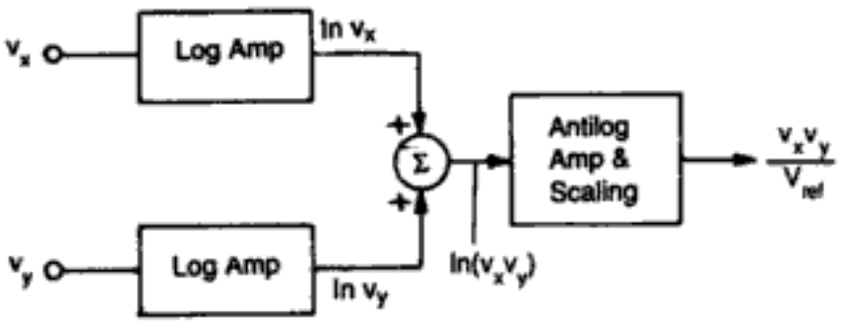

Fig. 4.20 (b) Block diagram of a log-antilog

Frequency Doubling

The multiplication of two sine waves of the same frequency, but of possibly different amplitudes and phase allows to double a frequency and to directly measure real power. Let

$$v_x = V_x \sin \omega t \tag{4.57}$$

$$v_y = V_y \sin (\omega t + \theta) \tag{4.58}$$

where θ is the phase difference between the two signals. Applying these two signals to the inputs of a four quadrant multiplier will yield an output as,

$$v_o = \frac{V_x \sin \omega t \, V_y \sin (\omega t + \theta)}{V_{ref}} \tag{4.54}$$

$$v_o = \frac{V_x V_y}{V_{ref}} \sin \omega t \, (\sin \omega t \cos \theta + \sin \theta \cos \omega t)$$

$$= \frac{V_x V_y}{V_{ref}} (\sin^2 \omega t \cos \theta + \sin \theta \sin \omega t \cos \omega t)$$

But $\sin^2 a = 1 - \cos^2 a$

and $\cos^2 a = 2 \cos^2 a - 1$

so $$\cos^2 a = \frac{1}{2} + \left(\frac{1}{2}\right)\cos 2a$$

$$\sin^2 a = 1 - \frac{1}{2} - \left(\frac{1}{2}\right)\cos 2a = \frac{1}{2} - \left(\frac{1}{2}\right)\cos 2a$$

so $$v_o = \frac{V_x V_y}{V_{ref}}\left[\cos\theta\left(\frac{1}{2} - \left(\frac{1}{2}\right)\cos 2\,\omega t\right) + \sin\theta \sin\omega t \cos\omega t\right] \quad (4.60)$$

But, $\sin a \cos a = \left(\frac{1}{2}\right)\sin 2a$

Hence, $$v_o = \frac{V_x V_y}{2 V_{ref}}(\cos\theta - \cos\theta\cos 2\omega t + \sin\theta \sin 2\omega t)$$

or, $$v_o = \frac{V_x V_y}{2V_{ref}}\cos\theta + \frac{V_x V_y}{2V_{ref}}(\sin\theta \sin 2\,\omega t - \cos\theta\cos 2\,\omega t) \quad (4.61)$$

The first term is a DC and is set by the magnitude of the signals and their phase difference. The second term varies with time, but at twice the frequency of the inputs (2ω).

Divider

Division, the complement of multiplication, can be accomplished by placing the multiplier circuit element in the op-amp's feedback loop. The output voltage from the divider in Fig. 4.20 (c) with input signals v_z and v_x as dividend and divisor respectively, is given by

$$v_o = -V_{ref}\frac{v_z}{v_x} \quad (4.62)$$

The result can be derived as follows. The op-amp's inverting terminal is at virtual ground. Therefore,

$$I_z = I_A \quad (4.63)$$

and $$I_z = \frac{v_z}{R} \quad (4.64)$$

The output voltage V_A of the multiplier is determined by the multiplication of v_x and v_y

$$V_A = \frac{v_x v_y}{V_{ref}} = \frac{v_x v_o}{V_{ref}} \quad (4.65)$$

Again $$V_A = -I_A R$$

so, $$I_A = -V_A/R = -\frac{v_x v_o}{V_{ref} R} \quad (4.66)$$

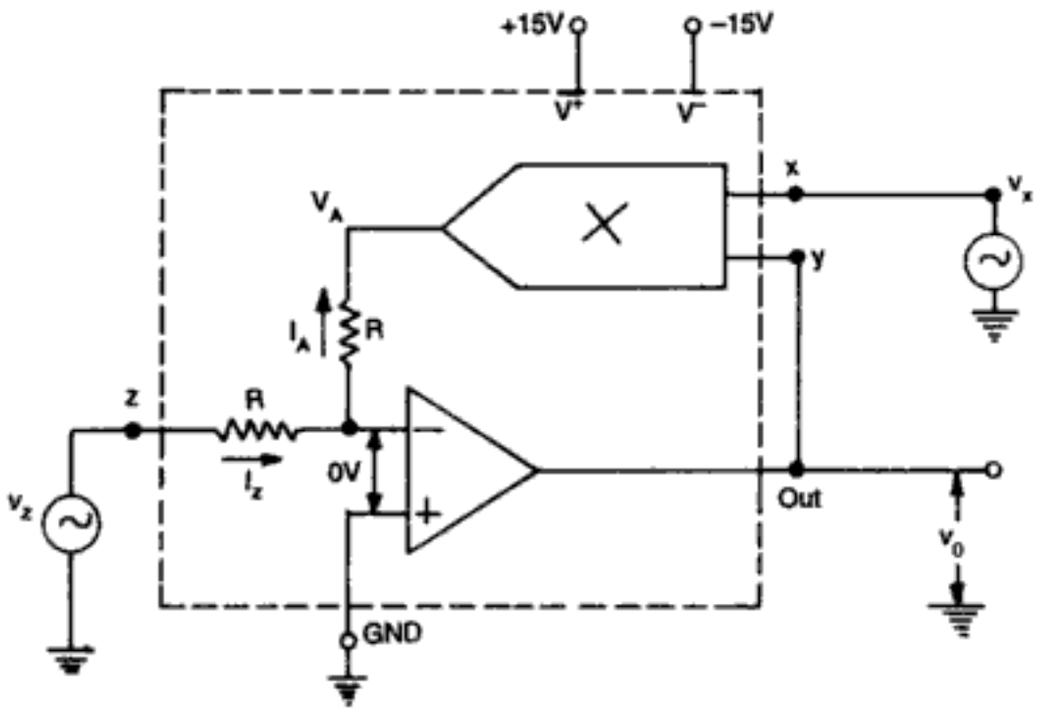

Fig. 4.20 (c) Multiplier IC configured as divider

As, $$I_z = I_A$$

so, $$I_z = -\frac{v_x v_0}{V_{ref} R}$$

From Eq. (4.64), wt get

$$v_z = I_z R = -\frac{v_x v_0}{V_{ref}}$$

or, $$v_0 = -V_{ref}\frac{v_z}{v_x} \qquad (4.67)$$

Division by zero is, of course, prohibited. Multiplier IC can be used for squaring a signal. Similarly, divider circuit can be used to take the square root of a signal.

4.10 DIFFERENTIATOR

One of the simplest of the op-amp circuits that contain capacitor is the differentiating amplifier, or differentiator. As the name suggests, the circuit performs the mathematical operation of differentiation, that is, the output waveform is the derivative of input waveform. A differentiator circuit is shown in Fig. 4.21 (a).

Analysis

The node N is at virtual ground potential i.e., $v_N = 0$. The current i_C through the capacitor is,

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Example 4.7

For the circuit shown in Fig. 4.27 if the input is a constant V, show that the output $v_o(t)$ is given by a differential equation.

Solution

The transfer gain of the circuit is,

$$\frac{V_o(s)}{V_i(s)} = -\frac{Z_f}{R_1} = -\frac{R_2 + \dfrac{R_3/sC}{R_3 + 1/sC}}{R_1}$$

$$= \frac{(R_2 + R_3) + sC R_2 R_3}{R_1 (1 + sC R_3)} \qquad (4.91)$$

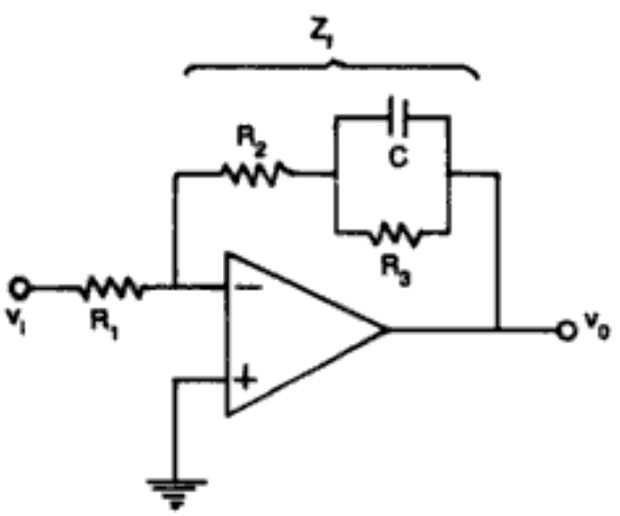

Fig. 4.27 Circuit for Example 4.7

or, $R_1(1 + s\,C\,R_3)\,V_o(s) + [(R_2 + R_3) + s\,C\,R_2R_3]\,V_i(s) = 0 \qquad (4.92)$

Writing Eq. (4.92) in time domain $\left(s \to \dfrac{d}{dt}\right)$, we get

$$R_1\left(1 + CR_3\frac{d}{dt}\right)v_o(t) + \left[(R_2 + R_3) + CR_2R_3\frac{d}{dt}\right]v_i(t) = 0 \qquad (4.93)$$

Since $v_i(t) = V$

Therefore, $\dfrac{dv_i(t)}{dt} = 0$

Hence $CR_1R_3\dfrac{dv_o}{dt} + R_1v_o + (R_2 + R_3)V = 0$

or, $C\dfrac{dv_o}{dt} + \dfrac{v_o}{R_3} + \dfrac{V}{R_1} + \dfrac{R_2}{R_1R_3}V = 0 \qquad (4.94)$

Example 4.8

Figure 4.28 shows a non-inverting integrator. Show that $v_o = \frac{1}{RC}\int v_i\, dt$.

Solution

The voltage at the (+) input terminal of the op-amp due to the potential divider is,

$$V(+) = \frac{1/sC}{R + 1/sC} V_i(s) \tag{4.95}$$

The output voltage $V_o(s)$ for the non-inverting amplifier is

$$V_o(s) = \left(1 + \frac{1/sC}{R}\right) V(+)$$

$$= \frac{1}{sRC} V_i(s) \tag{4.96}$$

Hence in time-domain, we get,

$$v_o = \frac{1}{RC}\int v_i\, dt$$

Note that there is no phase inversion in a non-inverting integrator.

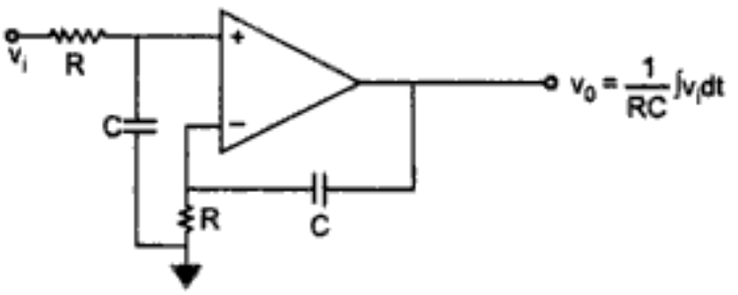

Fig. 4.28 Noninverting integrator circuit

4.12 ELECTRONIC ANALOG COMPUTATION

An analog computer performs linear operations such as multiplication by a constant, addition, subtraction and integration. Since these operations are sufficient for the solution of linear differential equation, it is possible to connect the various modules of an analog computer for obtaining the solution of differential equation.

We have already discussed the building blocks of the analog computer, that is, op-amp used as inverter, scale changer, summer, integrator, summing integrator etc. Potentiometer is widely used in analog computer to multiply voltages by a constant less than unity.

The symbolic representation of a summer, potentiometer and summing integrator is shown in Fig. 4.29 (a, b, c).

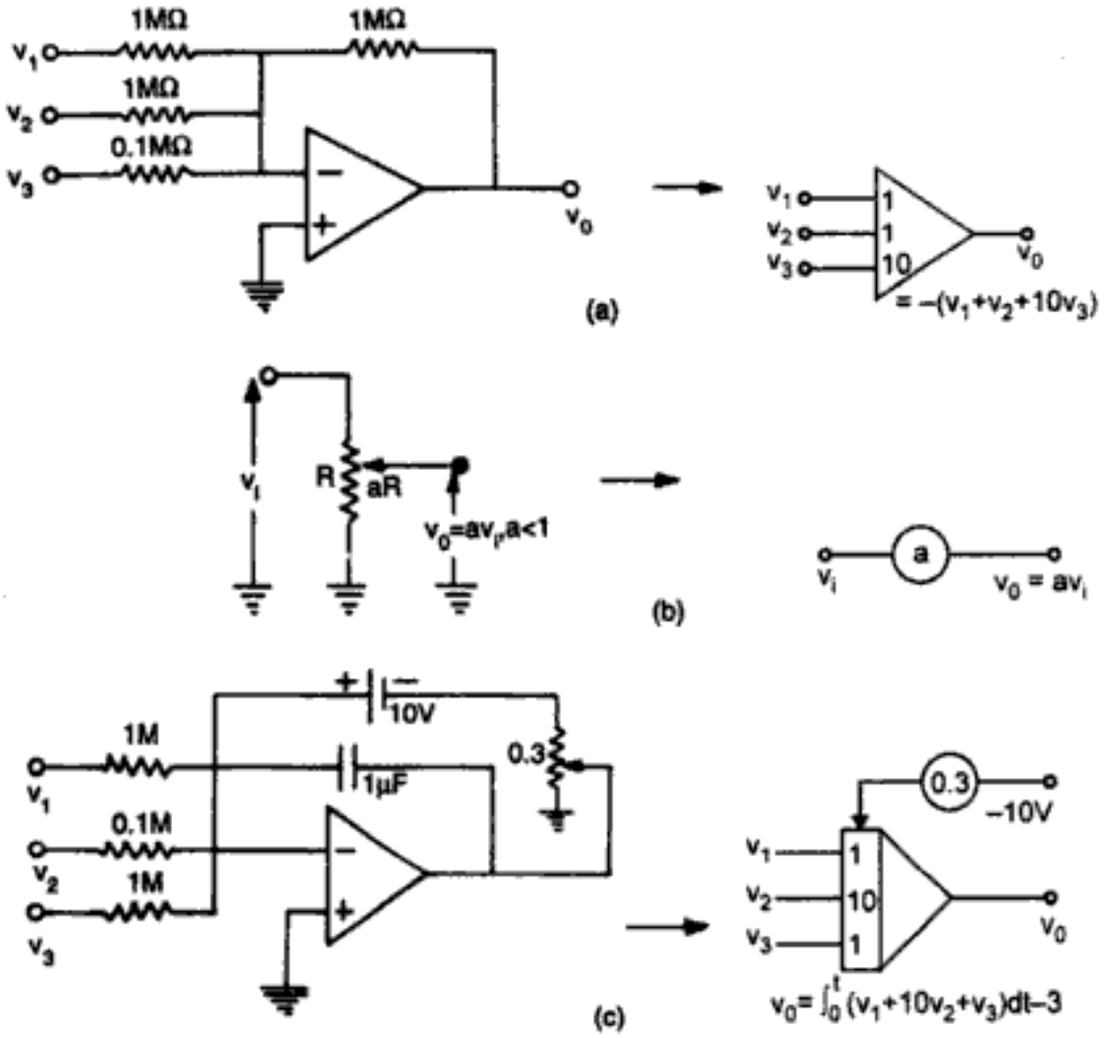

Fig. 4.29 (a) Summer and its symbolic representation (b) Potentiometer and its symbol. (c) Summing integrator and its symbol

Let us now see how an analog computer can be used to solve a second order differential equation given as,

$$\frac{d^2y}{dt^2} + 5.4\frac{dy}{dt} + 0.58\,y = u(t) \tag{4.97}$$

with initial conditions,

$$y\,(0) = -\,4.8 \text{ and } \left.\frac{dy}{dt}\right|_{t=0} = \dot{y}(0) = 2.3$$

Rewrite Eq. (4.97) by keeping the highest order derivative on the left hand side and taking all other terms to the right side as

$$\ddot{y} = -5.4\,\dot{y} - 0.58\,y + u(t) \tag{4.98}$$

Assuming $\ddot{y}$ is available, it may be successively integrated to obtain $\dot{y}$ and y as shown in Fig. 4.30 (a). At the output of amplifier 4, i.e. point B, we obtain the sum

$$-5.4\,\dot{y} - 0.58\,y + u(t)$$

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3573. The 3573 is desigred to deliver 100W peak or 40W continuous output power and can be used to drive dc and ac motors, electronic valves and push-pull solenoids.

4.14 OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA)

In Sec. 4.5, we have discussed the use of 741 op-amp as a voltage to current converter. A voltage to current converter is an amplifier which produces an output current proportional to an input voltage. The constant of proportionality is the transconductance of the amplifier and therefore such amplifiers are also known as transconductance amplifier. Due to wide applications, specially designed single chip transconductance amplifiers are available, called, operational transconductance amplifier (OTA). The symbolic representation of an OTA is shown in Fig. 4.37 (a). An OTA is a voltage-input, current-output device such that

$$I_o = g_m V_{in} = g_m (V_1 - V_2) \tag{4.107}$$

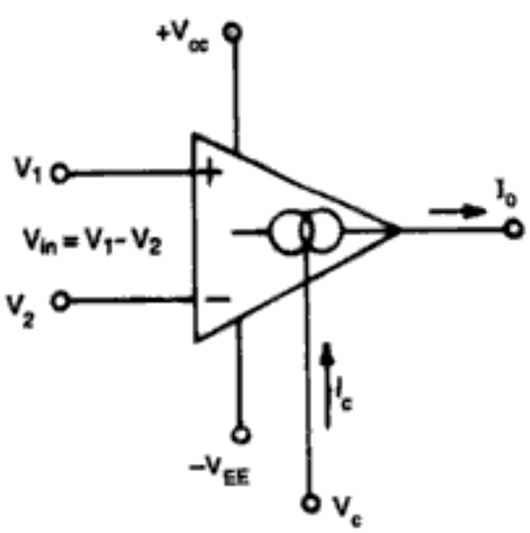

Fig. 4.37 (a) Symbol for OTA

where g_m is the transconductance, or gain of the OTA. The unique feature of an OTA is that it is possible to vary g_m over a wide range by means of an external control current. OTAs are used to implement programmable amplifiers and integrators in audio processing and electronic music synthesis. They are also used as current switches in sample-and-hold applications. Another important application of OTA using VLSI technique is in Neural networks. Popular OTAs are the CA3080 (RCA), the LMI 3600/700 (National Semiconductor) and the NE 5517 (Signetics).

The simplified internal circuit diagram of an OTA is shown in Fig. 4.37 (b). Transistors Q_1 and Q_2 form a differential pair. Current mirror $Q_3 - Q_4$ accepts the control current I_c which can be adjusted by an external resistance R_{ext} and control voltage V_c. Due to current mirror

$Q_3 - Q_4$, we get $I_4 = I_c$. The current I_4 is divided at the emitters of Q_1 and Q_2. Thus

$$I_1 + I_2 = I_4$$

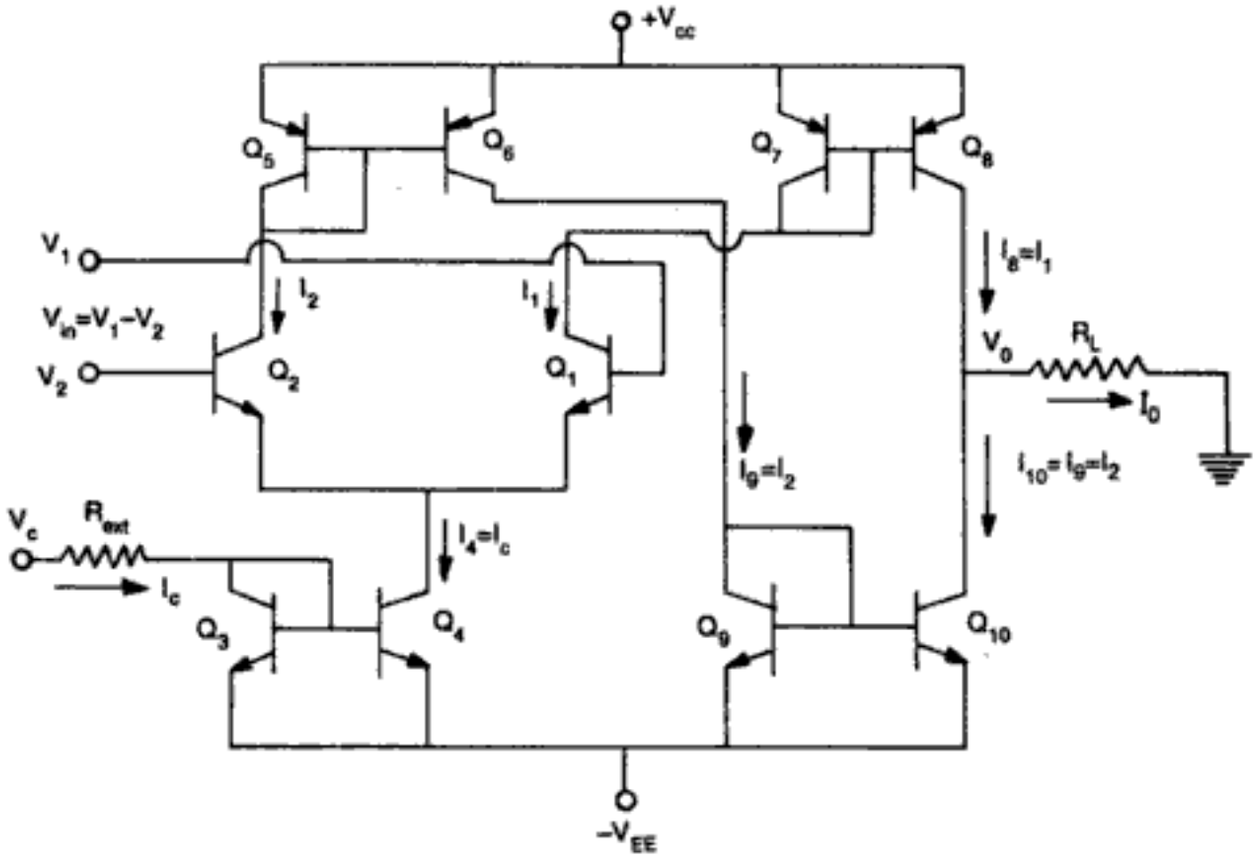

Fig. 4.37 (b) Simplified internal diagram of OTA

Current mirror $Q_5 - Q_6$ duplicates I_2 to yield $I_9 = I_2$. The current I_2 is in turn duplicated by current mirror $Q_9 - Q_{10}$ to produce $I_{10} = I_9 = I_2$. Similarly, current mirror $Q_7 - Q_8$ duplicates I_1 to yield $I_8 = I_1$. By KCL, we have,

$$I_o = I_8 - I_{10} = I_1 - I_2 \tag{4.108}$$

Hence, the voltage gain A_v can be written as

$$A_v = \frac{V_o}{V_{in}} = \frac{I_o R_L}{V_{in}} = g_m R_L \tag{4.109}$$

The transconductance g_m can be calculated as

$$I_1 = I_s \, e^{V_1/V_T} \tag{4.110}$$

and

$$I_2 = I_s \, e^{V_2/V_T} \tag{4.111}$$

where, I_s = reverse saturation current of transistor Q_1, Q_2 assumed to be equal and, V_T = volts equivalent of temperature

Now
$$I_c = I_1 + I_2 = I_s\left[e^{V_1/V_T} + e^{V_2/V_T}\right] \tag{4.112}$$

or,
$$I_s = \frac{I_c}{e^{V_1/V_T} + e^{V_2/V_T}} \tag{4.113}$$

So,
$$I_1 = \frac{I_c\, e^{V_1/V_T}}{e^{V_1/V_T} + e^{V_2/V_T}} \tag{4.114}$$

and
$$I_2 = \frac{I_c\, e^{V_2/V_T}}{e^{V_1/V_T} + e^{V_2/V_T}} \tag{4.115}$$

Hence
$$I_1 - I_2 = I_c \frac{e^{V_1/V_T} - e^{V_2/V_T}}{e^{V_1/V_T} + e^{V_2/V_T}} \tag{4.116}$$

Multiplying both the numerator and denominator by $e^{-\frac{V_1+V_2}{2}}$; Eq. (4.116) can be expressed in terms of voltage difference $(V_1 - V_2)$ as,

$$I_o = I_1 - I_2 = I_c \frac{e^{\frac{V_1 - V_2}{2V_T}} - e^{-\frac{V_1 - V_2}{2V_T}}}{e^{\frac{V_1 - V_2}{2V_T}} + e^{-\frac{V_1 + V_2}{2V_T}}} \tag{4.117}$$

$$= I_c \tanh\left(\frac{V_1 - V_2}{2V_T}\right) \tag{4.118}$$

A plot of output current I_o as a function of $(V_1 - V_2)$ is shown in Fig. 4.38. A transconductance amplifier basically computes a tan-hyperbolic. It operates linearly for a very small range of inputs and smoothly transits to saturation. The transconductance is given by

$$g_m = \left|\frac{\partial I_o}{\partial V_{in}}\right| = \frac{I_c}{2V_T} \tag{4.119}$$

$$\left(\text{with the assumption that for small } V_1 - V_2 ; \tanh\left(\frac{V_1 - V_2}{2V_T}\right) = \frac{V_1 - V_2}{2V_T}\right)$$

Then the voltage gain A_v is,

$$A_v = g_m R_L = \frac{I_c R_L}{2V_T} \tag{4.120}$$

Thus the voltage gain of the OTA circuit can be externally controlled by the control current I_c.

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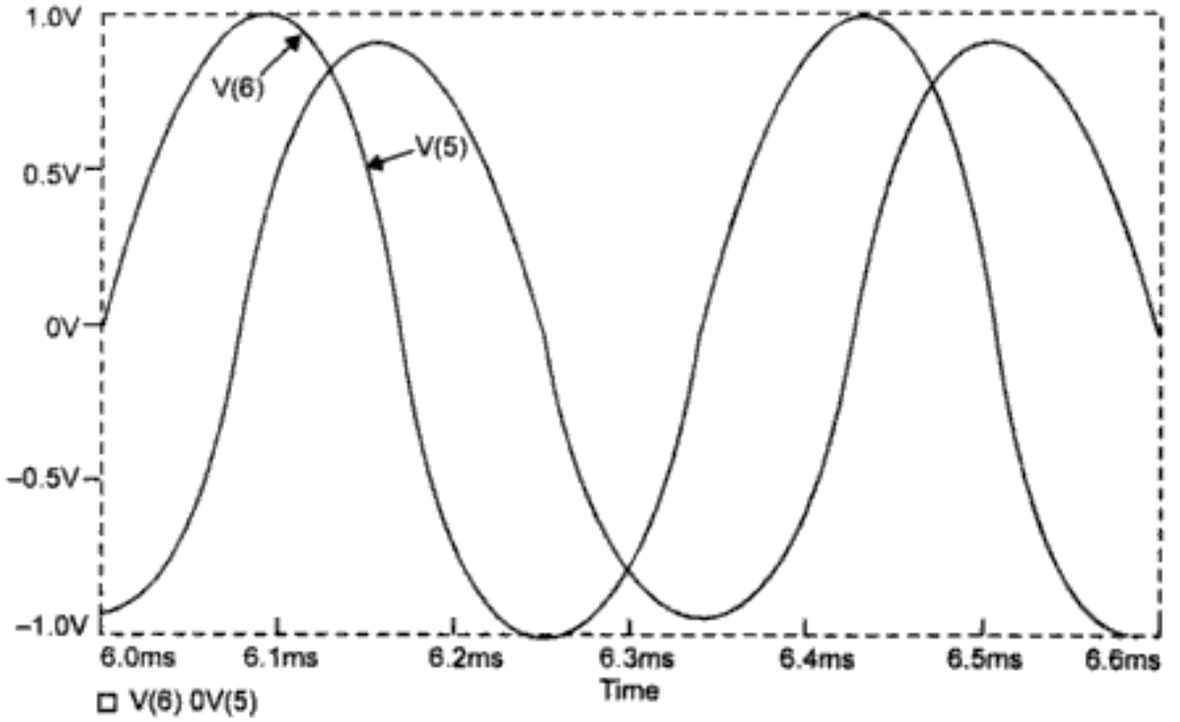

Fig. C 4.2 (c) Input and output waveforms of a practical differentiator

Experiment 4.3

To demonstrate the operation of a Lossy Integrator

Design Aspects

Fig. E. 4.3 (a) shows a lossy integrator designed in Example 4.4.

The resistor R_f (100 kΩ) is connected across the 0.01 μF capacitor to prevent the amplifier from saturation due to the presence of any dc offset in the input.

Choose $R_f C_f$ = period of the signal to be integrated = $1/f_a$ and R_f = 10 R_1.

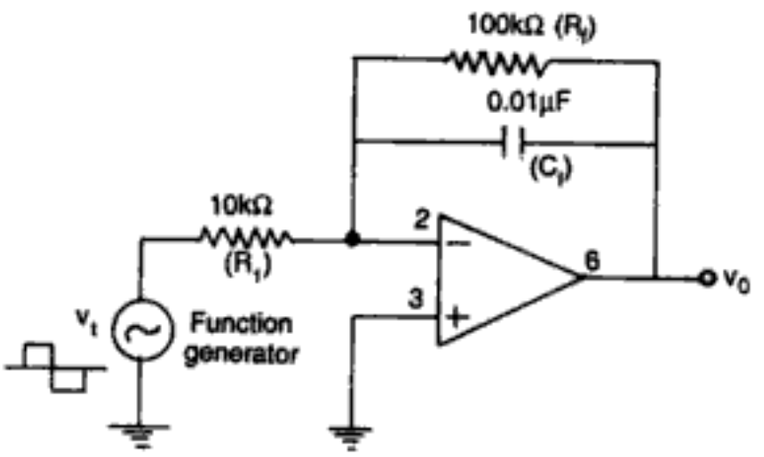

Fig. E. 4.3 (a) A Lossy integrator

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5

Comparators and Waveform Generators

5.1 INTRODUCTION

An operational amplifier in the open-loop configuration operates in a non-linear manner. There are a number of applications of op-amp in this mode, such as, comparators, detectors, limiters and digital interfacing devices namely converters. In this chapter, we shall discuss comparator and its applications.

5.2 COMPARATOR

A comparator is a circuit which compares a signal voltage applied at one input of an op-amp with a known reference voltage at the other input. It is basically an open-loop op-amp with output $\pm V_{sat}$ ($= V_{CC}$) as shown in the ideal transfer characteristics of Fig. 5.1 (a). However, a commercial op-amp has the transfer characteristics of Fig. 5.1 (b).

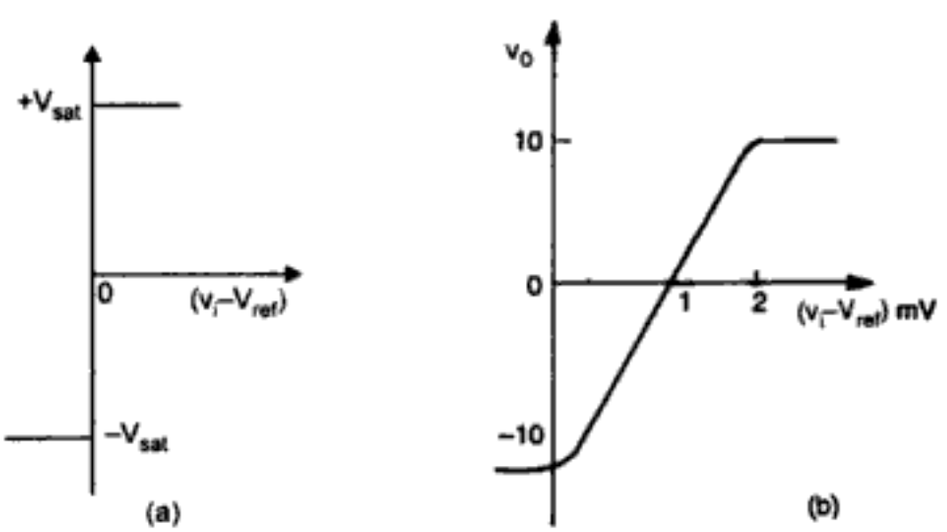

Fig. 5.1 The transfer characteristics (a) ideal comparator (b) practical comparator

It may be seen that the change in the output state takes place with an increment in input v_i of only 2 mV. This is the uncertainty region where output cannot be directly defined. There are basically two types of comparators:

Non-inverting comparator
Inverting comparator.

The circuit of Fig. 5.2 (a) is called a non-inverting comparator. A fixed reference voltage V_{ref} is applied to (–) input and a time varying

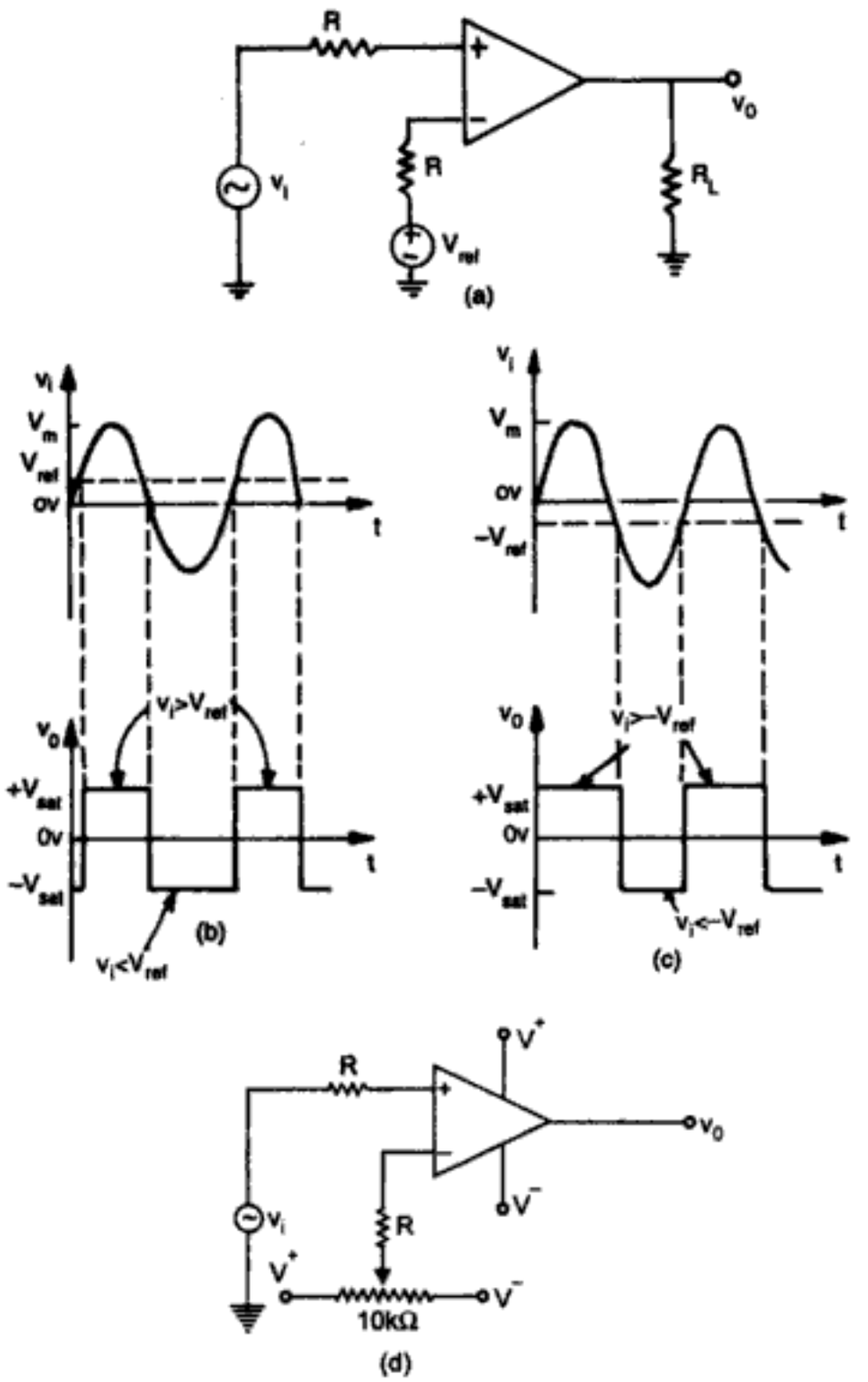

Fig. 5.2 (a) Non-inverting comparator. Input and output waveforms for (b) V_{ref} positive (c) V_{ref} negative (d) Practical noninverting comparator

signal v_i is applied to (+) input. The output voltage is at $-V_{sat}$ for $v_i < V_{ref}$. And v_o goes to $+V_{sat}$ for $v_i > V_{ref}$. The output waveform for a sinusoidal input signal applied to the (+) input is shown in Fig. 5.2 (b and c) for positive and negative V_{ref} respectively.

In a practical circuit V_{ref} is obtained by using a 10 kΩ potentiometer which forms a voltage divider with the supply voltages $V+$ and $V-$ with the wiper connected to (–) input terminal as shown in Fig. 5.2 (d). Thus a V_{ref} of desired amplitude and polarity can be obtained by simply adjusting the 10 kΩ potentiometer.

Figure 5.3 (a) shows a practical inverting comparator in which the reference voltage V_{ref} is applied to the (+) input and v_i is applied to (–) input. For a sinusoidal input signal, the output waveform is shown in Fig. 5.3 (b) and (c) for V_{ref} positive and negative respectively.

Output voltage levels independent of power supply voltages can also be obtained by using a resistor R and two back to back zener diodes at the output of op-amp as shown in Fig. 5.3 (d). The value of resistance R is chosen so the zener diodes operate at the recommended current. It can be seen that the limiting voltages of v_o are $(V_{Z1} + V_D)$ and $-(V_{Z2} + V_D)$ where V_D (~ 0.7 V) is the diode forward voltage.

In the waveforms of Figs. 5.2 and 5.3, the output transitions are shown as taking place instantaneously. Practical circuits, however, take a certain amount of time to switch from one voltage level to another. The actual waveform will therefore exhibit slanted edges as well as delays at the points of input threshold crossing. These effects are more noticeable at high frequencies where the output switching times are comparable or even longer than the input period itself. Thus there is an upper limit to the operating frequency of any comparator.

If 741, the internally compensated op-amp is used as comparator, the primary limitation is the slew rate. Since 741C has slew rate equal to 0.5 V/μs, it takes $2 \times 13/0.5 \simeq 50$ μs ($V_{sat} = \pm 13$V for 741) to swing from one saturation level to the other. In many applications, this is too long. To increase the response time, it is possible to use uncompensated op-amps such as 301, for comparator applications.

Although uncompensated op-amps make faster comparators than compensated op-amps, there are applications where even higher speeds are required. Also, for interfacing, it is often desired that the output logic levels be compatible with standard logic families such as TTL, CMOS, ECL. To accomodate these needs, monolithic voltage comparators are available. Some of the comparator chips available are the Fairchild μA 710 and 760, the National LM 111, 160 and 311. The response time for 311 is 200 ns whereas 710 is a high speed comparator with a response time of 40 ns. CMOS comparators are also available. Some examples are TLC 372 dual, TLC 374 quad (Texas Instruments), MC 14574 quad (Motorola).

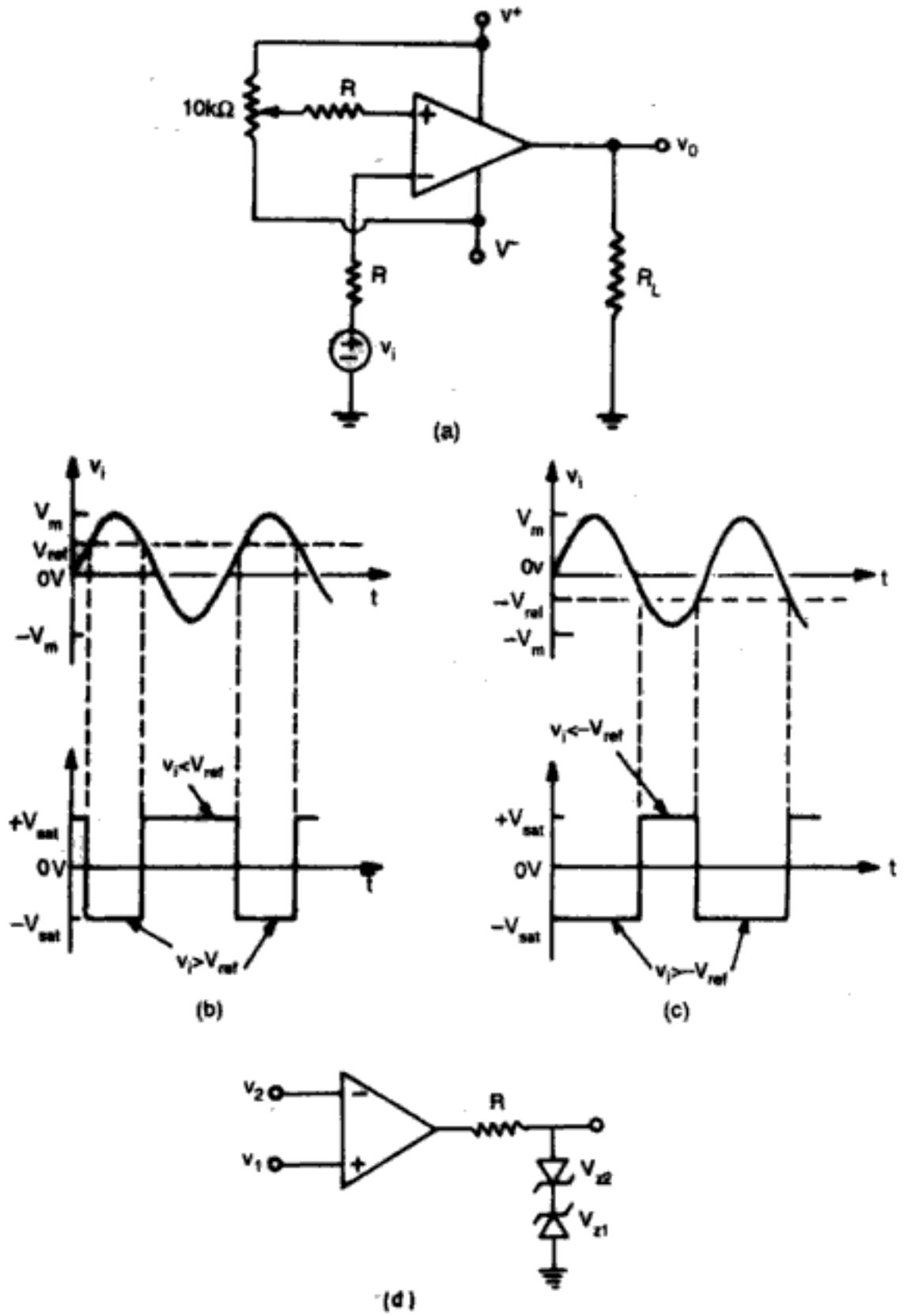

Fig. 5.3 (a) Inverting comparator. Input and output waveforms (b) $V_{ref} > 0$ (c) $V_{ref} < 0$ (d) Comparator with zener diode at the output

5.2.1 Applications of Comparator

Some important applications of comparator are:

Zero crossing detector
Window detector
Time marker generator
Phase meter.

Zero Crossing Detector

The basic comparators of Fig. 5.2 (a) and 5.3 (a) can be used as a zero crossing detector provided that V_{ref} is set to zero. An inverting zero-crossing detector is shown in Fig. 5.4 (a) and the output waveform for a sinusoidal input signal is shown in Fig. 5.4 (b). The circuit is also called a sine to square wave generator.

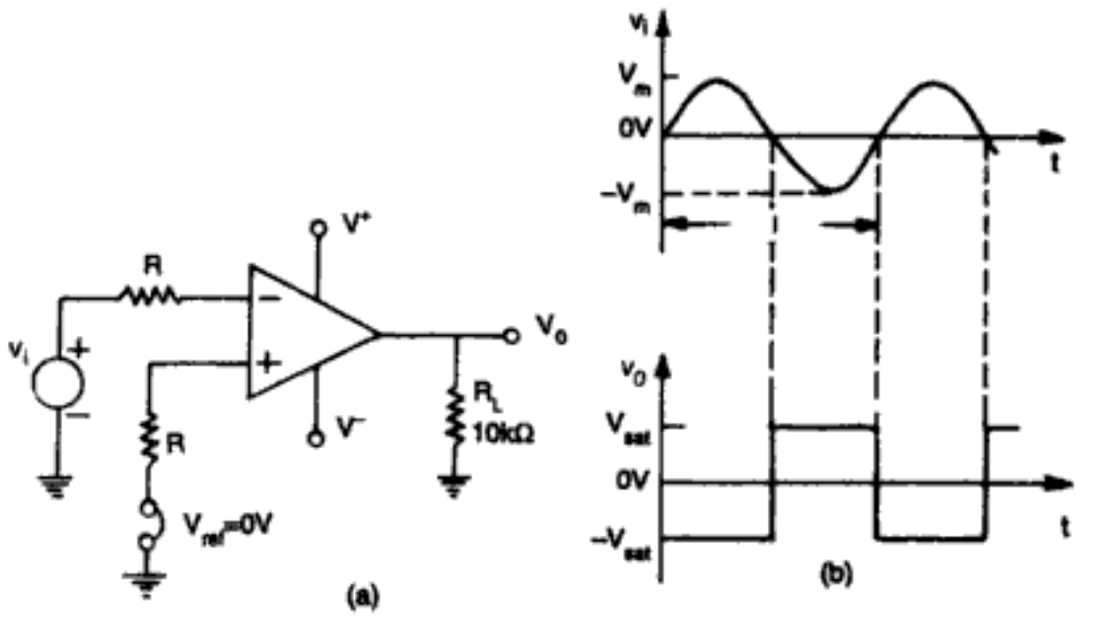

Fig. 5.4 (a) Zero crossing detector (b) Input and output waveforms

Window Detector

Sometimes one may like to mark the instant at which an unknown input is between two threshold levels. This can be achieved by a circuit called window detector. Figure 5.5 shows a three level detector with indicator circuit. There are three indicators: Yellow (LED 3) for input too low (< 3V), Green (LED 2) for safe input (3 – 6V) and Red (LED 1) for high input (> 6V). They are turned ***on*** and ***off*** as indicated in Table 5.1.

Table 5.1 Three level comparator LED specifications

Input (volts)	*Yellow LED 3*	*Green LED 2*	*Red LED 1*
Less than 3 V	On	Off	Off
Between 3 V and 6 V	Off	On	Off
Greater than 6V	Off	Off	On

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positive pulses of spacing T and may be used for triggering the monoshots, SCR, sweep voltage of CRT etc.

Phase Detector

The phase angle between two voltages can also be measured using the circuit of Fig. 5.6 (a). Both voltages are converted into spikes and the time interval between the pulse spikes of one input and that of the other is measured. The time interval is proportional to the phase difference. One can measure phase angles from 0° to 360° with such a circuit.

Example 5.1

(a) For the comparator shown in Fig. 5.7 (a) plot the transfer curve if the op-amp is an ideal one and $V_{Z1} = V_{Z2} = 9$ V.
(b) Repeat part (a) if the open loop gain of op-amp is 50,000.

Solution

(a) Since $A_{OL} = \infty$, even a small positive or negative voltage at the input drives the output to $\pm V_{sat}$. This causes V_{Z1} or V_{Z2} to break down, giving output voltage $v_o = \pm (V_Z + V_D) = \pm 9.7$ V. The transfer curve is shown in Fig. 5.7 (b).

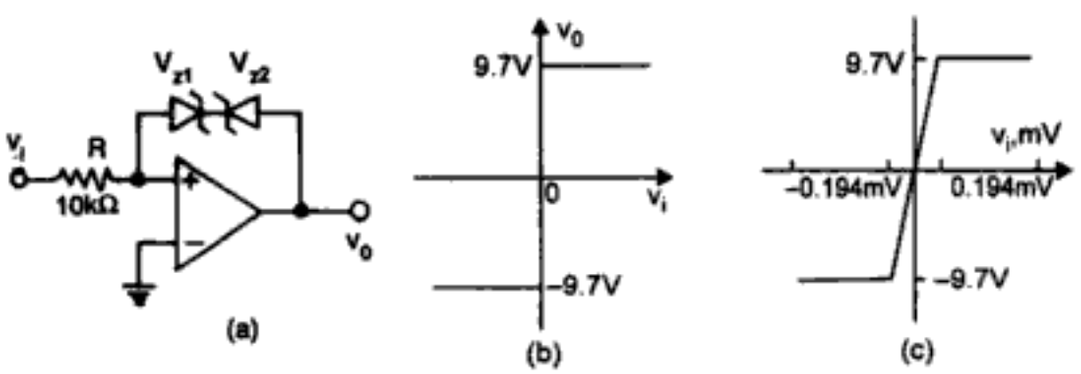

Fig. 5.7 (a) Circuit of Example 5.1 (b) Transfer curve for Example 5.1 (a). (c) Transfer curve for Example 5.1 (b)

(b) Now $A_{OL} = 50{,}000$, so $\Delta v_i = \dfrac{9.7}{A_{OL}} = 0.194$ mV. The zeners break down after ± 0.194 mV as shown in the transfer curve of Fig. 5.7 (c).

5.3 REGENERATIVE COMPARATOR (SCHMITT TRIGGER)

If positive feedback is added to the comparator circuit, gain can be increased greatly. Consequently, the transfer curve of comparator becomes more close to ideal curve. Theoretically, if the loop gain $-\beta A_{OL}$ is adjusted to unity, then the gain with feedback, A_{Vf} becomes

infinite. This results in an abrupt (zero rise time) transition between the extreme values of output voltage. In practical circuits, however, it may not be possible to maintain loop-gain exactly equal to unity for a long time because of supply voltage and temperature variations. So a value greater than unity is chosen. This also gives an output waveform virtually discontinuous at the comparison voltage. This circuit, however, now exhibits a phenomenon called hysteresis or backlash.

Figure 5.8 (a) shows such a regenerative comparator. The circuit is also known as Schmitt Trigger. The input voltage is applied to the (–) input terminal and feedback voltage to the (+) input terminal. The input voltage v_i triggers the output v_o every time it exceeds certain voltage levels. These voltage levels are called upper threshold voltage (V_{UT}) and lower threshold voltage (V_{LT}). The hysteresis width is the difference between these two threshold voltages i.e. $V_{UT} - V_{LT}$. These threshold voltages are calculated as follows.

Suppose the output $v_o = + V_{sat}$. The voltage at (+) input terminal will be

$$V_{ref} + \frac{R_2}{R_1 + R_2}(V_{sat} - V_{ref}) = V_{UT} \tag{5.1}$$

This voltage is called upper threshold voltage V_{UT}. As long as v_i is less than V_{UT}, the output v_o remains constant at $+ V_{sat}$. When v_i is just greater than V_{UT}, the output regeneratively switches to $-V_{sat}$ and remains at this level as long as $v_i > V_{UT}$ as shown in Fig. 5.8 (b).

For $v_o = -V_{sat}$, the voltage at the (+) input terminal is,

$$V_{ref} - \frac{R_2}{R_1 + R_2}(V_{sat} + V_{ref}) = V_{LT} \tag{5.2}$$

This voltage is referred to as lower threshold voltage V_{LT}. The input voltage v_i must become lesser than V_{LT} in order to cause v_o to switch from $-V_{sat}$ to $+V_{sat}$. A regenerative transition takes place as shown in Fig. 5.8 (c) and the output v_o returns from $-V_{sat}$ to $+V_{sat}$ almost instantaneously. The complete transfer characteristics are shown in Fig. 5.8 (d).

Note that $V_{LT} < V_{UT}$ and the difference between these two voltages is the hysteresis width V_H and can be written as

$$V_H = V_{UT} - V_{LT} = \frac{2 R_2 V_{sat}}{R_1 + R_2} \tag{5.3}$$

Because of the hysteresis, the circuit triggers at a higher voltage for increasing signals than for decreasing ones. Further, note that if peak-to-peak input signal v_i were smaller than V_H then the Schmitt trigger circuit, having responded at a threshold voltage by a transition in one direction would never reset itself, that is, once the output has jumped to, say, $+V_{sat}$ it would remain at this level and never return

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$$V_{UT} = -V_{LT} = \frac{R_2 V_{sat}}{R_1 + R_2}$$

If an input sinusoid of frequency $f = 1/T$ is applied to such a comparator, a symmetrical square wave is obtained at the output. The vertical edge of the output waveform however will not occur at the time the sine wave passes through zero [Fig. 5.8 (f)] but is shifted in phase by θ where $\sin\theta = V_{UT}/V_m$ and V_m is the peak sinusoidal voltage.

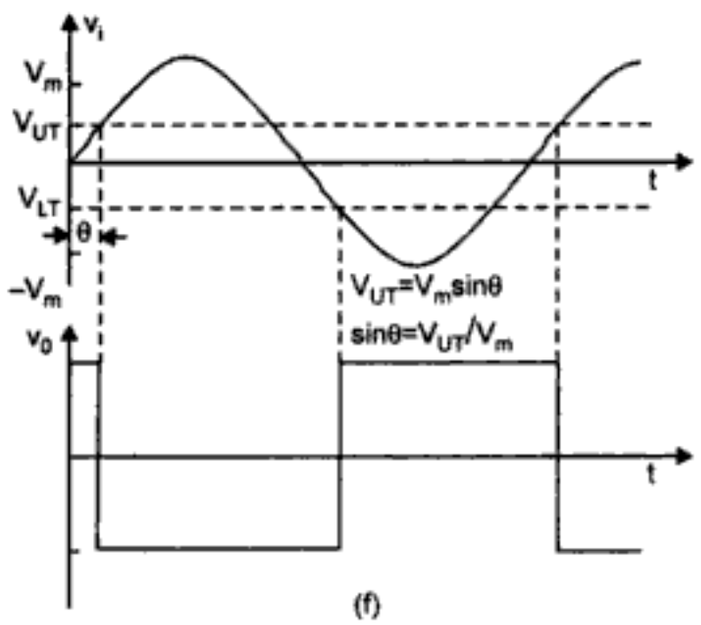


Fig. 5.8 (f) Shift θ in the output waveform for $V_{UT} = -V_{LT}$

Special purpose Schmitt triggers are commercially available. T1–13, T1–14 and T1–132 chips with totem pole output and $V_{UT} = 1.7$ V, $V_{LT} = 0.9$ V are available. The T1–132 package is a quad two-input NAND Schmitt trigger. CMOS Schmitt triggers offer the advantage of high input impedance and low power consumption. Examples of CMOS inverting Schmitt trigger are the CD40106B and 744C14.

Example 5.2

In the circuit of Schmitt trigger of Fig. 5.8 (a), $R_2 = 100\ \Omega$, $R_1 = 50\ k\Omega$, $V_{ref} = 0V$, $v_i = 1V_{pp}$ (peak-to-peak) sine wave and saturation voltage = ± 14V. Determine threshold voltages V_{UT} and V_{LT}.

Solution

From Eqs. (5.1) and (5.2)

$$V_{UT} = \frac{100}{50100} \times 14 = 28\ \text{mV}$$

$$V_{LT} = \frac{100}{50100} \times (-14) = -28\ \text{mV}$$

Example 5.3

A Schmitt trigger with the upper threshold level V_{UT} = 0V and hysteresis width V_H = 0.2V converts a 1 kHz sine wave of amplitude $4V_{pp}$ into a square wave. Calculate the time duration of the negative and positive portion of the output waveform.

Solution

$$V_{UT} = 0$$

$$V_H = V_{UT} - V_{LT} = 0.2 \text{ V}$$

So, $$V_{LT} = -0.2 \text{ V}$$

In Fig. 5.9, the angle θ can be calculated as

$$-0.2 = V_m \sin(\pi + \theta) = -V_m \sin\theta = -2 \sin\theta$$

$$\theta = \text{arc sin } 0.1 = 0.1 \text{ radian}$$

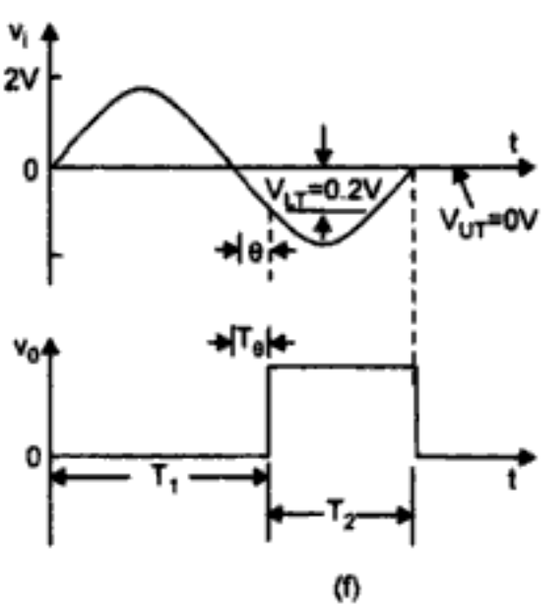
The period, $T = 1/f = 1/1000 = 1$ ms

$$wT_\theta = 2\pi\,(1000)\,T_\theta = 0.1$$

$$T_\theta = (0.1/2\pi) \text{ ms} = 0.016 \text{ ms}$$

So, $$T_1 = T/2 + T_\theta = 0.516 \text{ ms}$$

and $$T_2 = T/2 - T_\theta = 0.484 \text{ ms}$$



(f)

Fig. 5.9 Circuit for Example 5.3

5.4 SQUARE WAVE GENERATOR (ASTABLE MULTIVIBRATOR)

A simple op-amp square wave generator is shown in Fig. 5.10 (a). Also called a free running oscillator, the principle of generation of square wave output is to force an op-amp to operate in the saturation region. In Fig. 5.10 (a) fraction $\beta = R_2/(R_1 + R_2)$ of the output is fed back to the (+) input terminal. Thus the reference voltage V_{ref} is βv_o and may

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At $t = T_1$, voltage across the capacitor reaches βV_{sat} and switching takes place, Therefore,

$$v_c(T_1) = \beta V_{sat} = V_{sat} - V_{sat}(1+\beta)e^{-T_1/RC} \qquad (5.6)$$

After algebraic manipulation, we get,

$$T_1 = RC \ln \frac{1+\beta}{1-\beta} \qquad (5.7)$$

This give only one half of the period.

Total time period

$$T = 2T_1 = 2RC \ln \frac{1+\beta}{1-\beta} \qquad (5.8)$$

and the output wave form is symmetrical.

If $R_1 = R_2$, then $\beta = 0.5$, and $T = 2RC \ln 3$. And for $R_1 = 1.16R_2$, it can be seen that $T = 2\ RC$

or
$$f_0 = \frac{1}{2RC}$$

The output swings from $+V_{sat}$ to $-V_{sat}$, so,

$$v_o \text{ peak-to-peak} = 2\ V_{sat} \qquad (5.9)$$

The peak to peak output amplitude can be varied by varying the power supply voltage. However, a better technique is to use back to back zener diodes as shown in Fig. 5.10 (c). The output voltage is regulated to $\pm (V_Z + V_D)$ by the zener diodes.

$$v_o \text{ peak-to-peak} = 2\ (V_Z + V_D) \qquad (5.10)$$

Resistor R_{sc} limits the currents drawn from the op-amp to,

$$I_{sc} = \frac{V_{sat} - V_Z}{R_{sc}} \qquad (5.11)$$

This circuit works reasonably well at audio frequencies. At higher frequencies, however, slew-rate of the op-amp limits the slope of the output square wave.

If an asymmetric square wave is desired, then zener diodes with different break down voltages V_{Z1} and V_{Z2} may be used. Then the output is either V_{o1} or V_{o2}, where $V_{o1} = V_{Z1} + V_D$ and $V_{o2} = V_{Z2} + V_D$. It can be easily shown that the positive section is given by,

$$T_1 = RC \ln \frac{1+\beta V_{o2}/V_{o1}}{1-\beta} \qquad (5.12)$$

The duration of negative section T_2 will be the same as given by Eq. (5.12) with V_{o1} and V_{o2} interchanged.

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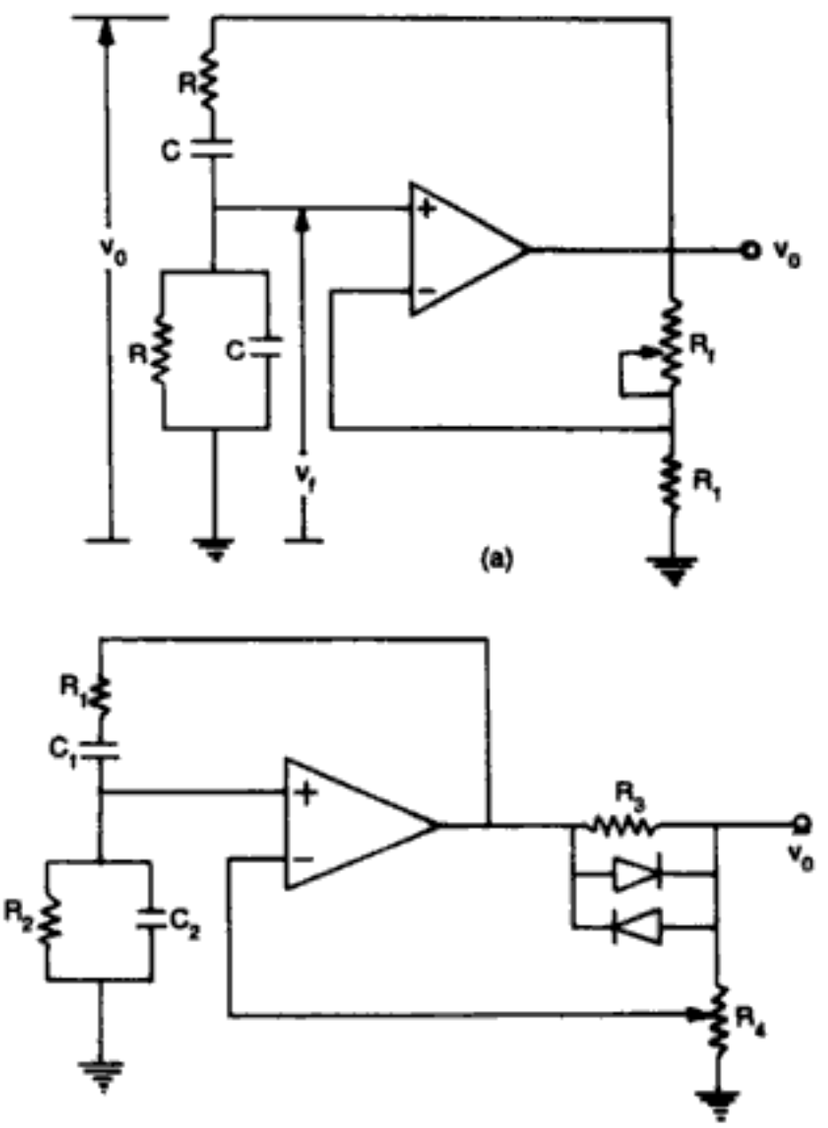

Fig. 5.16 (a) Wien bridge oscillator (b) practical Wien bridge oscillator with adaptive negative feedback

of the amplifier which in turn lowers the output amplitude. Hence sustained oscillations can be obtained. Further, if the output signal falls, the diodes would begin to turn-off thereby increasing R_f which in turn increases gain.

Summary

1. A comparator is an open loop op-amp with analog inputs and a digital output ($\pm V_{sat} \approx V_{cc}$).
2. Reduced output voltage levels can be obtained by using back-to-back zener diodes at the output.
3. Zero crossing detector is a comparator with $V_{ref} = 0$.
4. A window detector determines when an unknown input is between two threshold levels.
5. Schmitt trigger is a comparator with positive feedback.
6. In Schmitt trigger, the input voltage triggers the output every time it exceeds certain voltage levels called upper threshold V_{UT} and lower threshold V_{LT}.

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PROBLEMS

5.1. Draw the input and output waveforms of the op-amp shown in Fig. P. 5.1.

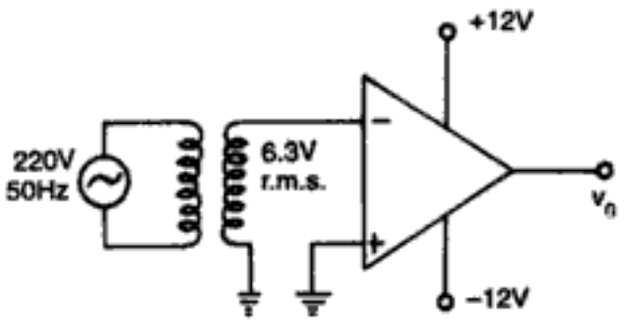

Fig. P. 5.1

5.2. Draw output of the op-amp shown in Fig. P. 5.2. (a) for given v_2 as in Fig. P. 5.2. (b) when (i) $V_1 = 0$ (ii) $V_1 = 4$V.

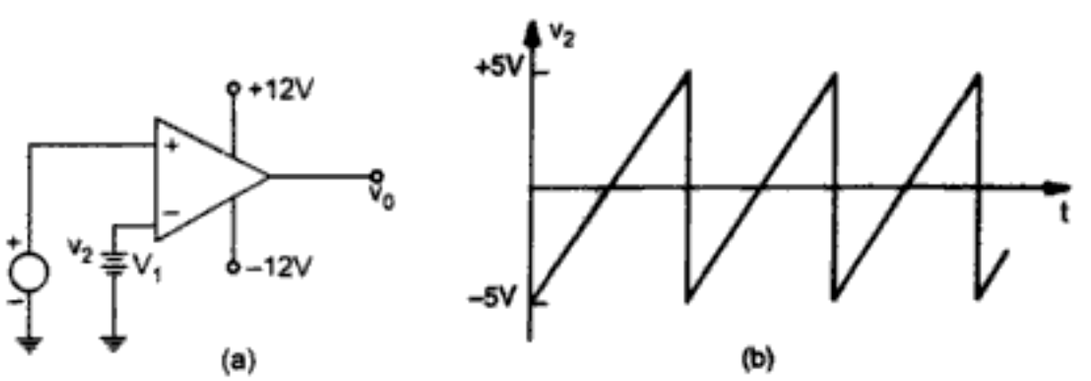

Fig. P. 5.2 (a) & (b)

5.3. For the circuit shown in Fig. P. 5.3., what is the condition of each of the LEDs for (i) $v_i = 1$ V (ii) $v_i = 2$ V.

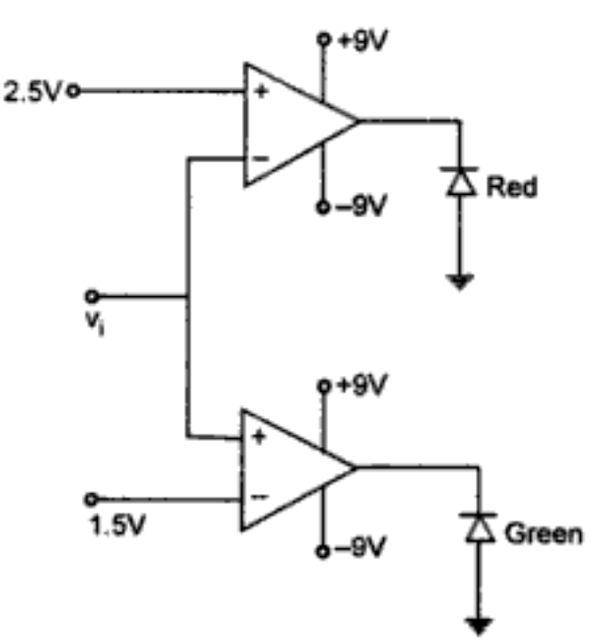

Fig. P. 5.3

5.4. For the circuit shown in Fig. P. 5.4, calculate the trigger points if supply voltage $V = \pm 12$ V. Plot the output voltage v_o vs t if v_i is a 100 Hz triangular wave of magnitude ± 10 V.

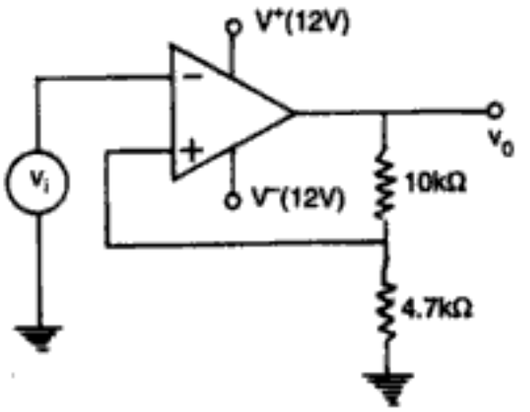

Fig. P. 5.4

5.5. In the circuit of Fig. 5.7 (a) $v_i = 100$ mV peak sine wave at 100 Hz, $R = 1$ kΩ and $V_{Z1} = V_{Z2} = 6.2$ V and the op-amp is a 741 with supply voltages = ± 12 V. Draw the output waveform.

5.6. For the circuit shown in Fig. P.5.6, $v_i = 500$ mV peak 100 Hz sine wave, $R = 100\ \Omega$, $V_Z = 6.2$ V, $V_D = 0.7$ V and supply voltages = ± 15 V. Determine the output voltage swing and draw the output waveform.

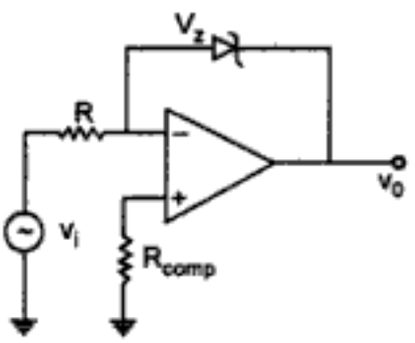

Fig. P. 5.6

5.7. In a Schmitt Trigger of Fig. 5.8 (a) hysteresis of 0.1 V is desired. Calculate V_{ref}, V_{sat} and R_1 if $V_{UT} = V_{ref}$, $A_{OL} = 100{,}000$ and loop gain is 1000 and $R_2 = 1$ kΩ.

5.8. The Schmitt Trigger of Fig. 5.8 (a) uses 9V zener diodes. Calculate R_1/R_2 and V_{ref} if $V_D = 0.7$ V, $V_{UT} = 0$ and $V_H = 0.2$ V.

5.9. (a) In the Schmitt trigger of Fig. 5.8 (a), $v_o = 8$ V, $V_{UT} = 4$ V and $V_{LT} = 3$ V. Calculate R_1/R_2 and V_{ref}.
(b) Calculate the value of V_{ref} so that V_{LT} is negative.
(c) Calculate V_{ref} for $V_{UT} = -V_{LT}$.

5.10. For the non-inverting Schmitt comparator circuit shown in Fig. P. 5.10, calculate the threshold levels V_{UT} and V_{LT} and the hysteresis V_H.

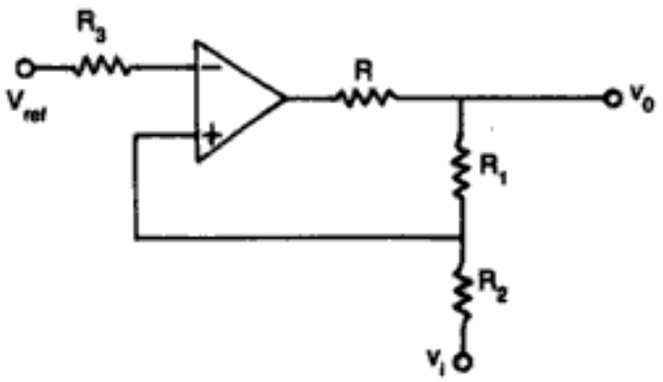

Fig. P. 5.10

5.11. In the square wave oscillator of Fig. 5.10 (a) calculate the frequency of oscillation if $R_2 = 10$ kΩ, $R_1 = 11.6$ kΩ, $R = 100$ kΩ, $C = 0.01$ μF.

5.12. Design a square wave oscillator for $f = 1$ kHz. The op-amp is a 741 with supply voltages ± 15 V.

5.13. Design a monostable multivibrator with trigger pulse shaping which will drive a LED ***on*** for 0.5 second each time it is pulsed.

Experiment 5.1

(a) To study the operation of 741 op-amp as a comparator.
(b) To design a Schmitt trigger for $V_{UT} = +0.5$V and $V_{LT} = -0.5$V and show its use for generating a square wave output.

(a) Comparator

Procedure

1. Connect the circuit shown in Fig. E. 5.1 (a) and adjust the 10 kΩ potentiometer so that $V_{ref} = +0.5$V.
2. Adjust the signal generator so that $v_i = 2$ V pp sine wave at 1 kHz.
3. Using a CRO observe the input and output waveform simultaneously. Plot the output waveform.
4. Adjust the 10 kΩ potentiometer so that $V_{ref} = -0.5$V. Repeat step 3.
5. To make a zero crossing detector, set $V_{ref} = 0$V and observe the output waveforms.

(b) Schmitt Trigger

Design: In Fig. E. 5.1 (b)

$$V_{UT} = \frac{R_2}{R_1 + R_2} V_{sat}$$

and

$$V_{LT} = \frac{R_2}{R_1 + R_2} (-V_{sat})$$

For 741, with supply voltages = ± 15V, the saturation voltage ± V_{sat} = ± 14 V.

So, $$0.5\text{V} = \frac{R_2}{R_1 + R_2}(14\text{ V})$$

Or, $R_1 = 27\ R_2$

Choose, $R_2 = 1\ \text{k}\Omega$

So, $R_1 = 27\ \text{k}\Omega$ (take a 50 kΩ pot)

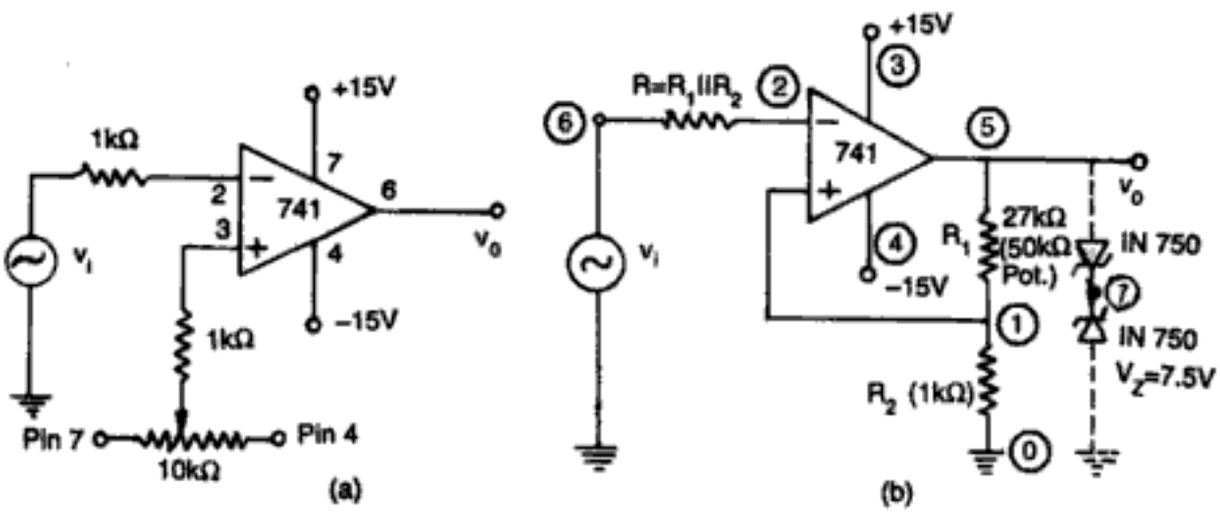

Fig. E. 5.1 (a) Comparator (b) Schmitt trigger

Procedure

1. Connect the circuit of Fig. 5.1(b) with the values obtained in the design. Please note than Fig. E. 5.1(b) has been numbered for PSPICE simulation given in Computer program 5.1.
2. Adjust the signal generator so that $v_i = 2$ V pp sine wave at 1 kHz.
3. Plot the input and output waveforms.
4. Connect two zener diodes (IN 750, $V_z = 7.5$ V) at the output and find value of R_1 to get the same values of V_{UT} and V_{LT}.

Computer Program 5.1 (Schmitt Trigger)

Fig. E. 5.1. (b) has been numbered for PSPICE simulation and its listing is shown below. The input and output waveforms have been shown in Fig. C. 5.1 (a) and (b) for (i) without zener diodes (ii) with zener diodes

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Design equations and component values:

(a) Phase shift oscillator:
In Fig. 5.15,

$$f_o = \frac{1}{2\pi\sqrt{6}\,RC} \text{ and } R_f \geq 29\,R_1$$

Choose $C = 0.1\ \mu F$,

Then $$R = \frac{1}{2\pi\,(500)\,(\sqrt{6})\,(10^{-7})} = 1.3\ k\Omega \text{ (use } 1.5\ k\Omega)$$

To prevent loading, $R_1 \geq 10\,R$
Therefore, take $R_1 = 10\,R = 15\ k\Omega$
$R_f = 29\ R_1 = 29 \times 15\ k\Omega$
$= 435\ k\Omega$
(Use $R_f = 500\ k\Omega$ potentiometer)

(b) Wien bridge oscillator:
In Fig. 5.16(a),

$$f_o = \frac{1}{2\pi\,RC} \text{ and } R_f = 2R_1$$

Choose $C = 0.05\ mF$

So, $$R = \frac{1}{2\pi\,(1000)\,(0.05 \times 10^{-6})} = 3.1\ k\Omega$$

Take $R_1 = 10R = 30\ k\Omega$
and $R_f = 2R_1 = 60\ k\Omega$ (Use 100 kΩ pot)

Procedure

1. Set up the Phase shift oscillator of Fig. 5.15 with the values obtained in the design.
2. See the output waveform on an oscilloscope. Adjust R_f to obtain a sine wave output.
3. Measure the frequency of oscillator and voltage amplitude.
4. Repeat steps 1, 2 and 3 for the Wien bridge oscillator.

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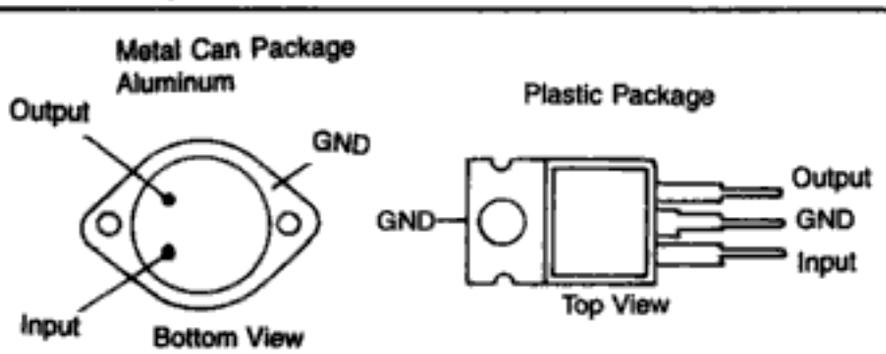
Table 6.1 Electrical characteristics of 7805 voltage regulator

Absolute Maximum Ratings	
Input Voltage (5 V through 18 V)	35 V
(24 V)	40 V
Internal Power Dissipation	Internally limited
Storage Temperature Range	–65°C to + 150°C
Operating Junction Temperature Range	
μA7800	–55°C to + 150°C
μA7800C	0°C to + 125°C

7805C

Electrical Characteristics V_{IN} = 10 V, I_{OUT} = 500 mA, 0°C ≤ T_j ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified.

Characteristic	*Condition*	*Min*	*Typ*	*Max*	*Unit*
Output Voltage	T_j = 25°C	4.8	5.0	5.2	V
Line Regulation	T_j = 25°C, 7 V ≤ V_{IN} ≤ V		3	100	mV
	T_j = 25°C, 8 V ≤ V_{IN} ≤ 12 V		1	50	mV
Load Regulation	T_j = 25°C, 5 mA ≤ I_{OUT} ≤ 1.5 A		15	100	mV
	T_j = 25°C, 250 mA ≤ I_{OUT} ≤ 750 mA		5	50	mV
Output voltage	7 V ≤ V_{IN} ≤ 20 V, 5 mA ≤ I_{OUT} ≤ 1.0 A, P ≤ 15 W	4.75		5.25	V
Quiescent Current	T_j = 25°C		4.2	8.0	mA
Quiescent Current Change with line	7 V ≤ V_{IN} ≤ 25 V			1.3	mA
Quiescent Current Change with load	5 mA ≤ I_{OUT} ≤ 1.0 A			0.5	mA
Output Noise Voltage	T_A = 25°C, 10 Hz ≤ 1 ≤ 100 kHz		40		μV
Ripple Rejection	f = 120 Hz, 8 V ≤ V_{IN} ≤ 18 V	62	78		dB
Dropout Voltage	I_{OUT} = 1.0 A, T_j = 25°C		2.0		V
Output Resistance	f = 1 kHz		17		mΩ
Short-Circuit Current	T_j = 25°C. V_{IN} = 35 V		750		mA
Peak Output Current	T_j = 25°C		2.2		A
Average Temperature coefficient of output voltage	I_{OUT} = 5 mA, 0°C ≤ T_j ≤ 125°C		1.1		mV/°C



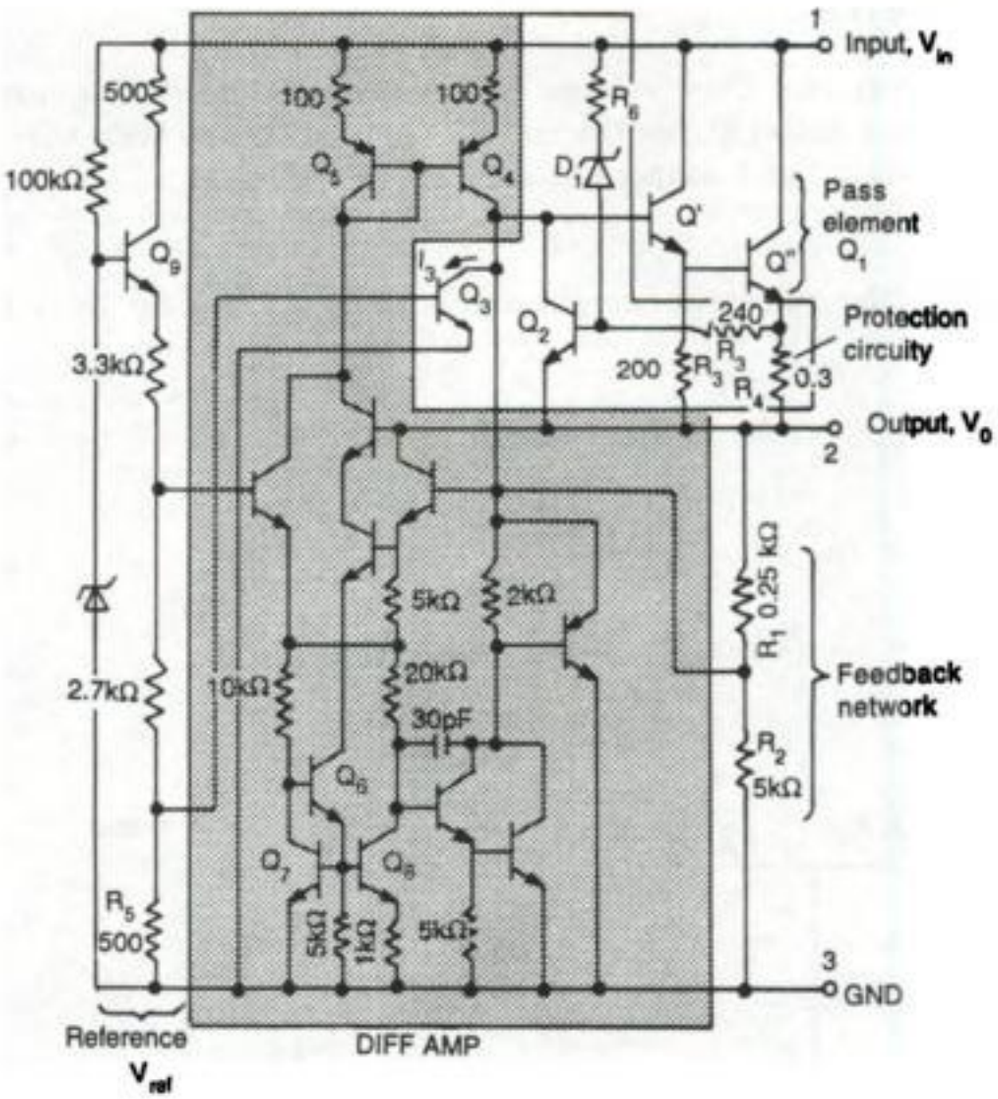


Fig. 6.3 Schematic diagram for MC 7800C series monolithic regulator

The monolithic regulator has in-built circuitry enclosed in the solid line to provide:

Over-current protection.

Thermal overload protection.

Current is limited by R_3, R_4 and transistor Q_2. If the output voltage goes low due to overload, the excess voltage appears across the pass element (Q' Q''), that is, across the collector emitter of Q''. When this voltage is more than the break-down voltage of the zener diode D_1, it starts conducting. This provides sufficient base current to transistor Q_2 and drives it ***on***. Now, because of the collector current of Q_2 when fully ***on***, current flowing to the base of Q' is reduced. This in turn reduces the conduction of Q''. Thus the volt-ampere product of the pass element (Q' Q'') is limited.

The thermal overload protection is provided by the resistor R_5 and transistor Q_3. The voltage drop across resistor R_5 is directly applied to the base-emitter of Q_3. When the temperature goes high, Q_3 conducts more, thereby reducing the base drive of $Q'Q''$ combination. This provides thermal protection.

Current Source

The three terminal fixed voltage regulator can be used as a current source. Figure 6.4(a) shows the circuit where 7805 has been wired to supply a current of 1 ampere to a 10 Ω, 10 watt load.

$$I_L = I_R + I_Q \tag{6.2}$$

where I_Q is the quiescent current and is about 4.2 mA for 7805. (See Table 6.1)

$$I_L = \frac{V_R}{R} + I_Q \tag{6.3}$$

Since I_L = 1A, $$\frac{V_R}{R} \simeq 1\text{A} \quad (I_Q << I_L) \tag{6.4}$$

Also V_R = 5 V (Voltage between terminal 2 and 3)

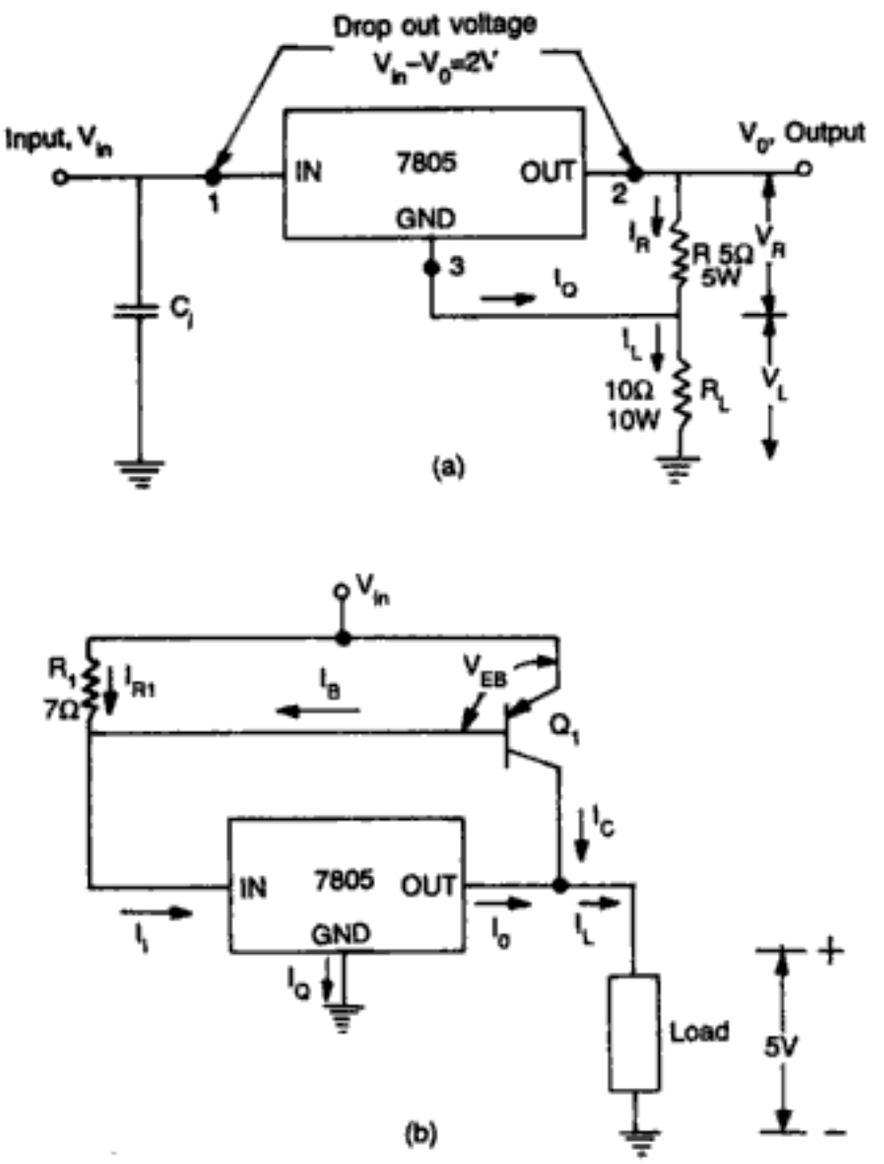


Fig. 6.4 (a) IC 7805 as a current source
(b) Boosting a three terminal regulator

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Solution

Load = 100Ω

For 7805, the output voltage across the load will be 5V.

$$I_L = 5V/100\Omega = 0.05A = 50 \text{ mA}$$

The voltage across R_1 is $7\Omega \times 50$ mA = 350 mV which is less than 0.7V. Hence Q_1 is ***off***.

So, $I_L = I_o = I_i = 50$ mA

and $I_c = 0$

Load = 5Ω

$$I_L = 5V/5\Omega = 1A$$

Assume that the entire current comes through regulator and that Q_1 is ***off***. Now the voltage drop across R_1 is equal to $7\Omega \times 1A = 7V$. Thus our assumption is wrong and Q_1 is ***on***. Putting the values in Eq. (6.10), it can be found that

$$I_o = 196 \text{ mA}$$

$$I_c = 904 \text{ mA}$$

Load = 1Ω

$$I_L = 5V/1\Omega = 5A$$

Here also Q_1 is ***on***. Solving Eq. (6.10) for I_o, we get

$$I_o = 446 \text{ mA}$$

so, $I_c = 4.55$ A

Fixed Regulator used as Adjustable Regulator

In the laboratory, one may need variable regulated voltages or a voltage that is not available as standard fixed voltage regulator. This can be achieved by using a fixed three terminal regulator as shown in Fig. 6.5. Note that the ground (GND) terminal of the fixed three terminal regulator is floating. The output voltage

$$V_o = V_R + V_{pot}$$

$$= V_R + (I_Q + I_{R1})\, R_2$$

$$= V_R + I_Q R_2 + \frac{V_R}{R_1} R_2$$

or, $$V_o = (1 + R_2/R_1)\, V_R + R_2 I_Q \qquad (6.12)$$

where V_R is the regulated voltage difference between the OUT and GND terminals. The effect of I_Q is minimized by choosing R_2 small enough to minimize the term $I_Q R_2$. The minimum output voltage is the value of the fixed voltage available from the regulator. The LM117,

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properly, both diodes will be reverse biased and will no longer have any effect on the circuit.

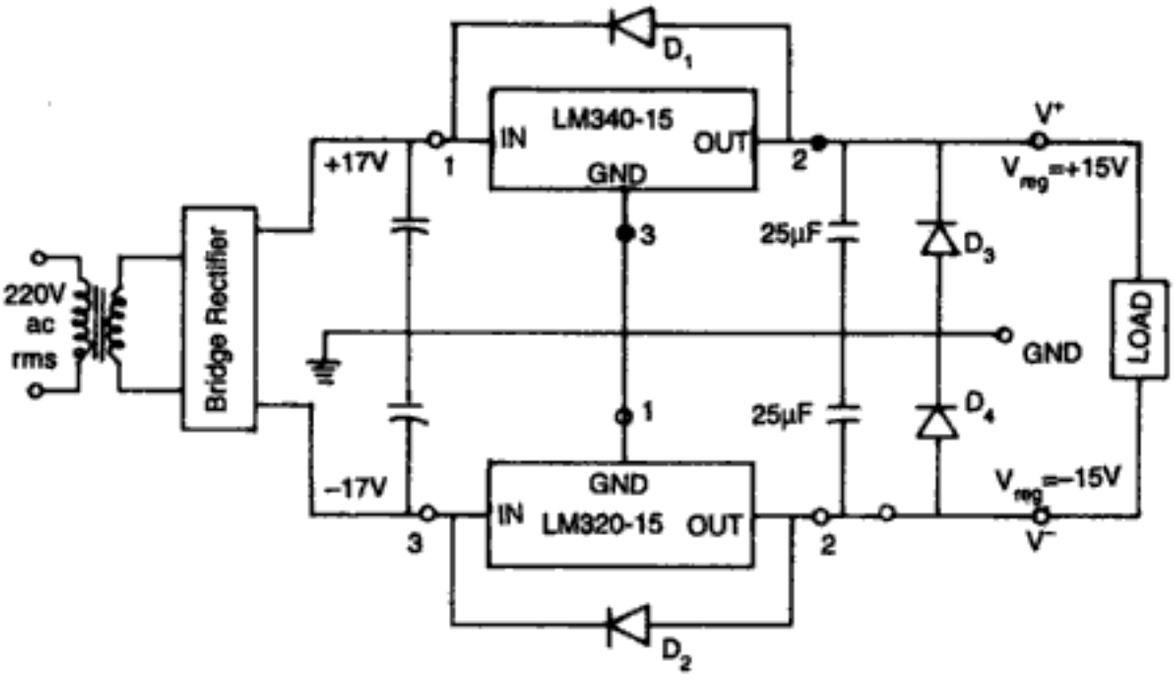


Fig. 6.6 A dual voltage (± 15V) supply

An op-amp draws less than 5 mA current, so a 100 mA supply can be used to drive a circuit consisting of 20 op-amps. LM 325H is a dual tracking ± 15V supply and is available in a 10-pin metal-can package and can furnish current upto 100 mA.

6.4 723 GENERAL PURPOSE REGULATOR

The three terminal regulators discussed earlier have the following limitations:

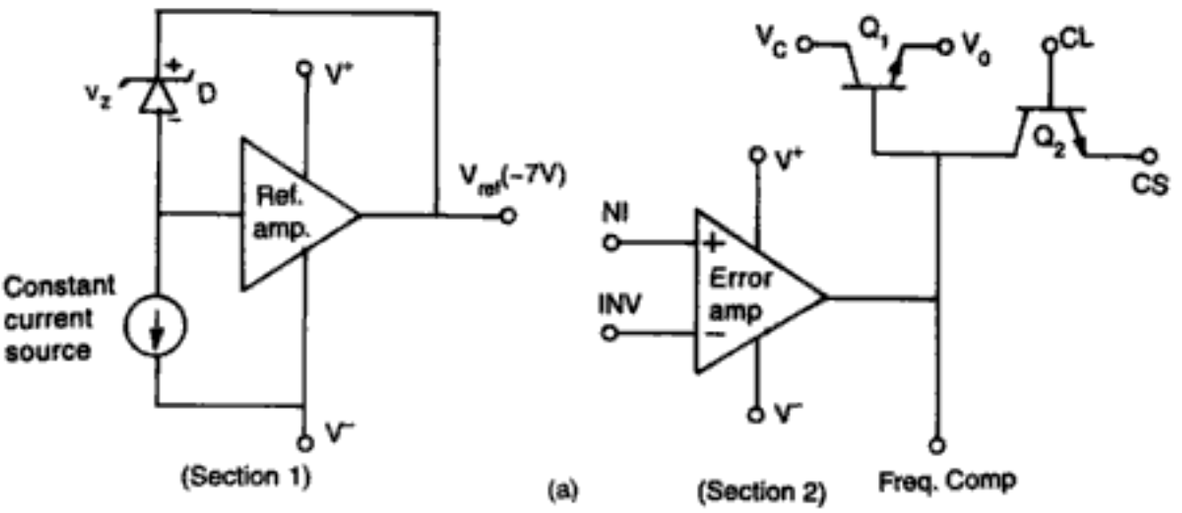
1. Not short circuit protection
2. Output voltage (positive or negative) is fixed.

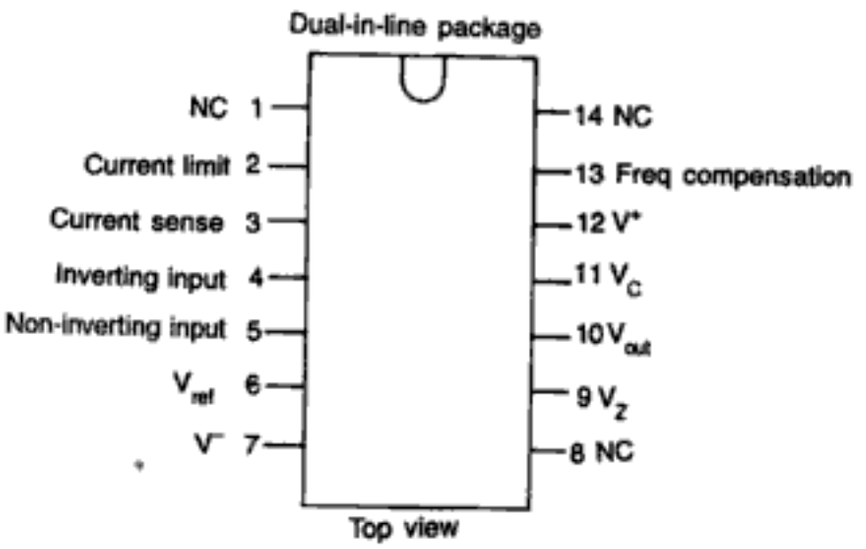
These limitations have been overcome in the 723 general purpose regulator, which can be adjusted over a wide range of both positive or negative regulated voltage. This IC is inherently low current device, but can be boosted to provide 5 amps or more current by connecting external components. The limitation of 723 is that it has no in-built thermal protection. It also has no short circuit current limits.

Figure 6.7 (a) shows the functional block diagram of a 723 regulator IC. It has two separate sections. The zener diode, a constant current source and reference amplifier produce a fixed voltage of about 7 volts at the terminal V_{ref}. The constant current source forces the zener to operate at a fixed point so that the zener outputs a fixed voltage.

The other section of the IC consists of an error amplifier, a series pass transistor Q_1 and a current limit transistor Q_2. The error amplifier compares a sample of the output voltage applied at the INV input terminal to the reference voltage V_{ref} applied at the NI input terminal.

The error signal controls the conduction of Q_1. These two sections are not internally connected but the various points are brought out on the IC package. 723 regulated IC is available in a 14-pin dual-in-line package or 10-pin metal-can as shown in Fig. 6.7(b). The important features and electrical characteristics are given in Table 6.2.





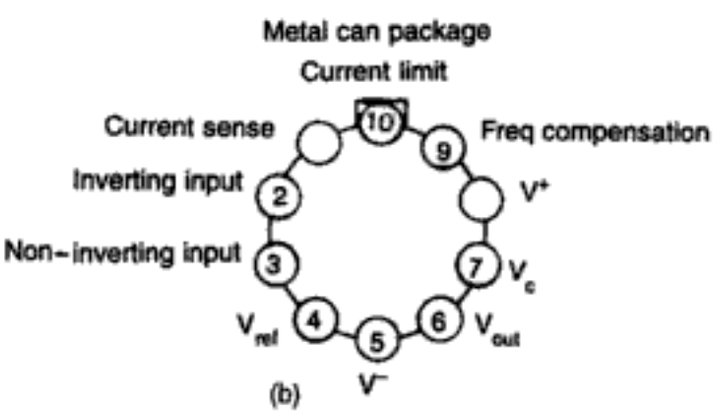


Fig. 6.7 (a) Functional block diagram of 723 regulator
(b) Pin diagram for 14-pin DIP and 10-pin metal can

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Current Foldback

In current limiting technique, the load current is maintained at a present value and when overload condition occurs, the output voltage V_0 drops to zero. However, if the load is short circuited, maximum current does flow through the regulator. To protect the regulator, one must devise a method which will limit the short circuit current and yet allow higher currents to the load.

Current foldback is the method used for this. Figure 6.10(a) shows the current foldback characteristic curve. As current demand increases, the output voltage is held constant till a present current level (I_{knee}) is reached. If the current demand exceeds this level, both output voltage and output current decrease. The circuit in Fig. 6.10(b) shows the method of applying current foldback. In order to understand the operation of the circuit, consider the circuit of Fig. 6.10(c). The voltage at terminal CL is divided by $R_3 - R_4$ network. The current limit transistor Q_2 conducts only when the drop across the resistance R_{sc} is large enough to produce a base-emitter voltage of Q_2 to be at least

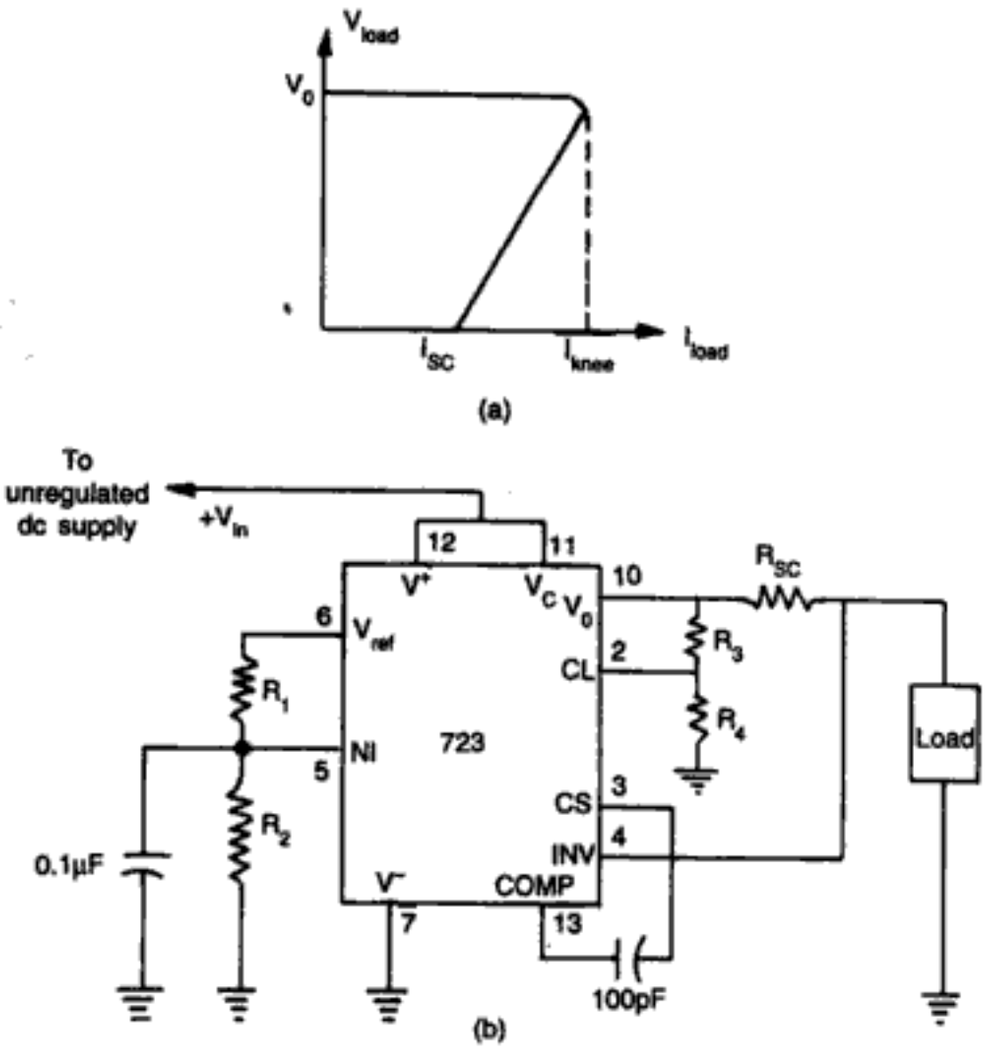

Fig. 6.10 (a) Current fold back characteristic curve (b) A low voltage regulator using current fold back

0.5 V. As Q_2 starts conducting, transistor Q_1 begins to turn off and the current I_L decreases. This reduces the voltage V_1 at the emitter of Q_1 and also the output voltage V_o. The voltage at the base of Q_2 (CL) will be $V_1R_4/(R_3 + R_4)$. Thus the voltage at the CL terminal drops by a smaller amount compared to the drop in voltage at CS terminal. This increases V_{BE} of Q_2 thereby increasing the conduction of Q_2, which in turn reduces the conduction of Q_1. That is, the current I_L further reduces. This process continues till $V_o = 0$V and V_1 is just large enough to keep 0.5V between CL and CS terminal. This point is I_{sc} and has been reduced by lowering both I_L and V_o.

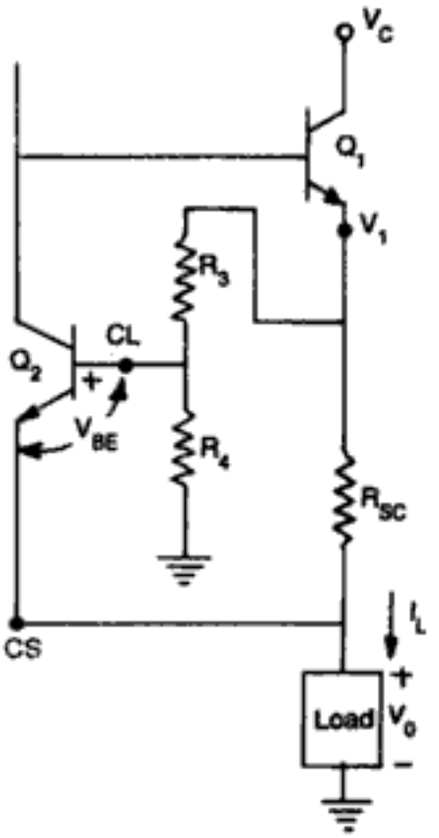

Fig. 6.10 (c) Current fold back (partial schematic)

Current Boosting

The maximum current that 723 IC regulator can provide is 140 mA. For many applications, this is not sufficient. It is possible to boost the current level simply by adding a boost transistor Q_1 to the voltage regulator as shown in Fig. 6.11. The collector current of the pass transistor Q_1 comes from the unregulated dc supply. The output current from V_o terminal drives the base of the pass transistor Q_1. This base current gets multiplied by the beta of the pass transistor, so that 723 has to provide only the base current. So,

$$I_{load} = \beta_{pass\ transistor} \times I_{o\ (723)} \qquad (6.19)$$

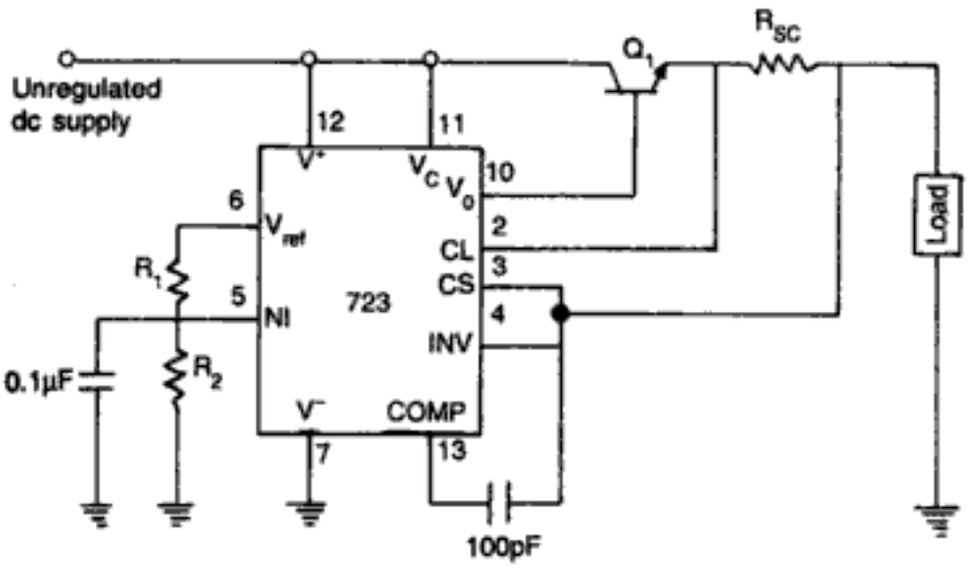

Fig. 6.11 Current boosted low voltage regulator

6.5 SWITCHING REGULATOR

The regulated power supplies discussed so far are referred to as linear voltage regulator, since the series pass transistor operates in the linear region. The linear voltage regulator has the following limitations.

The input stepdown transformer is bulky and the most expensive component of the linear regulated power supply mainly because of low line frequency (50 Hz). Because of the low line frequency, large values of filter capacitors are required to decrease the ripple. The efficiency of a series regulator is usually very low (typically 50 percent). The input voltage must be greater than the output voltage. The greater the difference in input-output voltage, more will be the power dissipated in the series pass transistor which is always in the active region. A TTL system regulator (V_o = 5V) when operated at 10V dc input gives 50 percent efficiency and only 25 percent for 20V dc input. Another limitation is that in a system with one dc supply voltage (such as + 5V for TTL) if there is need for ± 15V for op-amp operation, it may not be economically and practically feasible to achieve this.

Switched mode power supplies overcome these difficulties. The switching regulator, also called switched mode regulator operate in a significantly different way from that of a conventional series regulator circuit discussed earlier. In series regulator, the pass transistor is operated in its linear region to provide a controlled voltage drop across it with a steady dc current flow. Whereas, in the case of switched-mode regulator, the pass transistor is used as a "controlled switch" and is operated at either cutoff or saturated state. Hence the power transmitted across the pass device is in discrete pulses rather than as a steady current flow. Greater efficiency is achieved since the pass device is operated as a low impedance switch. When the pass device is at cutoff, there is no current and dissipates no power. Again when

the pass device is in saturation, a negligible voltage drop appears across it and thus dissipates only a small amount of average power, providing maximum current to the load. In either case, the power wasted in the pass device is very little and almost all the power is transmitted to the load. Thus efficiency in switched mode power supply is remarkably high–in the range of 70–90%.

Switched mode regulators rely on pulse width modulation to control the average value of the output voltage. The average value of a repetitive pulse waveform depends on the area under the waveform. If the duty cycle is varied as shown in Fig. 6.12, the average value of the voltage changes proportionally.

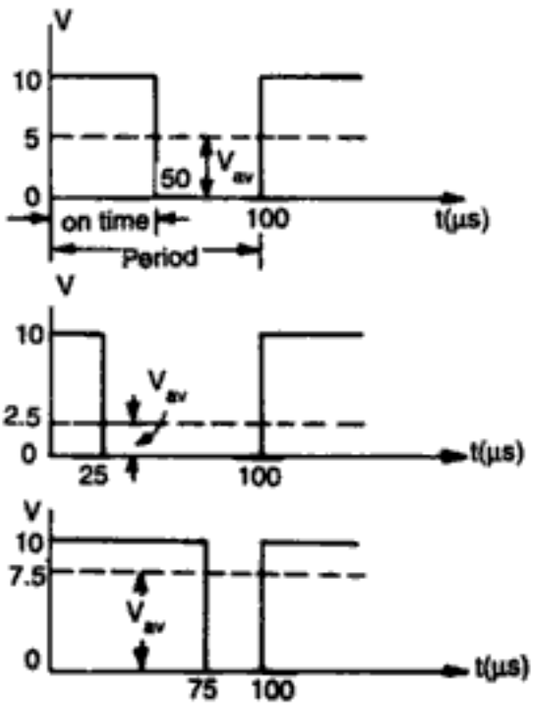

Fig. 6.12 Pulse width modulation and average value

A switching power supply is shown in Fig. 6.13. The bridge rectifier and capacitor filters are connected directly to the ac line to give unregulated dc input. The thermistor R_t limits the high initial capacitor charge current. The reference regulator is a series pass regulator of the type shown in Fig. 6.1. Its output is a regulated reference voltage V_{ref} which serves as a power supply voltage for all other circuits. The current drawn from V_{ref} is usually very small (~ 10 mA), so the power loss in the series pass regulator does not affect the overall efficiency of the switched mode power supply (SMPS). Transistors Q_1 and Q_2 are alternately switched ***off*** and ***on*** at 20 kHz. These transistors are either fully ***on*** ($V_{CE\ sat}$ ~ 0.2V) or cut-off, so they dissipate very little power. These transistors drive the primary of the main transformer. The secondary is centre-tapped and full wave rectification is achieved by diodes D_1 and D_2. This unidirectional square wave is next filtered through a two stage *LC* filter to produce output voltage V_o.

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The regulation of V_o is achieved by the feedback circuit consisting of a pulse-width modulator and steering logic circuit. The output voltage V_o is sampled by a R_1R_2 divider and a fraction $R_1/(R_1+R_2)$ is compared with a fixed reference voltage V_{ref} in comparator 1. The output of this voltage comparison amplifier is called $V_{control}$ and is shown in Fig. 6.14 (a). $V_{control}$ is applied to the (–) input terminal of comparator 2 and a triangular waveform of frequency 40 kHz (also shown in Fig. 6.14 (a)) is applied at the (+) input terminal. It may be noted that a high frequency triangular waveform is being used to reduce the ripple. The comparator 2 functions as a pulse width modulator and its output is a square wave v_A (Fig. 6.14 (b)) of period $T(f = 40$ kHz). The duty cycle of the square wave is $T_1/(T_1 + T_2)$ and varies with $V_{control}$ which in turn varies with the variation of v_o. The output v_A drives a steering logic circuit shown in the dashed block. It consists of a 40 kHz oscillator cascaded with a flip-flop to produce two complementary outputs v_Q and $v_{\overline{Q}}$ shown in Fig. 6.14 (d) and (e). The output v_{A1} and v_{A2} of AND gates A_1 and A_2 are shown in Fig. 6.10 (f) and (g). These waveforms are applied at the base of transistor Q_1 and Q_2. Depending upon whether transistor Q_1 or Q_2 is ***on***, the waveform at the input of the transformer will be a square wave as shown in Fig. 6.14 (h). The rectified output v_B is shown in Fig. 6.14 (i).

An inspection of Fig. 6.13 shows that the output current passes through the power switch consisting of transistors Q_1 and Q_2, inductor having low resistance and the load. Hence using a switch with low losses (transistor with small $V_{CE\,(sat)}$ and high switching speed) and a filter with high quality factor, the conversion efficiency can easily exceed 90%.

If there is a rise in dc output voltage V_o, the voltage control $V_{control}$ of the comparator 1 also rises. This changes the intersection of the $V_{control}$ with the triangular waveform and in this case decreases the time period T_1 in the waveform of Fig. 6.14 (b). This in turn decreases the pulse width of the waveform driving the main power transformer. Reduction in pulse width lowers the average value of the dc output V_o. Thus the initial rise in the dc output voltage V_o has been nullified.

So far we have discussed the operation of the SMPS. Now we shall be able to justify why SMPS has better efficiency than linear regulated power supply. We have noted that very high frequency signals (about 40 kHz or more) are being applied. The transistors Q_1 and Q_2 are acting as the switches and become alternately ***on*** and ***off*** at a frequency of 20 kHz (Fig. 6.14 (a)). Again the transistor Q_1 or Q_2 is ***on*** for very small duration and consumes negligibly small power since $V_{CE\,(sat)}$ (0.2V) is small. It may also be noted that the high operating frequency used for the switching transistors allows the use of smaller transformers, capacitors and inductors. This allows a decrease in size and cost.

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(vi) Replace R_L with a short circuit and measure the load current. This gives I_{sc}.

(vii) Make $R_{sc} = 0$. With $V_{in} = 10V$, measure and record I_L and V_L for I_L: 5 mA, 10 mA, upto $I_{L\,(max)}$ where $I_{L\,(max)}$ is 5 mA greater than the value of I_{sc} measured in step (vi).
Caution: Do not short circuit the output of the regulator. It is better to connect a 100 Ω resistor in series with R_L to avoid accidental short circuit.

(viii) With $R_{sc} = 0$, adjust R_L for a load current I_L of 1 mA. To determine line regulation, measure and record V_L for V_{in}: 10V, 15V, ... upto 35V in 5V increments. Calculate percent line regulation.

Procedure (c)

(i) Connect the current foldback circuit shown in Fig. E. 6.1. (c).

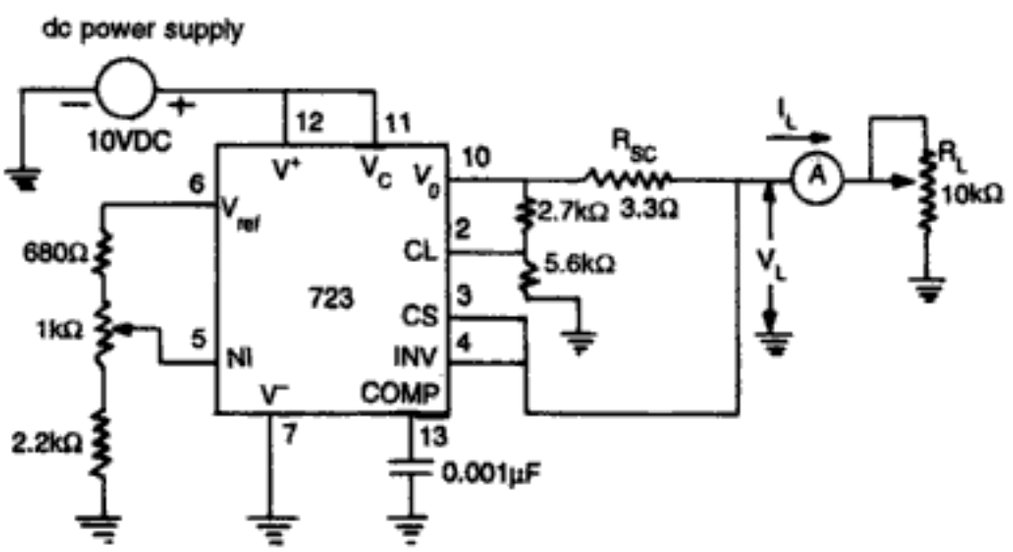


Fig. E. 6.1 (c) Current foldback circuit

(ii) Adjust R_L (10 kΩ-pot) and gradually increase the load current I_L until you observe a sudden reduction in V_L and I_L. The point at which this drop begins is the knee of the current foldback. By adjusting R_L, measure and record I_L and V_L in the vicinity of the knee and plot the current foldback characteristic. Measure V_{sc} across R_{sc} at the knee.

(iii) Replace R_L with a short circuit and record the short circuit load current.

7

Active Filters

7.1 INTRODUCTION

Electric filters are used in circuits which require the separation of signals according to their frequencies. Filters are widely used in communication and signal processing and in one form or another in almost all sophisticated electronic instruments. Such filters can be built from, (i) passive RLC components, (ii) crystals or (iii) resistors, capacitors and op-amps (active filters). In this chapter, we are discussing (i) RC active filters and (ii) switched capacitor filters. Further, active filters in its low-pass, high-pass, band-pass, band elimination configuration and state variable filter have been discussed.

7.2 RC ACTIVE FILTERS

A frequency selective electric circuit that passes electric signals of specified band of frequencies and attenuates the signals of frequencies outside the band is called an electric filter. Filters may be analog or digital. Our point of discussion, in this chapter, will be analog filters.

The simplest way to make a filter is by using passive components (resistors, capacitors, inductors). This works well for high frequencies, that is, radio frequencies. However, at audio frequencies, inductors become problematic, as the inductors become large, heavy and expensive. For low frequency application, more number of turns of wire must be used which in turn adds to the series resistance degrading inductor's performance, i.e. low Q, resulting in high power dissipation.

The active filters overcome the aforementioned problems of the passive filters. They use op-amp as the active element, and resistors and capacitors as the passive elements. The active filters, by enclosing a capacitor in the feedback loop, avoid using inductors. In this way, inductorless active RC filters can be obtained. Also, as op-amp is used in non-inverting configuration, it offers high input impedance and low output impedance. This will improve the load drive capacity and the

load is isolated from the frequency determining network. Because of the high input impedance of the op-amp, large value resistors can be used, thereby reducing the value (size and cost) of the capacitors required in the design.

The active filters have their limitation too. High frequency response is limited by the gain-bandwidth (GBW) product and slew rate of the op-amp. Moreover, the high frequency active filters are more expensive than the passive filters. The passive filter in high frequency range is a more economic choice for applications.

The most commonly used filters are:

Low Pass Filter	(LPF)
High Pass Filter	(HPF)
Band Pass Filter	(BPF)
Band Reject Filter	(also called Band Stop Filter) (BSF)

The frequency response of these filters is shown in Fig. 7.1, where dashed curve indicates the ideal response and solid curve shows the

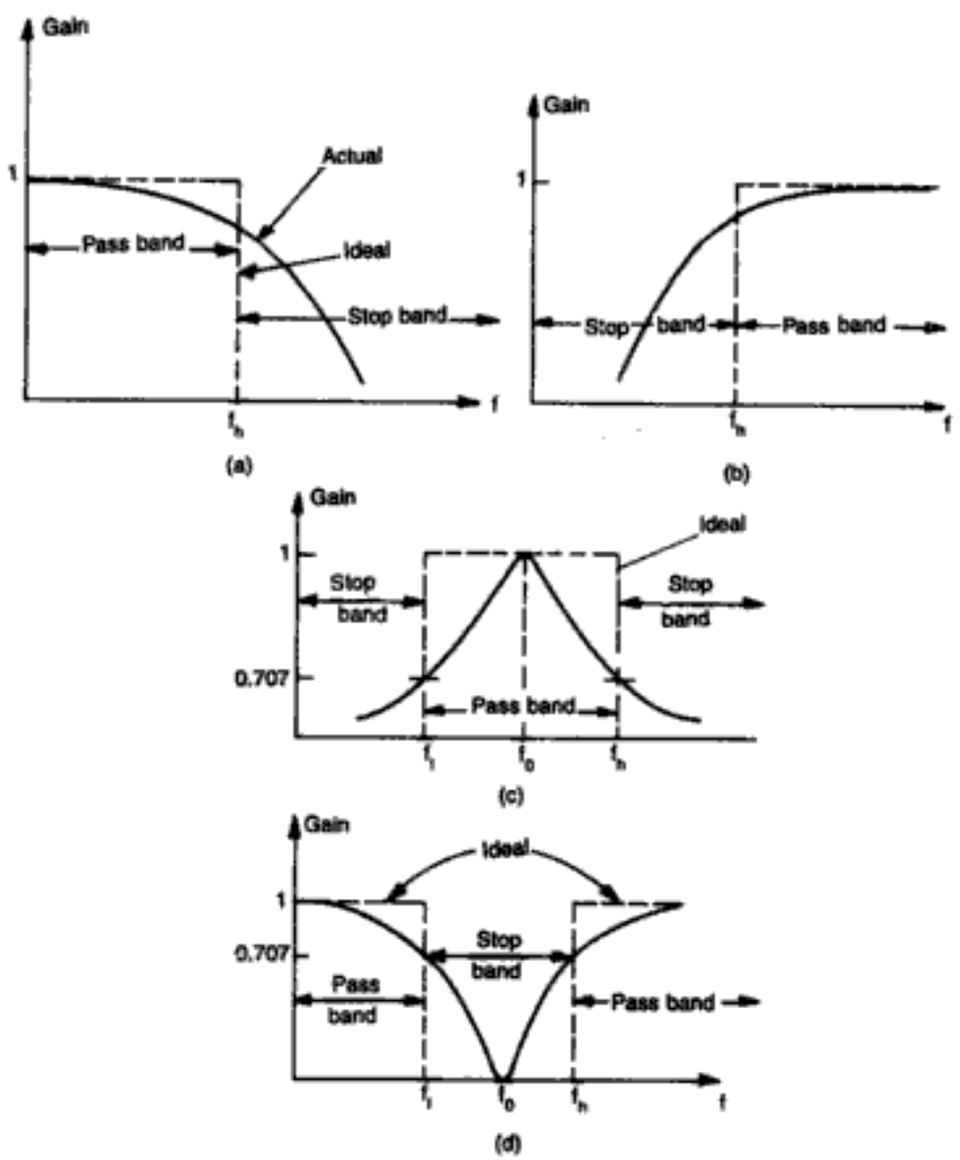


Fig. 7.1 Frequency response of filters (a) low-pass (b) high-pass (c) band pass (d) band reject

practical filter response. It is not possible to achieve ideal characteristics. However, with special design techniques it is possible to closely approximate the ideal response.

Active filters are typically specified by the voltage transfer function,

$$H(s) = \frac{V_0(s)}{V_i(s)}$$

Under steady state conditions, (i.e., $s = j\omega$)

$$H(j\omega) = |H(j\omega)| e^{j\phi(\omega)} \tag{7.1}$$

where $|H(j\omega)|$ is the magnitude or the gain function and $\phi(\omega)$ is the phase function. Usually the magnitude response is given in dB as

$$20 \log |H(j\omega)| \tag{7.2}$$

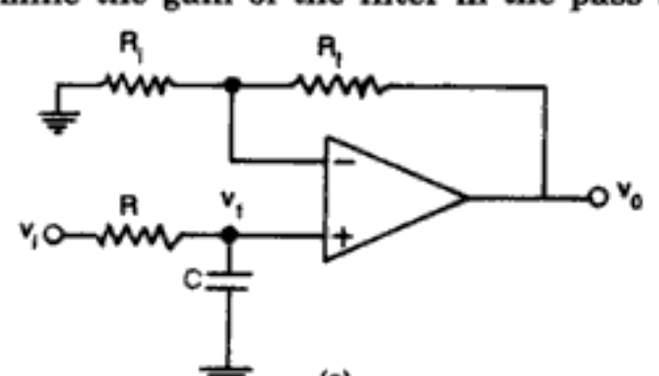
and the phase response is given in degrees as

$$-\phi(\omega) \times 57.296 \text{ degrees} \tag{7.3}$$

Sometimes, active filters are specified by a loss function $V_i(s)/V_0(s)$. The use of loss function is a carry over from passive filter design.

7.2.1 First Order Low Pass Filter

Active filters may be of different orders and types. A first order filter consists of a single RC network connected to the (+) input terminal of a non-inverting op-amp amplifier and is shown in Fig. 7.2 (a). Resistors R_i and R_f determine the gain of the filter in the pass band.



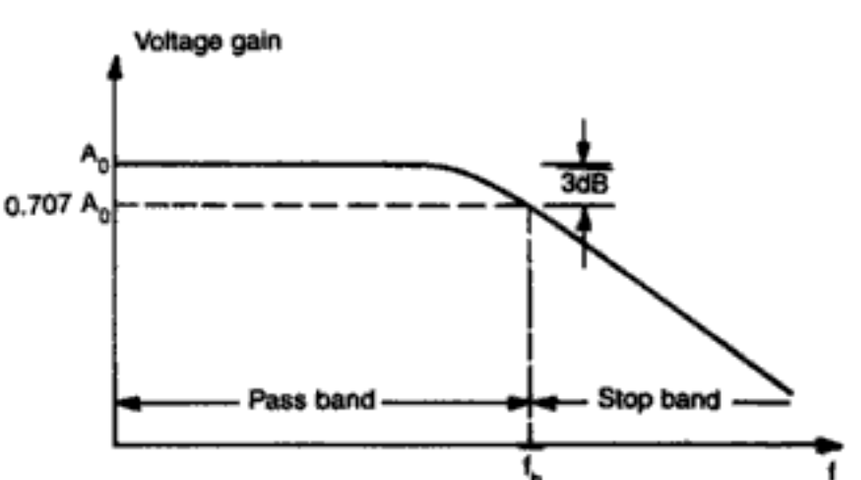


Fig. 7.2 (a) First order low-pass filter (b) Frequency response

The voltage v_1 across the capacitor C in the s-domain is

$$V_1(s) = \frac{\frac{1}{sC}}{R + \frac{1}{sC}} V_i(s)$$

so, $$\frac{V_1(s)}{V_i(s)} = \frac{1}{RCs + 1} \tag{7.4}$$

where $V(s)$ is the Laplace transform of v in time domain.

The closed loop gain A_o of the op-amp is,

$$A_o = \frac{V_o(s)}{V_1(s)} = \left(1 + \frac{R_f}{R_i}\right) \tag{7.5}$$

So, the overall transfer function from Eq. (7.4) and (7.5) is

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{V_o(s)}{V_1(s)} \cdot \frac{V_1(s)}{V_i(s)} = \frac{A_o}{RCs + 1} \tag{7.6}$$

Let $$\omega_h = \frac{1}{RC} \tag{7.7}$$

Therefore, $$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{A_o}{\frac{s}{\omega_h} + 1} = \frac{A_o \omega_h}{s + \omega_h} \tag{7.8}$$

This is the standard form of the transfer function of a first order low-pass system.

To determine the frequency response, put $s = j\omega$ in Eq. (7.8). Therefore, we get

$$H(j\omega) = \frac{A_o}{1 + j\omega RC} = \frac{A_o}{1 + j(f/f_h)} \tag{7.9}$$

where $$f_h = \frac{1}{2\pi RC} \text{ and } f = \frac{\omega}{2\pi}$$

At very low frequency, i.e. $f << f_h$

$$|H(j\omega)| \simeq A_o \tag{7.10}$$

At $f = f_h$,

$$|H(j\omega)| = \frac{A_o}{\sqrt{2}} = 0.707\, A_o \tag{7.11}$$

At very high frequency i.e. $f >> f_h$

$$|H(j\omega)| << A_o \simeq 0 \tag{7.12}$$

The frequency response of the first order low pass filter is shown in Fig. 7.2 (b). It has the maximum gain, A_o at $f = 0$ Hz. At f_h the gain falls to 0.707 time (i.e. –3 dB down) the maximum gain (A_o). The frequency range from 0 to f_h is called the pass band. For $f > f_h$ the gain decreases at a constant rate of –20 dB/decade. That is, when the frequency is increased ten times (one decade), the voltage gain is divided by ten or in terms of dBs, the gain decreases by 20 dB (= 20 log 10). Hence, gain rolls off at the rate of 20 dB/decade or 6 dB/octave after frequency, f_h. The frequency range $f > f_h$ is called the stop band. Obviously, the low pass filter characteristics obtained is not an ideal one as the rate of decay is small for the first order filter.

7.2.2 Second Order Active Filter

An improved filter response can be obtained by using a second order active filter. A second order filter consists of two *RC* pairs and has a roll-off rate of – 40 dB/decade. A general second order filter (Sallen-Key filter) is shown in Fig. 7.3. The results derived here can be used for analysing low pass and high pass filters.

The op-amp is connected as non-inverting amplifier and hence,

$$v_o = \left(1 + \frac{R_f}{R_i}\right) v_B = A_o v_B \tag{7.13}$$

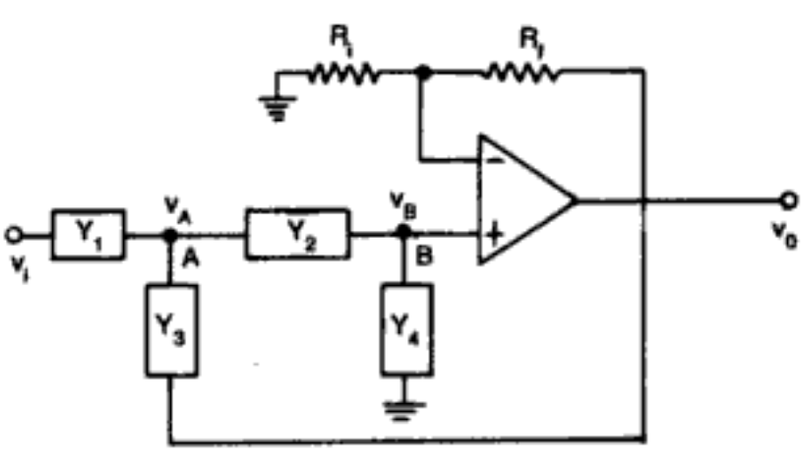


Fig. 7.3 Sallen-Key filter (General second order filter)

where $$A_o = 1 + \frac{R_f}{R_i} \tag{7.14}$$

and v_B is the voltage at node *B*.

Kirchhoff's current law (KCL) at node A gives

$$v_i Y_1 = v_A(Y_1 + Y_2 + Y_3) - v_o Y_3 - v_B Y_2$$

$$= v_A (Y_1 + Y_2 + Y_3) - v_o Y_3 - \frac{v_o Y_2}{A_o} \tag{7.15}$$

where v_A is the voltage at node *A*.

KCL at node B gives,

$$v_A Y_2 = v_B(Y_2 + Y_4) = \frac{v_o(Y_2 + Y_4)}{A_o}$$

$$v_A = \frac{v_o(Y_2 + Y_4)}{A_o Y_2} \tag{7.16}$$

Substituting Eq. (7.16) in Eq. (7.15) and after simplification, we get the voltage gain as

$$\frac{v_o}{v_i} = \frac{A_o Y_1 Y_2}{Y_1 Y_2 + Y_4(Y_1 + Y_2 + Y_3) + Y_2 Y_3 (1 - A_o)} \tag{7.17}$$

To make a low pass filter, choose, $Y_1 = Y_2 = 1/R$ and $Y_3 = Y_4 = sC$ as shown in Fig. 7.4. For simplicity, equal components have been used.

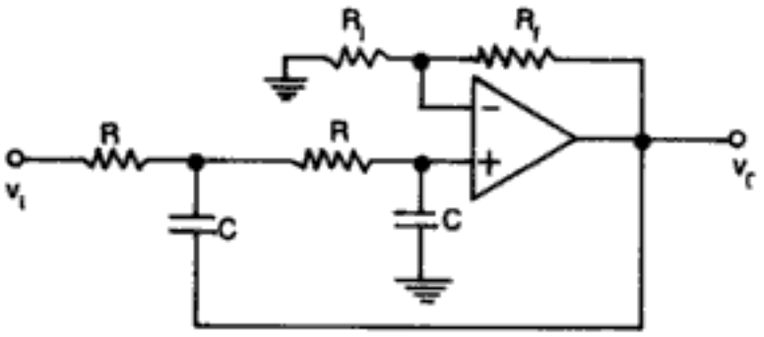


Fig. 7.4 Second order low-pass filter

From Eq. (7.17), we get the transfer function $H(s)$ of a low pass filter as,

$$H(s) = \frac{A_o}{s^2 C^2 R^2 + sCR(3 - A_o) + 1} \tag{7.18}$$

This is to note that from Eq. (7.18), $H(0) = A_o$ for $s = 0$ and $H(\infty) = 0$ for $s = \infty$ and obviously the configuration is for low pass active filter. It may be noted that for minimum dc offset $R_i R_f/(R_f + R_i) = R + R = 2R$ should be satisfied.

Second order physical systems have been studied extensively since long back and their step response, damping coefficient and its cause and effect relationship are known. We shall exploit those ideas in case of second order RC active filter. The transfer function of low pass second order system (electrical, mechanical, hydraulic or chemical) can be written as,

$$H(s) = \frac{A_o \omega_h^2}{s^2 + \alpha \omega_h s + \omega_h^2} \tag{7.19}$$

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coefficient of 1.73. This gives better pulse response, however, causes attenuation in the upper end of the pass band.

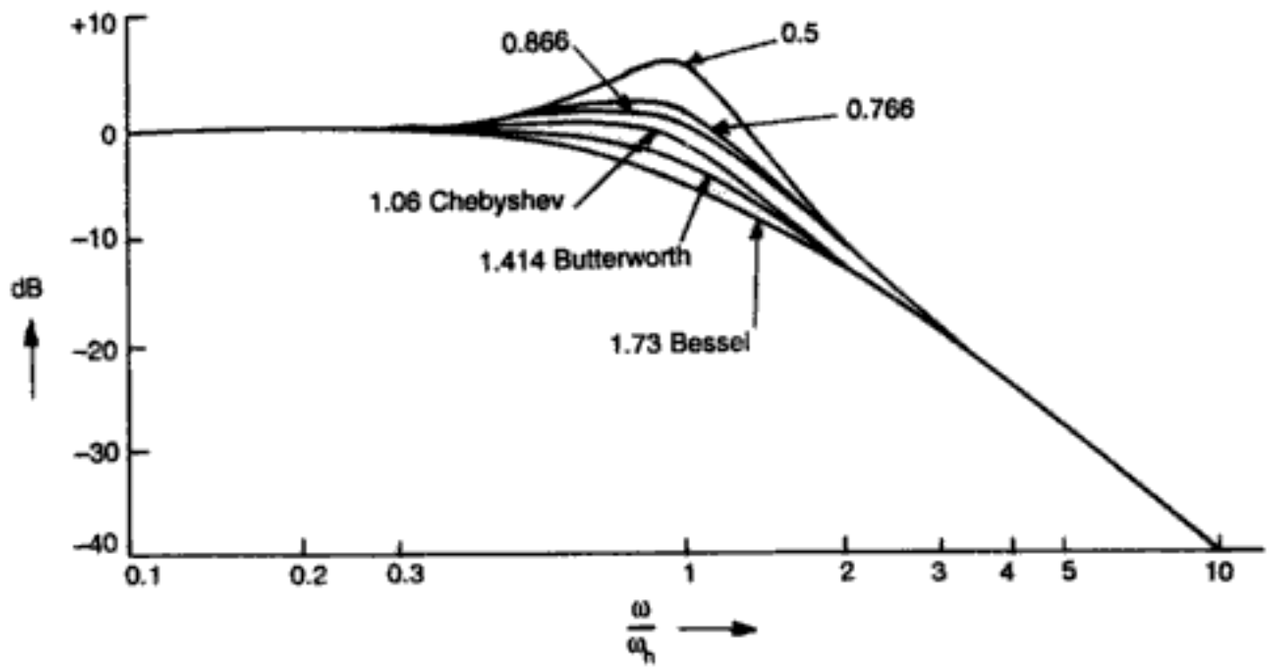

Fig. 7.5 Second order low-pass active filter response for different damping (unity gain $A_0 = 1$)

We shall discuss only Butterworth filter in this text as it has maximally flat response with damping coefficient $\alpha = 1.414$. From Eq. (7.24), with $\alpha = 1.414$, we get

$$20 \log |H(j\omega)| = 20 \log \left| \frac{V_o}{V_i} \right| = 20 \log \frac{A_0}{\sqrt{1 + \left(\frac{\omega}{\omega_h} \right)^4}} \tag{7.25}$$

Hence for n-th order generalized low-pass Butterworth filter, the normalized transfer function for maximally flat filter can be written as

$$\left| \frac{H(j\omega)}{A_0} \right| = \frac{1}{\sqrt{1 + \left(\frac{\omega}{\omega_h} \right)^{2n}}} \tag{7.26}$$

7.2.3 Higher Order Low-Pass Filter

A second order filter can provide – 40 dB/decade roll-off rate in the stop band. To match with ideal characteristics, the roll-off rate should be increased by increasing the order of the filter. Each increase in order will produce – 20 dB/decade additional increase in roll-off rate,

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$$v_A Y_2 = -v_o Y_5$$

$$v_A = -v_o (Y_5/Y_2) \tag{7.33}$$

Putting v_A in Eq. (7.32), we get

$$v_i Y_1 + v_o Y_3 = -\frac{v_o Y_5 (Y_1 + Y_2 + Y_3 + Y_4)}{Y_2}$$

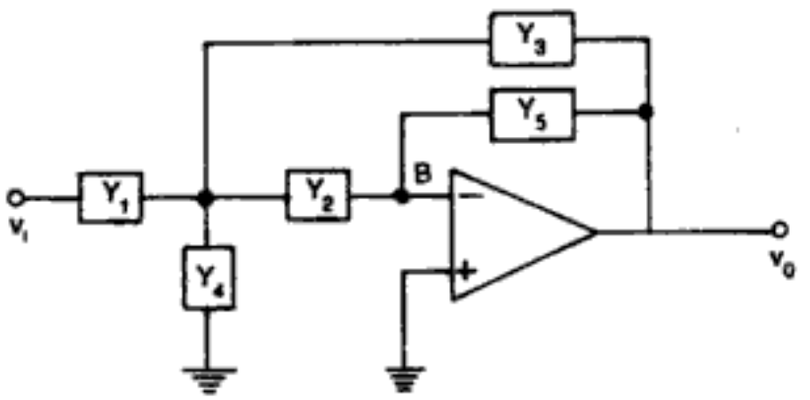

Fig. 7.9 (a) Band-pass configuration

or,
$$v_i Y_1 = v_o \left[-\frac{Y_2 Y_3 + Y_1 Y_5 + Y_2 Y_5 + Y_3 Y_5 + Y_4 Y_5}{Y_2} \right]$$

Hence

$$\frac{v_o}{v_i} = -\frac{Y_1 Y_2}{Y_2 Y_3 + Y_1 Y_5 + Y_2 Y_5 + Y_3 Y_5 + Y_4 Y_5} \tag{7.34}$$

For this circuit to be band pass filter, put $Y_1 = G_1$, $Y_2 = sC_2$, $Y_3 = sC_3$, $Y_4 = G_4$ and $Y_5 = G_5$ as in Fig. 7.9 (b). Then the transfer function becomes,

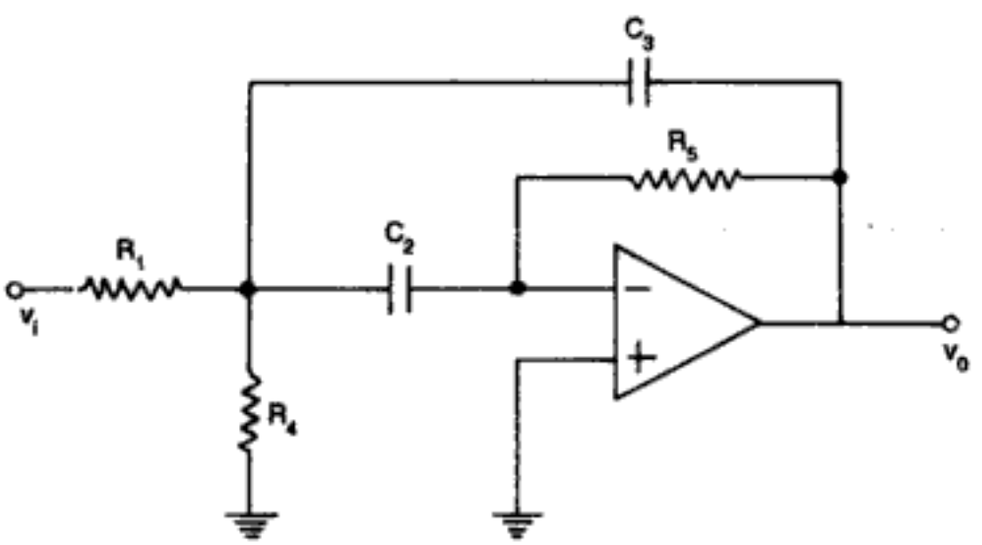

Fig. 7.9 (b) Second order band-pass filter

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{-sG_1C_2}{s^2C_2C_3 + s(C_2 + C_3)G_5 + G_5(G_1 + G_4)}$$

or,
$$H(s) = \frac{-G_1}{sC_3 + G_5(C_2 + C_3)/C_2 + (G_1 + G_4)G_5/sC_2} \tag{7.35}$$

The transfer function of Eq. (7.35) is equivalent to the gain expression of a parallel RLC circuit of Fig. 7.10(a) driven by a current source $G'v_i$ and with band pass characteristics as shown in Fig. 7.10 (b). The gain expression is,

$$\frac{V_o(s)}{V_i(s)} = -\frac{G'}{Y} = \frac{-G'}{sC + G + 1/sL} \tag{7.36}$$

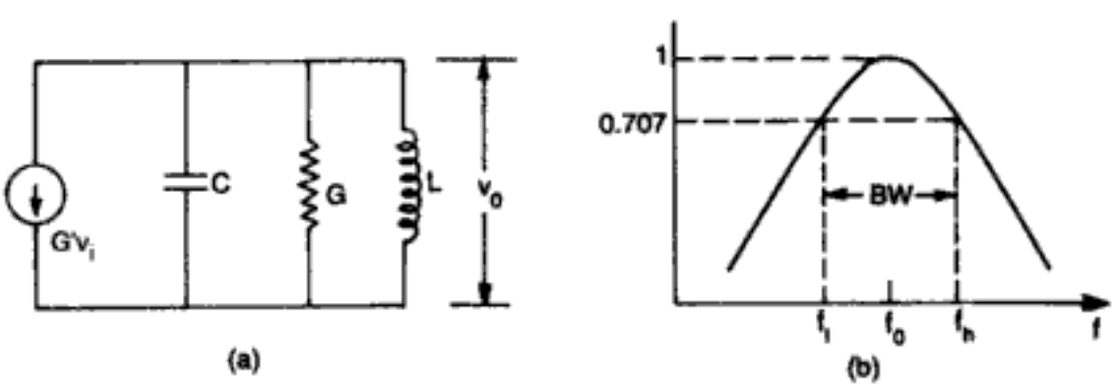

Fig. 7.10 (a) A parallel RLC circuit (b) Band-pass characteristics

Comparing the gain expression of Eq. (7.35) and Eq. (7.36), we get,

$$G' = G_1 \tag{7.37}$$

$$L = \frac{C_2}{G_5(G_1 + G_4)} \tag{7.38}$$

$$G = \frac{G_5(C_2 + C_3)}{C_2} \tag{7.39}$$

and
$$C = C_3 \tag{7.40}$$

At resonance, the circuit of Fig. 7.10(a) has unity power factor, i.e. imaginary part is zero which gives the resonant frequency ω_o as,

$$\omega_o^2 = \frac{1}{LC} = G_5\frac{(G_1 + G_4)}{C_2C_3} \tag{7.41}$$

The gain at resonance is,

$$\left.\frac{v_o}{v_i}\right|_{\omega = \omega_o} = -\frac{G'}{G} = -\frac{G_1}{G} = -\frac{(G_1/G_5)C_2}{C_2 + C_3}$$

$$= -\frac{(R_5/R_1)C_2}{C_2 + C_3} \tag{7.42}$$

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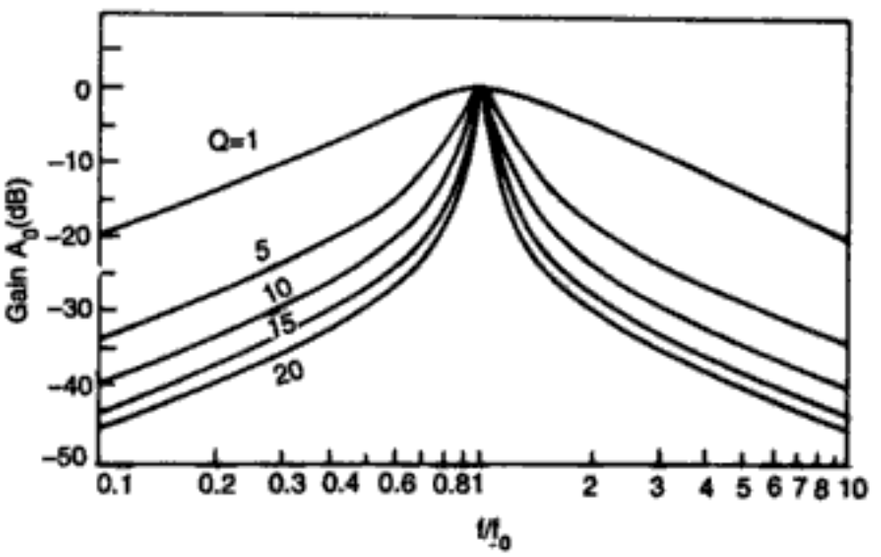


Fig. 7.11 Single op-amp band-pass filter response

It is obvious from Eq. (7.25) that for $\omega << \omega_0$ and $\omega >> \omega_0$ the gain is zero and for $\omega = \omega_0$ the gain is A_0. It may be noted that A_0 is negative.

Wide Band-Pass Filter

A wide band-pass filter can be formed by cascading a HPF and LPF section. If the HPF and LPF are of the first order, then the band-pass filter (BPF) will have a roll-off rate of – 20 dB/decade.

For the high pass section of Fig. 7.12 the magnitude of gain is

$$|H_{HP}| = \left| \left(1 + \frac{R_f}{R_i}\right) \frac{j\,2\pi f R_2 C_2}{1 + j\,2\pi f R_2 C_2} \right|$$

$$= \left| A_{01} \frac{j(f/f_\ell)}{1 + j(f/f_\ell)} \right|$$

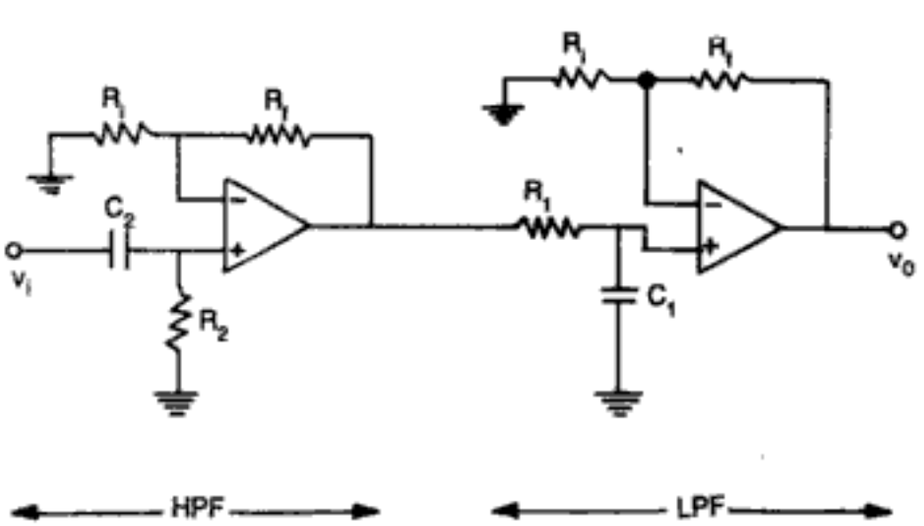


Fig. 7.12 First order band-pas filter

$$= \frac{A_{o1}\,(f/f_\ell)}{\sqrt{1+(f/f_\ell)^2}} \tag{7.50}$$

where $$f_\ell = \frac{1}{2\pi R_2 C_2} \tag{7.51}$$

Similarly, for the low-pass section of Fig. 7.12, the magnitude of gain is

$$|H_{LP}| = \frac{A_{o2}}{\sqrt{1+(f/f_h)^2}} \tag{7.52}$$

where $$f_h = \frac{1}{2\pi R_1 C_1} \tag{7.53}$$

The voltage gain magnitude of the wide band pass filter is the product of that of LPF and HPF. One can calculate the frequency response from the equation

$$\left|\frac{v_o}{v_i}\right| = \left|\frac{A_o\,(f/f_1)}{\sqrt{\left[1+(f/f_\ell)^2\right]\left[1+(f/f_h)^2\right]}}\right| \tag{7.54}$$

where the total pass band gain $A_o = A_{o1} \times A_{o2}$

In a similar fashion, to obtain BPF of – 40 dB/decade fall-off rate, second order HPF and LPF sections are to be cascaded.

Example 7.6

Design a wide-band pass filter having $f_\ell = 400$ Hz, $f_h = 2$ kHz and pass band gain of 4. Find the value of Q of the filter.

Solution

The pass band gain is 4. The LPF and HPF sections each of Fig. 7.12 may be designed to give gain of 2, that is, $A_o = 1 + R_f/R_i = 2$. So R_f and R_i should be equal. Let $R_f = R_i = 10$ kΩ for each of LPF and HPF sections.

For LPF, $f_h = 2$ kHz $= 1/2\,\pi\, R_1 C_1$. Let $C_1 = 0.01$ μF gives $R_1 = 7.9$ kΩ. For HPF, $f_\ell = 400$ Hz $= 1/2\,\pi\, R_2 C_2$. Let $C_2 = 0.01$ μF gives $R_2 = 39.8$ kΩ.

Again $f_o = \sqrt{f_h f_\ell} = \sqrt{2000 \times 400} = 894.4$

$$Q = f_o/BW = f_o/(f_h - f_\ell) = 894.4/(2000 - 400) = 0.56$$

Obviously, for wide band pass filter, Q is very low, i.e., $Q < 10$.

7.2.6 Band Reject Filter

A band reject filter (also called a band stop or band elimination) can be either (i) Narrow band reject or (ii) Wide band reject filter. The

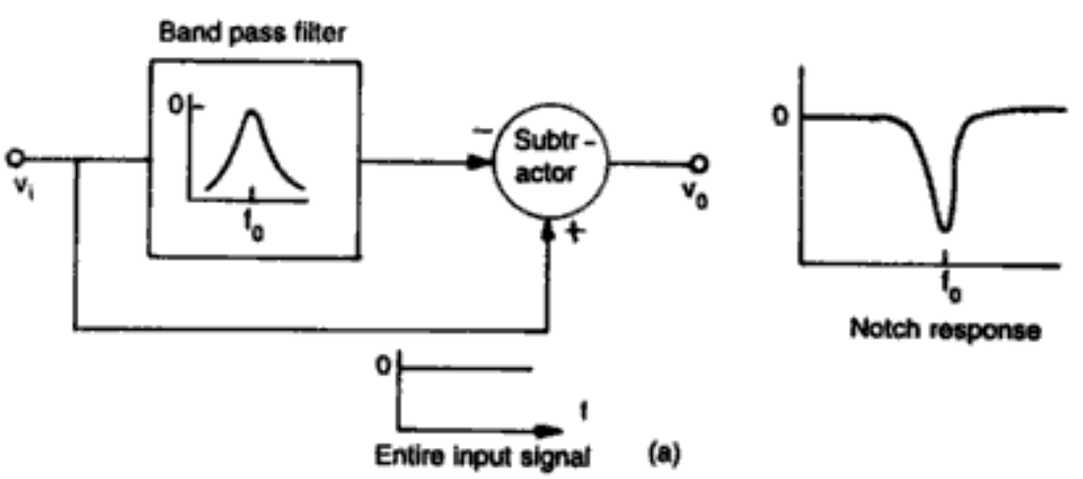
narrow band reject filter is commonly called a notch filter and is useful for the rejection of a single frequency, such as 50 Hz power line frequency hum.

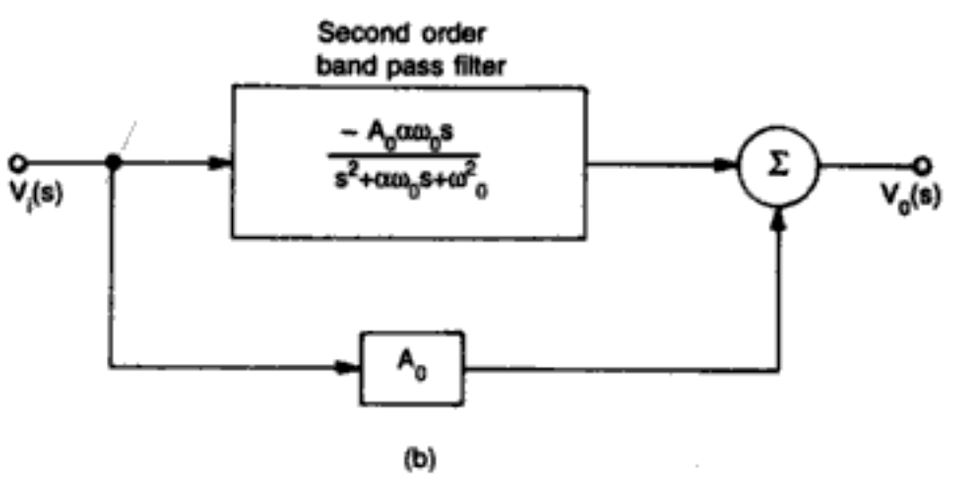
There are several ways to make notch filters. One simple technique is to subtract the band pass filter output from its input. This principle is illustrated in Fig. 7.13 (a).

The band pass filter discussed earlier has an inverted output as the gain or transfer Eq. (7.35) is negative. Therefore, while implementing Fig. 7.13 (a), we must use a summer instead of a subtractor. Also, the band pass filter has a gain of A_0, so that output at the centre frequency will be $-A_0 \times v_i$. To completely subtract this output, the input of the summer must be precisely $A_0 v_i$. Thus, a gain of A_0 must be added between the input signal and the summer as shown in Fig. 7.13(b). The output, of the circuit in the s domain is,

$$V_0(s) = A_0 V_i(s) + \left(\frac{-A_0 \alpha \omega_0 s \, V_i(s)}{s^2 + \alpha \omega_0 s + \omega_0^2} \right) \tag{7.55}$$

$$\frac{V_0(s)}{V_i(s)} = A_0 - \frac{A_0 \alpha \omega_0 s}{s^2 + \alpha \omega_0 s + \omega_0^2}$$





(b)

Fig. 7.13 (a) Notch filter block diagram (b) Practical notch filter block diagram

$$= A_0\left(1 - \frac{\alpha\omega_0 s}{s^2 + \alpha\omega_0 s + \omega_0^2}\right)$$

$$= \frac{A_0(s^2 + \omega_0^2)}{s^2 + \alpha\omega_0 s + \omega_0^2} \tag{7.56}$$

This is the transfer function for a second order notch filter and the circuit schematic is shown in Fig. 7.14. It is evident from Eq. (7.56), that for $\omega << \omega_0$ and for $\omega >> \omega_0$ the pass band gain is $|A_0|$ and at frequency $\omega = \omega_0$ the gain is zero.

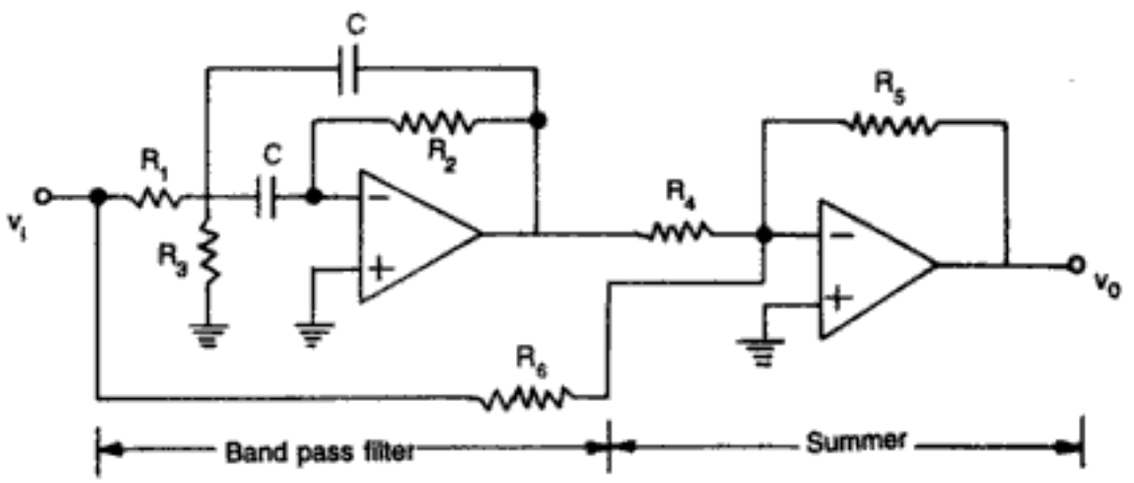


Fig. 7.14 Notch filter schematic

Another commonly used notch filter is the twin-T network as shown in Fig. 7.15(a). We will determine the notch frequency, Q factor and bandwidth for this configuration.

Node voltage equations in s-domain (by KCL) for the active filter circuit of Fig. 7.15(a) can be written as,

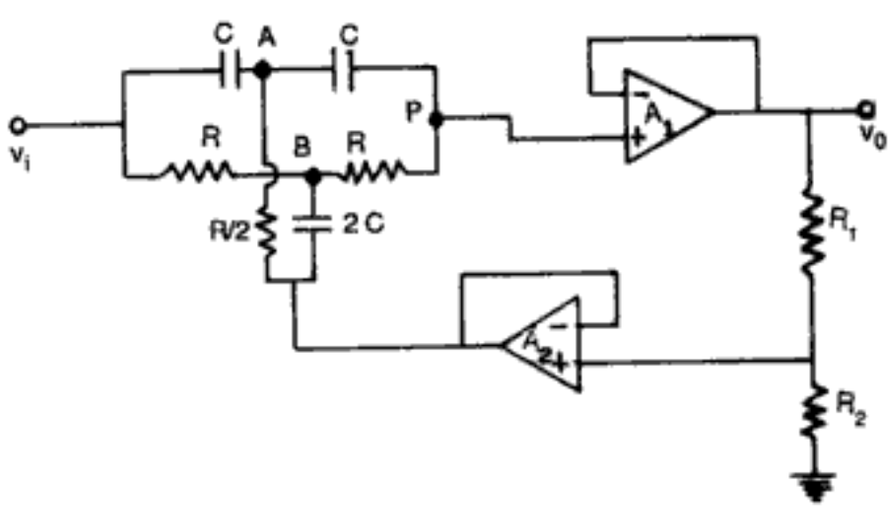


Fig. 7.15 (a) Twin-T notch filter

At node A: $(V_i - V_A)\,sC + (V_o - V_A)\,sC + (KV_o - V_A)2G = 0$

or, $$sC\,V_i + (sC + 2KG)\,V_o = 2\,(sC + G)\,V_A \qquad (7.57)$$

where V_A is the Laplace transform of the voltage at node A. Similarly V_i and V_o are transformed input and output. The s in the parenthesis has been dropped in the Laplace transform for simplicity.

At node B: $(V_i - V_B)G + (V_o - V_B)G + 2\,(KV_o - V_B)sC = 0$

or, $$GV_i + (G + 2\,KsC)\,V_o = 2(G + sC)V_B \qquad (7.58)$$

where V_B is the Laplace transform of the voltage at node B.

At node P: $(V_A - V_o)\,sC + (V_B - V_o)G = 0$

or, $$sC\,V_A + GV_B = (G + sC)V_o \qquad (7.59)$$

where, $K = R_2/(R_1 + R_2)$ and $G = 1/R$

From these node voltage equations, the transfer function can be written as,

$$H(s) = \frac{V_o}{V_i} = \frac{G^2 + s^2 C^2}{G^2 + s^2C^2 + 4(1 - K)s\,CG}$$

$$= \frac{s^2 + (G/C)^2}{s^2 + (G/C)^2 + 4(1 - K)s\,(G/C)} \qquad (7.60)$$

In the steady state (i.e. $s = j\omega$),

$$H(j\omega) = \frac{\omega^2 - \omega_o^2}{\omega^2 - \omega_o^2 - j\,4\,(1 - K)\,\omega\,\omega_o} \qquad (7.61)$$

where, $\omega_o = G/C = 1/RC$

i.e., $$f_o = \frac{1}{2\pi\,RC} \qquad (7.62)$$

From Eq. (7.61), $H(j\omega)$ becomes zero for $\omega = \omega_o$ and approaches unity as $\omega << \omega_o$ and for $\omega >> \omega_o$. In practice the high frequency response will be limited by the high frequency response of the op-amp. At 3-dB points, $|H| = 1/\sqrt{2}$

i.e. $$\omega^2 - \omega_o^2 = \pm\, 4(1 - K)\,\omega\,\omega_o$$

or $$(\omega/\omega_o)^2 \pm 4(1 - K)\,(\omega/\omega_o) - 1 = 0 \qquad (7.63)$$

Solving the quadratic equation, we get the upper and lower half power frequencies as,

$$f_h = f_0\left[\sqrt{1 + 4(1 - K)^2} + 2\,(1 - K)\right] \qquad (7.64)$$

and $$f_l = f_o\left[\sqrt{1 + 4\,(1 - K)^2} - 2(1 - K)\right] \qquad (7.65)$$

The 3-dB bandwidth,

$$BW = f_h - f_\ell = 4(1 - K)f_o \tag{7.66}$$

$$Q = \frac{f_o}{BW} = \frac{1}{4(1-K)} \tag{7.67}$$

As K approaches unity, Q factor becomes very large and BW approaches 0. In fact, mismatches between resistors and capacitors limit the Q-factor and BW to practically realizable value. It is advisable to use the components of 0.1 percent tolerance resistors and 1 percent tolerance capacitors for very high value of Q-factor. The frequency response is shown in Fig. 7.15(b).

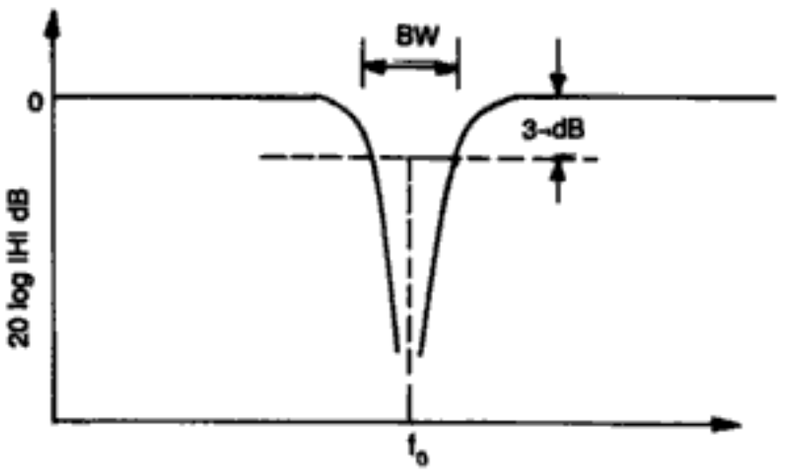


Fig. 7.15 (b) Frequency response of notch filter

Example 7.7

Design a 50 Hz active notch filter.

Solution

Given f_o = 50 Hz. Let C = 0.1 μF then from Eq. (7.62), we get R = $1/2\,\pi f_o C$ = 1/2 (3.14) (50) (10^{-7}) = 31.8 kΩ.

For $R/2$,. take two resistors of 31.8 kΩ in parallel and for $2C$, take two 0.1 μF capacitors in parallel to make the twin-T notch filter as shown in Fig. 7.15(a) where resistors R_1 and R_2 are for adjustment of gain.

Wide Band-Reject Filter

A wide band-reject filter ($Q < 10$) can be made using a LPF, HPF and a summer. It is of course necessary that (i) the lower cut off-frequency f_ℓ of the HPF should be much greater than the upper cut-off frequency f_h of the LPF and (ii) the pass band gain of LPF and HPF should be same.

Example 7.8

Design a wide band reject filter having f_h = 400 Hz and f_ℓ = 2 kHz having pass band gain as 2.

Solution

For HPF, $f_\ell = 2$ kHz $= 1/2\ \pi R_2 C_2$. Letting $C_2 = 0.1\ \mu$F gives $R_2 = 795\ \Omega$ ($\approx 800\ \Omega$). Again $A_o = A_{o2} = 2 = (1 + R_f/R_i)$ gives $R_f = R_i = 10$ kΩ (say). For LPF, $f_h = 400$ Hz $= 1/2\ \pi\ R_1 C_1$. Letting $C_1 = 0.1\ \mu$F gives $R_1 = 3978\ \Omega$ (choose 4 kΩ). Further $A_o = A_{o1} = 2 = (1 + R_f/R_i)$ gives $R_i = R_f = 10$ kΩ (say). The schematic arrangement and the frequency response is shown in Figs. 7.16 (a, b).

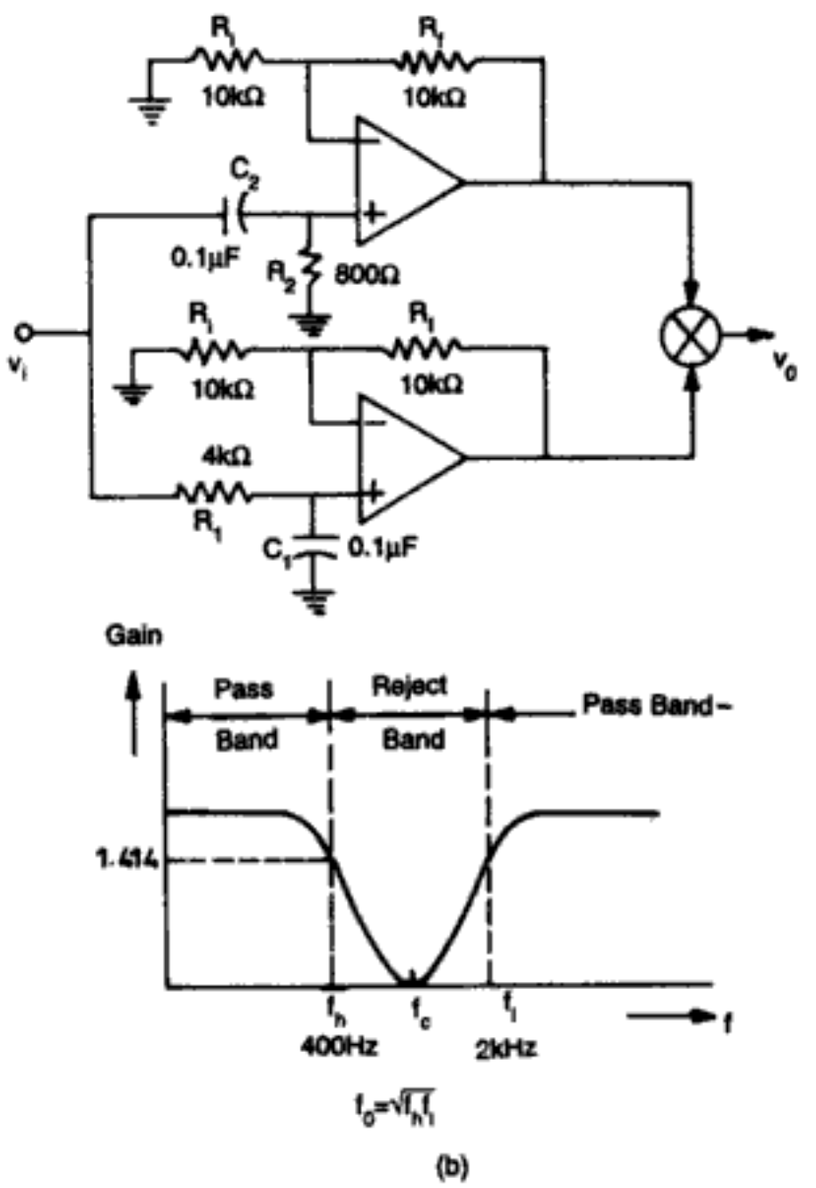


Fig. 7.16 (a) Wide band-reject filter (b) Frequency response

7.3 TRANSFORMATION

We shall now show that a high-pass, band-pass or band-reject filter can be obtained using an ideal low-pass transfer function by simple frequency transformation. For simplicity, let us normalize the frequency such that the cut-off frequency of the low pass function is unity. Let 'p' be the frequency domain of the low pass and 's' the frequency domain of interest.

Low-pass to High-pass Transformation

We get the high-pass characteristics by the following low-pass to high-pass transformation $p = 1/s$. For example, a third order Butterworth low-pass transfer function in p-domain given as

$$H(p) = \frac{A_o}{p^3 + 2p^2 + 2p + 1} \tag{7.68}$$

can be transformed to high-pass by the transformation $p = 1/s$ as

$$H(s) = \frac{A_o s^3}{s^3 + 2s^2 + 2s + 1} \tag{7.69}$$

The high-pass filter has the same pass band flatness as that of the Butterworth low-pass filter.

A low pass filter can be transformed to a high-pass filter simply by interchanging R and C components and vice versa. A simple $RC : CR$ transformation is shown in Fig. 7.4 and Fig. 7.8. This is to note that the 3-dB (cut-off) frequency is the same for both the original low-pass and the transformed high-pass filter i.e., $f_{3\text{-dB}} = 1/2\ \pi\ RC$.

Low-pass to Band-pass Transformation

Consider a first order Butterworth low-pass transfer function in p-domain as

$$H(p) = \frac{A_o}{p + 1} \tag{7.70}$$

Let the transformation

$$p = \frac{s^2 + \omega_o^2}{(\omega_h - \omega_\ell)s} \tag{7.71}$$

In order to normalize, put

$$s_n = s/\omega_o \tag{7.72}$$

and quality factor, $$Q = \frac{\omega_o}{\omega_h - \omega_\ell}$$

Then Eq. (7.71) can be rewritten as

$$p = \frac{Q(s_n^2 + 1)}{s_n} \tag{7.73}$$

Substituting the transformation from Eq. (7.73) to Eq. (7.70), we get

$$H(s_n) = \frac{(A_o/Q)s_n}{s_n^2 + (1/Q)s_n + 1} \tag{7.74}$$

This is identical with Eq. (7.48) of band pass filter. The quality factor Q is an important parameter. If Q is very high, i.e $Q >> 1$, the filter is called narrow band filter (i.e., $\omega_o >> (\omega_h - \omega_\ell)$) and the response is symmetric about the central frequency ω_o.

Low-pass to Band-reject Transformation

The transformation is given by

$$p = \frac{(\omega_h - \omega_\ell)s}{s^2 + \omega_o^2} = \frac{s_n}{Q(s_n^2 + 1)} \tag{7.75}$$

where $s_n = s/\omega_o$

The band-reject transfer function corresponding to first order low-pass of Eq. (7.70) and is given by

$$H(S_n) = \frac{A_o(s_n^2 + 1)}{s_n^2 + (1/Q)s_n + 1} \tag{7.76}$$

Note at $s_n = j1$, $|H(j1)| = 0$. Such filters are called 'notch filter' with normalized null frequency as $\omega_o = 1$.

7.4 STATE VARIABLE FILTER

The state variable configuration uses two op-amp integrators and one op-amp adder to provide simultaneous second order low-pass, band-pass and high-pass filter responses. The circuit can be viewed as analog computer simulation of biquadratic transfer function. Although, in general, all component values are different, imposing equal value simplifies algebra without diminishing versatality.

A simple state variable configuration has been shown in Fig. 7.17 (a). It uses two op-amp integrators and one op-amp summer. The outputs v_{HP}, v_{BP}, v_{LP} of high-pass, band-pass and low-pass filters are obtained at the output of op-amp A_1, A_2 and A_3 respectively. For simplification, it is assumed that V is the Laplace transform of the corresponding v in time domain.

The op-amp A_2 works as an inverting integrator, so the Laplace transformed output V_{BP} is given by

$$V_{BP} = -\frac{1}{RCs} V_{HP} \tag{7.77}$$

If $R = 1$ MΩ and $C = 1$ μF, so that $RC = 1$, we get,

$$V_{BP} = -\frac{1}{s} V_{HP} \tag{7.78}$$

Also for the inverting integrator A_3, we may write

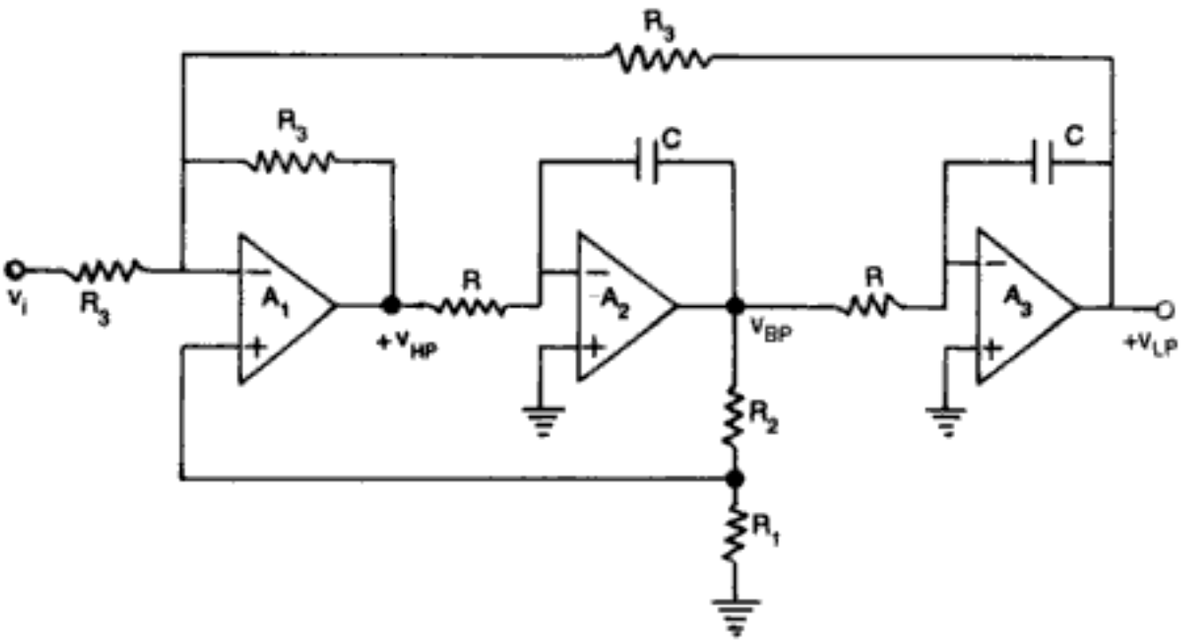


Fig. 7.17 (a) State variable filter

$$V_{LP} = \frac{1}{s} V_{BP}$$

$$= \frac{1}{s^2} V_{HP} \tag{7.79}$$

Op-amp A_1 is a three input summer. The output V_{HP} can be written using superposition theorem. That is,

$$V_{HP} = -\left(\frac{R_3}{R_3}\right)V_i - \left(\frac{R_3}{R_3}\right)V_{LP} + \left(1 + \frac{R_3}{R_3 \,||\, R_3}\right)\left(\frac{R_1}{R_1 + R_2}\right)V_{BP}$$

$$= -V_i - V_{LP} + 3\left(\frac{R_1}{R_1 + R_2}\right)V_{BP}$$

Put $$\alpha = 3\left(\frac{R_1}{R_1 + R_2}\right)$$

Then $$V_{HP} = -V_i - V_{LP} + \alpha V_{BP} \tag{7.80}$$

Eliminating V_{BP} and V_{LP} using Eqs. (7.78) and (7.79), we get

$$V_{HP} = -V_i - \frac{V_{HP}}{s^2} - \frac{\alpha}{s} V_{HP}$$

$$V_{HP}\left(1 + \frac{\alpha}{s} + \frac{1}{s^2}\right) = -V_i$$

So, the high pass transfer function H_{HP} is

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The circuit of Fig. 7.17(a) can be modified to that of Fig. 7.17(b) where a fourth op-amp has been used to get a notch filter response. The op-amp A_4 provides the notch filter response by combining the low-pass and high-pass output. The notch filter output V_N is written as

$$V_N = -\left(\frac{R_4}{R_4}\right)V_{HP} - \left(\frac{R_4}{R_4}\right)V_{LP}$$

$$= -V_{HP} - V_{LP} \tag{7.89}$$

Putting the values of V_{HP} and V_{LP}, the transfer function of notch filter is obtained as

$$H_N = \frac{V_N}{V_i} = \frac{s^2 + 1}{s^2 + \alpha s + 1} \tag{7.90}$$

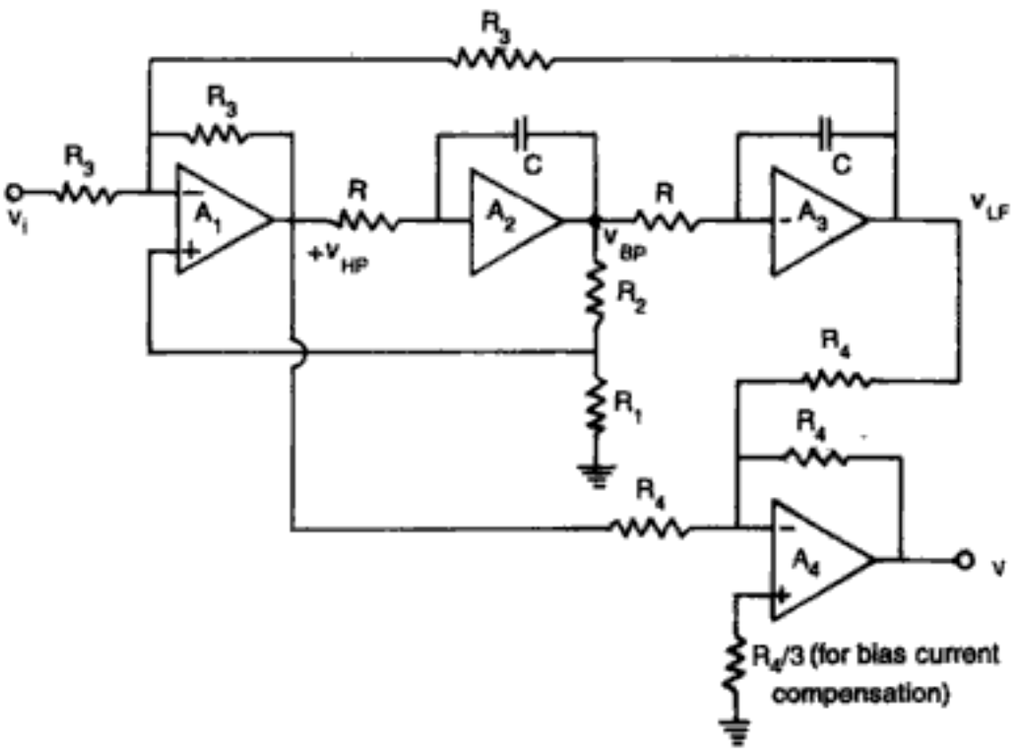

Fig. 7.17 (b) Four op-amp state variable filter with notch response

Thus it is possible to obtain LP, BP, HP and notch filter outputs from a state variable filter and therefore these are also known as universal filters. Quad op-amps such as LF347, TL074 and TLC274, FET input device are especially suited for these applications. With the advancement of IC technology, universal filters are available in single IC chip form. Datel's FLT-U2 and AF100 of National Semiconductor are the typical examples of IC universal filters.

State Variable Formulation

It may be noted that this filter is called state variable filter because the analog simulation can be made after the state variable formulation of the proper transfer function.

The band-pass filter transfer function of Eq. (7.48) can be rewritten for $A_o = -1$, $\omega_o = 1$, $\alpha = 1$ and assuming a dummy variable $X_1 = \mathcal{L}x_1(t)$, as

$$\frac{V_{BP}}{X_1} \cdot \frac{X_1}{V_i} = s\frac{1}{s^2 + s + 1} \tag{7.91}$$

Let $$\frac{X_1}{V_i} = \frac{1}{s^2 + s + 1} \tag{7.92}$$

which can written in time domain as

$$\ddot{x}_1 + \dot{x}_1 + x_1 = v_i$$

Let $$\dot{x}_1 = x_2$$

then $$\dot{x}_2 = -x_1 - x_2 + v_i$$

These can be written in matrix form as

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ -1 & -1 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \end{bmatrix} v_i \tag{7.93}$$

and $$\frac{V_{BP}}{X_1} = s \tag{7.94}$$

leads to the output in time domain as $v_{BP} = \dot{x}_1 = x_2$

or, $$v_{BP} = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} \tag{7.95}$$

Similarly the high-pass transfer function H_{HP} of Eq. (7.81) with $\alpha = 1$ can be rewritten assuming another dummy variable $Y = \mathcal{L}y(t)$ as

$$H_{HP} = \frac{V_{HP}}{V_i} = -1 + \frac{s+1}{s^2 + s + 1} = -1 + \frac{Y}{V_i} \tag{7.96}$$

where $$\frac{Y}{V_i} = \frac{Y}{X_1} \cdot \frac{X_1}{V_i} = (s+1) \cdot \frac{1}{s^2 + s + 1} \tag{7.97}$$

Let $$\frac{X_1}{V_i} = \frac{1}{s^2 + s + 1} \tag{7.98}$$

It leads to

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ -1 & -1 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \end{bmatrix} v_i \tag{7.99}$$

and $$\frac{Y}{X_1} = (s + 1) \tag{7.100}$$

leads to in time domain $y = \dot{x}_1 + x_1 = x_2 + x_1$

or,
$$y = \begin{bmatrix} 1 & 1 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} \tag{7.101}$$

Hence the output

$$V_{HP} = y - v_i = \begin{bmatrix} 1 & 1 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} - (1)\, v_i \tag{7.102}$$

The simulation of Eqs. (7.99) and (7.102) is shown in Fig. 7.18 having V_{HP} as output.

Similarly, the low-pass transfer function of Eq. (7.75) can be written in the same fashion as

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ -1 & -1 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \end{bmatrix} v_i \tag{7.103}$$

and output

$$V_{LP} = \begin{bmatrix} -1 & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}$$

The simulation is as shown in Fig. 7.18.

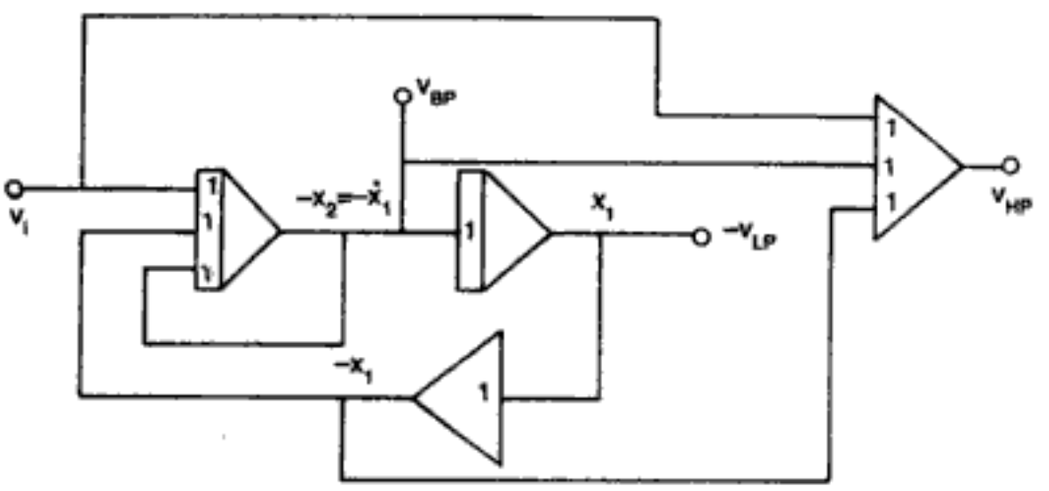

Fig. 7.18 Simulation of state variable filter

7.5 SWITCHED CAPACITOR FILTERS

Active *RC* filters using ICs have advantages of not using inductors and of offering easy implementation of various high performance low-pass, high-pass, band-pass and band-elimination filters. The resistor values needed for these filters are generally much too large for fabrication on a monolithic IC chip. Integrated (diffused) resistors have poor temperature and linearity characteristics. Large value resistors (≥ 10 kΩ) take up an excessive amount of chip area. This is the major reason that active filters have not previously been fully integrated in MOS technology. The switched capacitor filter offers an attractive alternative to the conventional *RC* active filter. A switched

capacitor filter shown in Fig. 7.19 is a three terminal element which consists of capacitors, periodic switches and operational amplifiers and whose open circuit voltage transfer function represents filtering characteristics. It is not possible to manufacture passive elements of an *RC* active filter with suitable values and quality in the same technology as the op-amps. For the range of frequencies within which the op-amp operates satisfactorily, it is not possible in MOS technology to implement *RC* products of sufficient magnitude and accuracy. On the other hand, in the case of switched capacitor filter, the *RC* products are set by capacitor ratios and the switch period. In MOS technology, the accuracy and the values of these quantities are suitable for the implementation of selective filters. The large resistor values required for active filter are easily simulated by the combination of small value capacitors (say 10 pF) and MOS switching transistors. The equivalent resistor value so obtained is high enough such that the filter capacitance value should be small enough to be easily incorporated on a monolithic IC chip. In this way, the complete active filter circuit can be obtained on a monolithic IC chip.

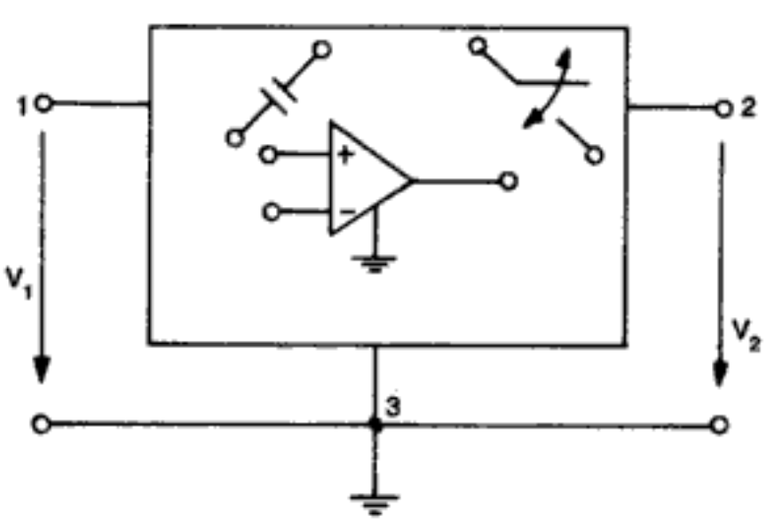

Fig. 7.19 Switched capacitor filter schematic

Thus, even a filter of relatively high order becomes an integrated circuit of a very small size, with a low power consumption and reliability and price which are potentially more favourable than those of passive *LC* and *RC* active filters. Further, the filters may be combined on the same substrate with other logic circuits, offering interesting prospects for the implementation of a complete system of analog and discrete signal processing.

7.5.1 Realization of Resistors by Single Capacitor

Consider the switched capacitor network in Fig. 7.20(a). The switch S is initially in position 'a', the capacitor C is charged to voltage V_1. The switch is then thrown to position 'b'. The capacitor C is discharged to the voltage V_2. Assume $V_2 < V_1$. The amount of charge that flows through the capacitor C is thus,

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is $Q = CV_1$. When ϕ goes low and $\bar{\phi}$ goes high, the capacitor C charges up in the opposite direction to V_2. The charge transfer from the output of the circuit back into C is $Q = C_1 (V_2 - V_1)$. The time average of this charge is the current flow i and is given by,

$$i = -\frac{Q}{T_{ck}} = -f_{ck} C (V_2 - V_1) = \frac{V_1 - V_2}{R} \tag{7.116}$$

where,

$$R = \frac{1}{f_{ck} C} \tag{7.117}$$

The two circuits just described use a series switched capacitor.

The circuit of Fig. 7.23(c) uses a shunt switched capacitor. The circuit is a modification of Fig. 7.21(b) with $V_2 = 0$. For this circuit,

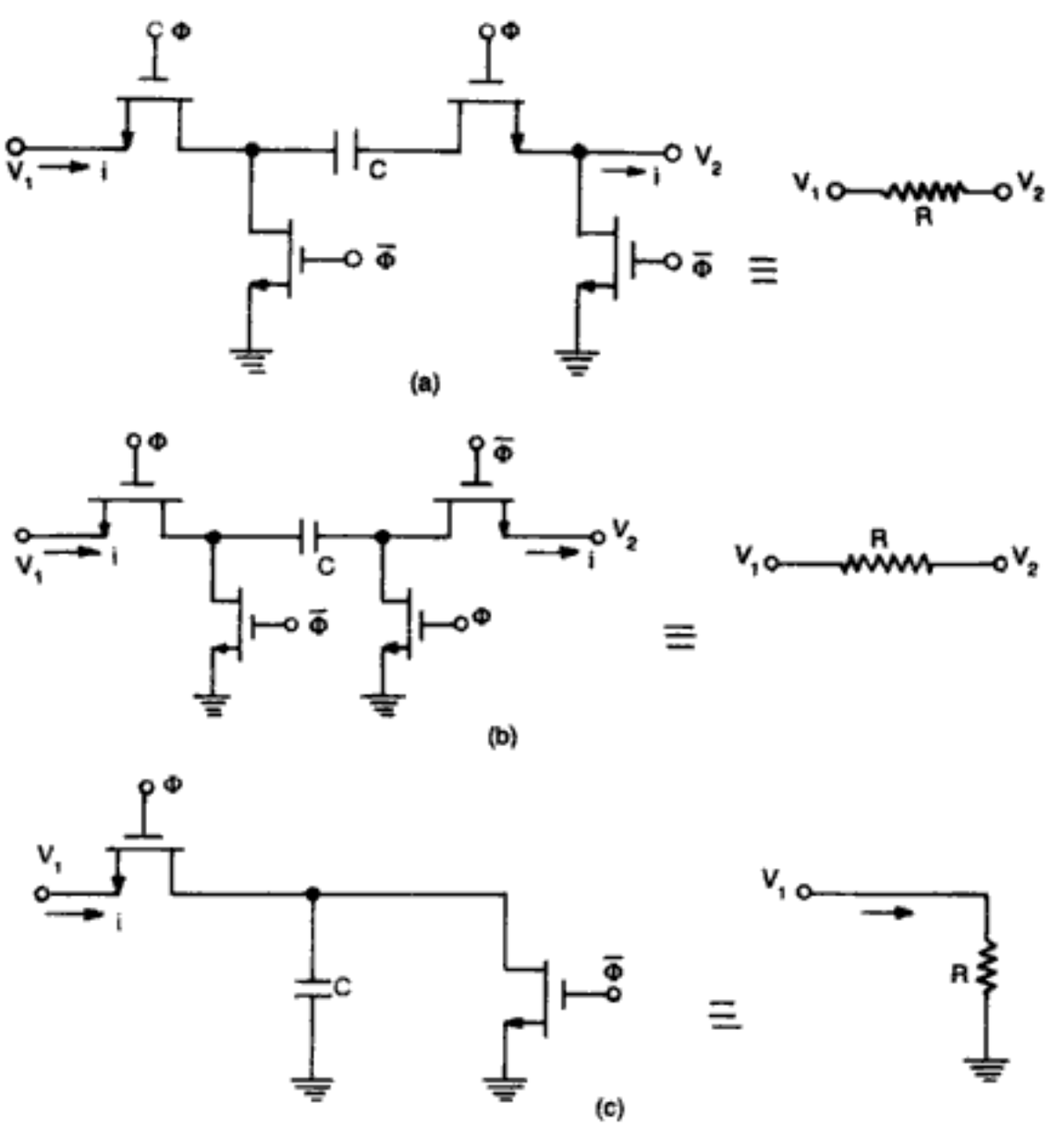

Fig. 7.23 (a) Noninverting series switched capacitor circuit (b) Inverting series switched capacitor circuit (c) Shunt capacitor circuit

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capacitors C_1 and C_2 and its MOS version is in Fig. 7.25(c).

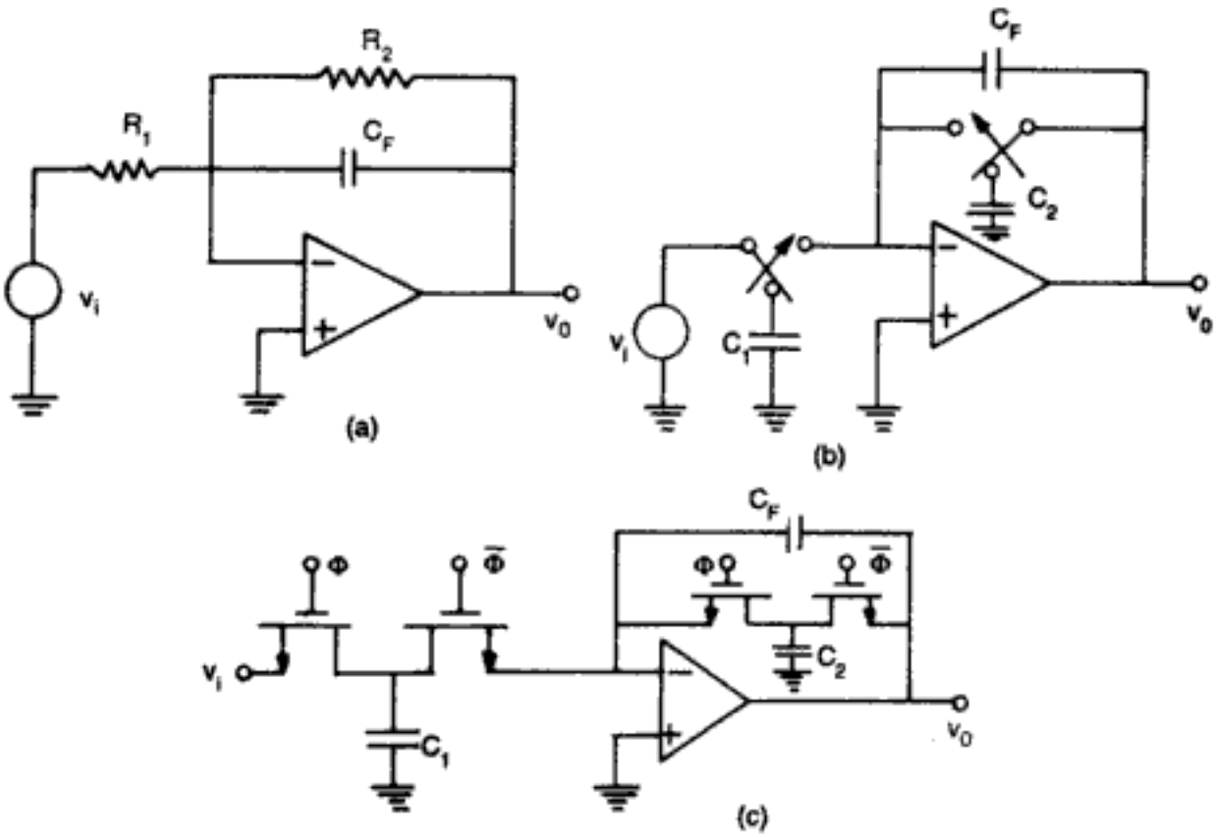

Fig. 7.25 (a) Lossy integrator (b) Switched capacitor version (c) CMOS version

$$R_2 = \frac{1}{f_{ck} C_2} \tag{7.125}$$

$$R_1 = \frac{1}{f_{ck} C_1} \tag{7.126}$$

So,
$$\frac{R_2}{R_1} = \frac{C_1}{C_2} \tag{7.127}$$

and
$$f_h = \frac{1}{2\pi C_F R_2} = \frac{1}{2\pi} \frac{C_2}{C_F} f_{ck} \tag{7.128}$$

Thus the transfer function can be rewritten as,

$$H(j\omega) = -\frac{C_1}{C_2}\left[\frac{1}{1 + j(f/f_h)}\right] \tag{7.129}$$

It is evident from the transfer function expression that the LP filter characteristics is a function of MOS capacitance ratio and the clock frequency.

Thus with the control of the clock frequency, the filter characteristic can be varied electronically. This also shows that SC filters are

inherently a programmable type. In a similar fashion, other types of active filters without resistance can also be achieved.

Switched capacitor filters are available in IC version from several manufacturers. The MF6-100 (National Semiconductor) is a 6th order low-pass Butterworth filter fabricated by CMOS technology. A monolithic switched capacitor universal filter (National Semiconductor MF 10) can be designed to provide LP, HP, BP and notch characteristics.

Summary

1. An electric filter is a frequency selective circuit that allows a specified band of frequencies and attenuates the frequencies outside this band.
2. Filters are classified in a number of ways: analog or digital, passive or active, audio or radio frequency.
3. Passive filters use inductors. At audio frequencies, inductors are bulky, expensive and have poor electrical characteristics. Active filters use op-amps.
4. The commonly used filters are: Low pass (LP), High pass (HP), Band pass (BP) and Band reject (BR).
5. Filter behaviour is usually described by frequency response plot. The gain magnitude is usually expressed in dB. Critical frequency occurs when the gain drops by 3 dB below the pass band gain. The critical frequency is the dividing line between the stop band and the pass band.
6. Low pass filters pass low frequencies and stop high frequencies. High pass filters do just the opposite. Critical frequency occurs where the gain has dropped by 3 dB below the pass band. A band pass filter has a pass band between the two cut-off frequencies f_h and f_l and all signals outside this pass band are stopped. The band reject filter, also called a notch filter, performs exactly opposite to the band pass.
7. A first order low pass filter has a –20 dB decade roll-off rate. The roll-off rate increases with the order of the filter. An n-th order filter has a roll-off rate of $-20\ n$ dB/decade.
8. Higher order filters are made by cascading first and second order filters.
9. A low pass filter can be converted into a high pass filter or vice versa, simply by interchanging resistors and capacitors.
10. The important transfer functions derived are:

    First order low pass: $\dfrac{A_o\ \omega_h}{s + \omega_h}$

    General Second order filter:

$$\frac{A_o Y_1 Y_2}{Y_1 Y_2 + Y_4(Y_1 + Y_2 + Y_3) + Y_2 Y_3(1 - A_o)}$$

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7.16. What is a switched capacitor? Discuss its importance.
7.17. Discuss various types of switched capacitors.
7.18. Give the circuit of a switched capacitor low pass filter.

PROBLEMS

7.1. Design a first order low pass filter for a high cut-off frequency of 2 kHz and pass band gain of 2.
7.2. Determine the order of the Butterworth low pass filter so that at $\omega = 1.5\ \omega_{3\text{-dB}}$, the magnitude response is down by at least 30 dB.
7.3. In the circuit of Fig. 7.4, $R = 3.3\ \text{k}\Omega$, $C = 0.047\ \mu\text{F}$, $R_i = 27\ \text{k}\Omega$ and $R_f = 20\ \text{k}\Omega$. Calculate the high frequency cut-off f_h and pass band gain A_o.
7.4. A low-pass Butterworth filter is to be designed to have a 3-dB bandwidth of 200 Hz and an attenuation of 50 dB at 400 Hz. Find the order of the filter.
7.5. Design a fourth order Butterworth low pass filter whose bandwidth is 1 kHz. Select all capacitors equal to 1000 nF.
7.6. Design a HPF at a cut-off frequency of 1 kHz and a pass band gain of 2.
7.7. Design a band pas filter so that $f_o = 2$ kHz, $Q = 20$ and $A_o = 10$. Choose $C = 1\ \mu\text{F}$.
7.8. Design a notch filter for $f_o = 8$ kHz and $Q = 10$. Choose $C = 500$ pF.
7.9. An ideal LPF having $f_h = 5$ kHz is cascaded with HPF having $f_\ell = 4.8$ kHz. Sketch the frequency response of the cascaded filter.
7.10. Find the transfer function of the circuits shown in Fig. P.7.10.

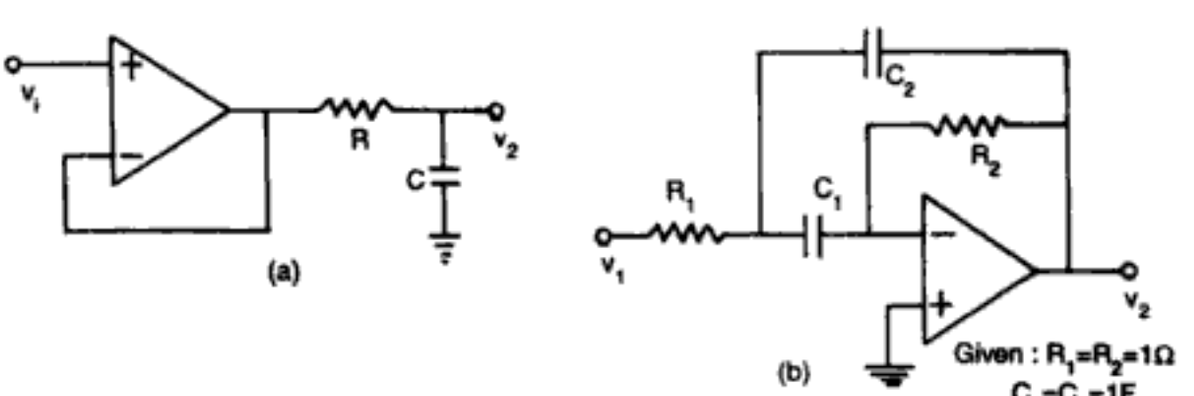

Fig. P. 7.10

7.11. Realize the circuit shown in Fig. P.7.10 using switched capacitors.
7.12. Find suitable component values of a lossy integrator of Fig. 7.25 (a), using switched capacitors. Given $f_h = 1$ kHz and low frequency gain of 10.

Experiment 7.1

To construct and plot the frequency response of a second order low pass, high pass filter. To measure the cut-off frequency in each case and verify with theoretical values.

Procedure

Low Pass Filter

1. Connect the circuit as shown in Fig. E.7.1 using discrete components. The values of the components have been taken from the Example 7.1. Please note that the Fig. E.7.1 has been numbered for the computer program 7.1.
2. Given an input signal v_i of 1 V peak to peak and measure the output voltage for different input frequencies (e.g. 100 Hz, 200 Hz, 500 Hz, 1 kHz, 1.5 kHz, 2.0 kHz, 5 kHz, 10 kHz).
3. Plot the frequency response 20 log (v_0/v_i) versus input signal frequency and find the 3 dB frequency from here.

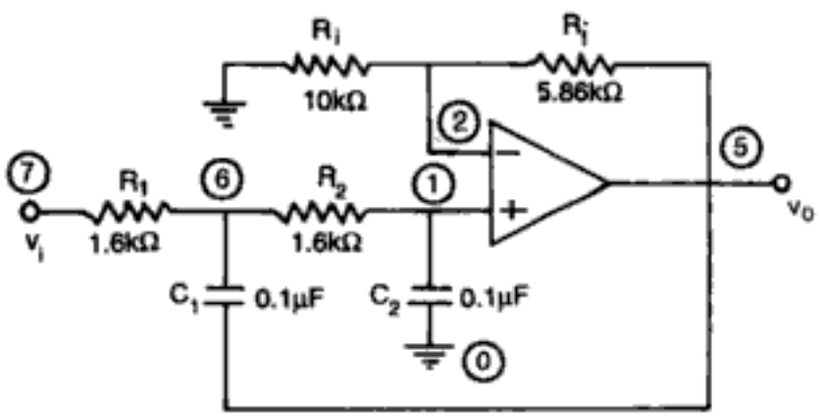

Fig. E.7.1 Second order low-pass filter

4. Calculate the theoretical value of upper cut-off frequency f_h and the pass band gain A_o:

$$f_h = \frac{1}{2\pi RC}; \quad \begin{bmatrix} R_1 = R_2 = R \\ C_1 = C_2 = C \end{bmatrix}$$

$$A_o\,(\text{dB}) = 20 \log \left(1 + \frac{R_f}{R_i}\right)$$

High Pass Filter

5. Interchange the resistor R with the capacitor C to make the high pass filter and repeat step 2 and 3.
6. Calculate the theoretical value of the lower cut-off frequency f_l and pass band gain A_o using the formula of step 4.

Computer Program 7.1

Figure E.7.1 has been numbered for PSPICE simulation. The listing for this simulation is shown in Fig. C. 7.1(a) and the frequency response is shown in Fig. C. 7.1(b).

Fig. C. 7.1 (a) Program Listing

```
*2nd order low pass Butterworth filter (Sallen key filter)
* * * * Circuit Description
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
    *LOWPASS BUTTERWORTH FILTER
    R1  7  6  1.6K
    R2  6  1  1.6K
    C1  6  5  0.1uF
    C2  1  0  0.1uF
    Ri  0  2  10K
    Rf  2  5  5.86k
*   Op-amp analysis
    X1  1  2  3  4  5  UA741
    .LIB  EVAL.LIB
*   Power supplies
    VCC  3  0  dc  12V
    VEE  0  4  dc  12V
    VIN  7  0  Ac  1V
    . AC DEC 20 1HZ 10 kHZ
    . PROBE
    □
```

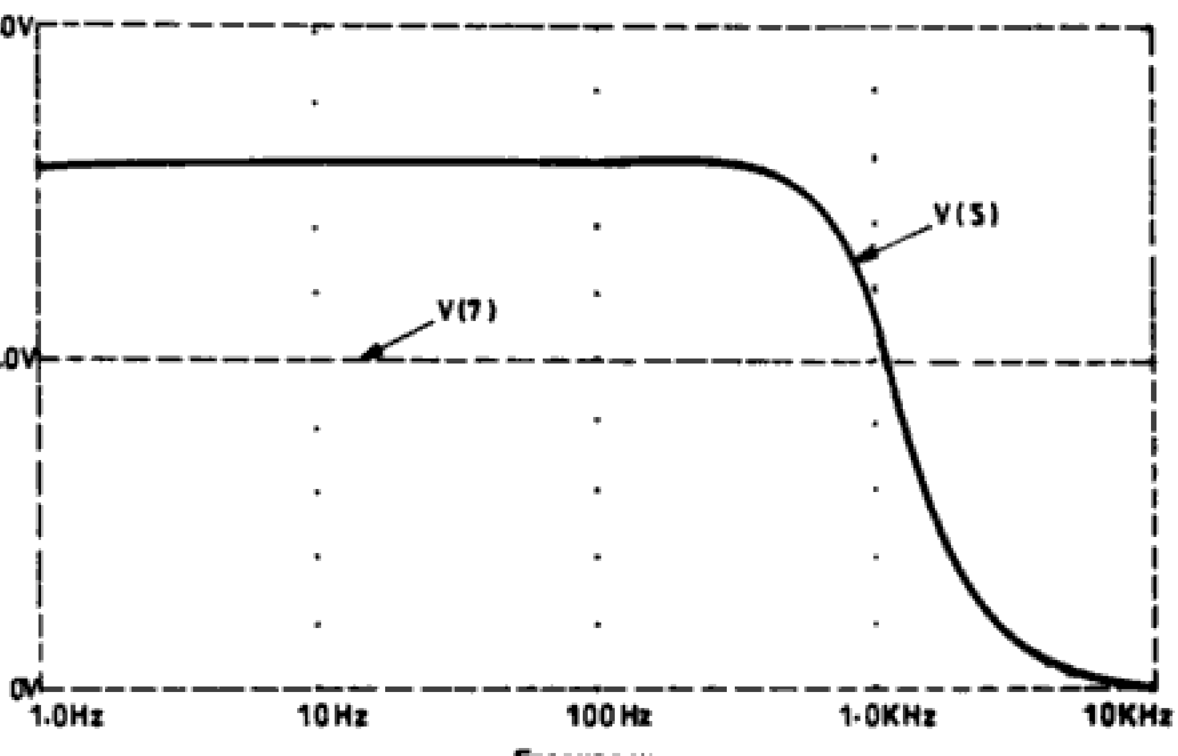

Fig. C. 7.1 (b) Frequency response of 2nd order low-pass filter

APPENDIX 7.1

Approximation Methods for Filter Design

We here consider techniques for approximating ideal filter transmission characteristics specifically for low pass filter.

Consider a realizable magnitude function that approximates the ideal low pass characteristics shown by dotted curve in Fig. 7.1 (a).

$$|H(j\omega)| = \frac{H(0)}{\sqrt{1+(\omega/\omega_0)^{2n}}}; n = 1, 2, 3 \ldots. \qquad \text{(A.7.1)}$$

This is known as the n-th order Butterworth or maximally flat response at $\omega = 0$. From the Binomial series expansion, $H(j\omega)$ can be written as †

$$|H(j\omega) = H(0)\left[1+\left(\frac{\omega}{\omega_0}\right)^{2n}\right]^{-1/2}$$

$$= H(0)\left[1-\frac{1}{2}\left(\frac{\omega}{\omega_0}\right)^{2n}+\frac{3}{8}\left(\frac{\omega}{\omega_0}\right)^{4n}-\frac{5}{16}\left(\frac{\omega}{\omega_0}\right)^{6n}+\ldots.\right] \qquad \text{(A.7.2)}$$

It can be seen that the first $(2n - 1)$ derivatives of $H(\omega)$ are zero at $\omega = 0$. Naturally approximation improves as n increases.

The pole locations corresponding to Eq. (A. 7.1) can be determined as,

$$|H(s)|^2 = H(s)\ H(-s) = \frac{H^2(0)}{1+(-s^2)^n} \qquad \text{(A. 7.3)}$$

The location of poles of $H(s)$ are found from,

$$1 + (-s^2)^n = 0 \qquad \text{(A. 7.4)}$$

The pole locations are:

$$s_k = \exp\left[j\left(\frac{2k-1}{n}\right)\frac{\pi}{2}\right]; n \text{ even} \qquad \text{(A. 7.5)}$$

$$s_k = \exp\left[j\,\frac{2k}{n}\cdot\frac{\pi}{2}\right]; n \text{ odd} \qquad \text{(A. 7.6)}$$

$$s_k = \exp\left[j\,\frac{2k+n-1}{2n}\cdot\frac{\pi}{2}\right]; k = 1, 2, \ldots\ldots, 2n. \qquad \text{(A. 7.7)}$$

---

† $(1+x)^{-n} = 1 + (-n)x + \dfrac{(-n)(-n-1)}{2!}x^2 + \dfrac{(-n)(-n-1)(-n-2)}{3!}x^3 + \ldots$

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Table A. 7.1 Computation of Butterworth Polynomial

n	Angles from either real axis; in degrees	$\lvert\cos\theta\rvert$	$\alpha = 2\cos\theta$	Butterworth Polynomial
1.	0	1		$s + 1$
2.	± 45	0.70711	1.414	$s^2 + 1.414\,s + 1$
3.	0	1		$(s + 1)(s^2 + s + 1)$
	± 60	0.5	1	$= s^3 + 2s^2 + 2s + 1$
4.	± 22.5	0.92388	1.84776	$(s^2 + 1.848\,s + 1)(s^2 + 0.765\,s$
	± 67.5	0.38268	0.76536	$+ 1) = s^4 + 2.613\,s^3 + 3.414\,s^2$ $2.613\,s + 1$
5.	0	1		$(s + 1)(s^2 + 1.618\,s + 1)$ $(s^2 + 0.618s + 1)$
	± 36	0.80902	1.61804	
	± 72	0.30902	0.61804	$= s^5 + 3.236s^4 + 5.236s^3 +$ $5.236s^2 + 3.236s + 1$
6.	± 15	0.96593	1.93186	$(s^2 + 1.932s + 1)(s^2 + 1.414s$ $+ 1)(s^2 + 0.518s + 1)$
	± 45	0.70711	1.41422	$= s^6 + 3.863s^5 + 7.464s^4 +$ $9.141s^3 + 7.464s^2 + 3.863s + 1$
	± 75	0.25822	0.51644	

8

555 Timer

8.1 INTRODUCTION

The 555 timer is a highly stable device for generating accurate time delay or oscillation. Signetics Corporation first introduced this device as the SE555/NE555 and it is available in two package styles, 8–pin circular style, TO–99 can or 8–pin mini DIP or as 14–pin DIP. The 556 timer contains two 555 timers and is a 14-pin DIP. There is also available counter timer such as Exar's XR-2240 which contains a 555 timer plus a programmable binary counter in a single 16-pin package. A single 555 timer can provide time delay ranging from microseconds to hours whereas counter timer can have a maximum timing range of days.

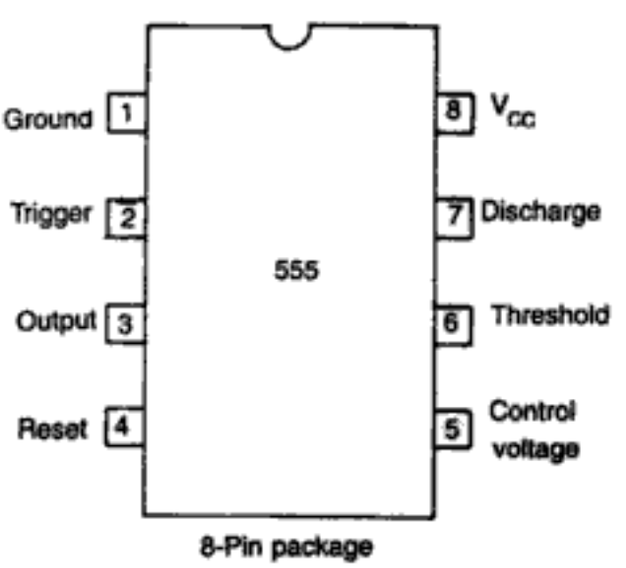

Fig. 8.1 Pin diagram

The 555 timer can be used with supply voltage in the range of + 5 V to + 18 V and can drive load upto 200 mA. It is compatible with both TTL and CMOS logic circuits. Because of the wide range of supply

voltage, the 555 timer is versatile and easy to use in various applications. Various applications include oscillator, pulse generator, ramp and square wave generator, mono-shot multivibrator, burglar alarm, traffic light control and voltage monitor etc.

8.2 DESCRIPTION OF FUNCTIONAL DIAGRAM

Figure 8.1 gives the pin diagram and Fig. 8.2 gives the functional diagram for 555 IC timer. Referring to Fig. 8.2, three 5 kΩ internal resistors act as voltage divider, providing bias voltage of (2/3) V_{cc} to the upper comparator (UC) and (1/3) V_{cc} to the lower comparator (LC), where V_{cc} is the supply voltage. Since these two voltages fix the necessary comparator threshold voltage, they also aid in determining the timing interval. It is possible to vary time electronically too, by applying a modulation voltage to the control voltage input terminal (pin 5). In applications, where no such modulation is intended, it is recommended by manufacturers that a capacitor (0.01 μF) be connected between control voltage terminal (pin 5) and ground to by-pass noise or ripple from the supply.

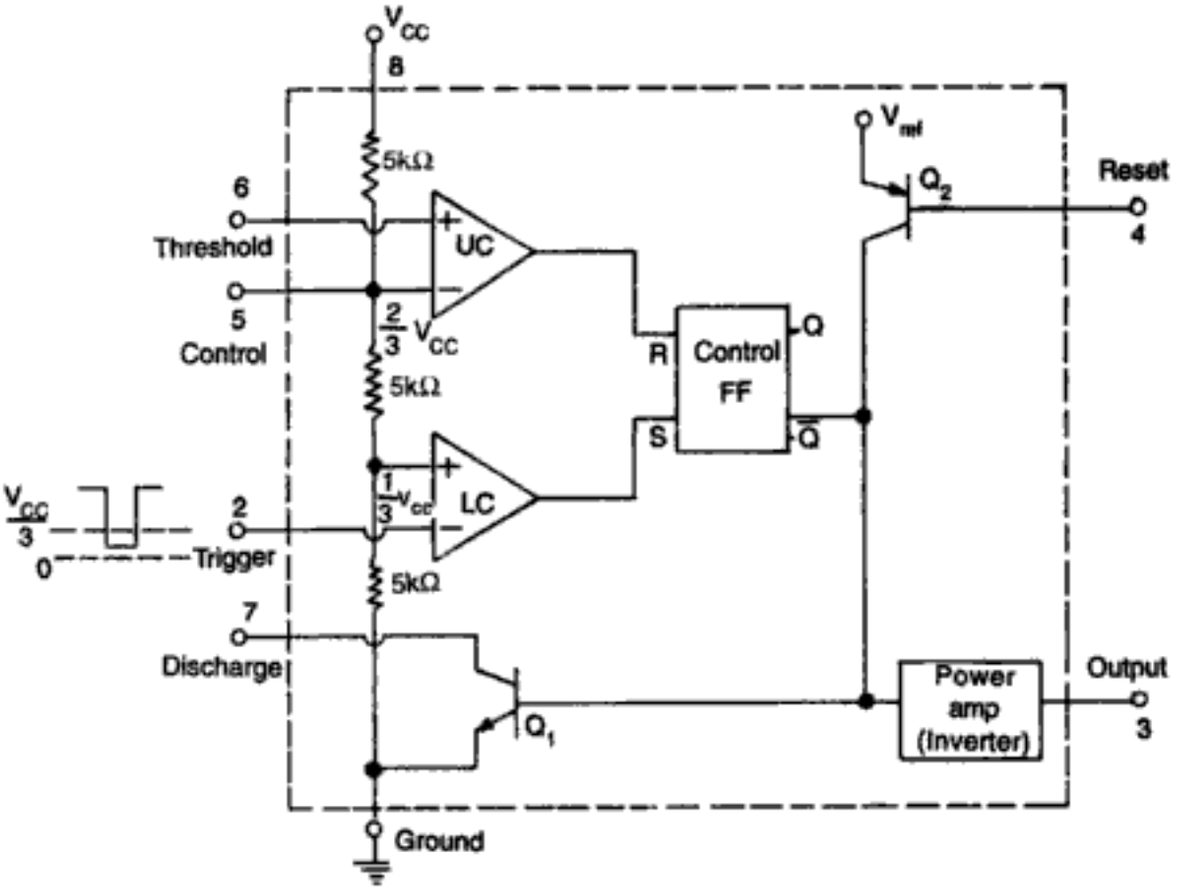

Fig. 8.2 Functional diagram of 555 timer

In the standby (stable) state, the output $\overline{Q}$ of the control flip-flop (FF) is HIGH. This makes the output LOW because of power amplifier which is basically an inverter. A negative going trigger pulse is applied to pin 2 and should have its dc level greater than the threshold level

of the lower comparator (i.e. $V_{cc}/3$). At the negative going edge of the trigger, as the trigger passes through ($V_{cc}/3$), the output of the lower comparator goes HIGH and sets the FF ($Q = 1$, $\overline{Q} = 0$). During the positive excursion, when the threshold voltage at pin 6 passes through (2/3) V_{cc}, the output of the upper comparator goes HIGH and resets the FF ($Q = 0$, $\overline{Q} = 1$).

The reset input (pin 4) provides a mechanism to reset the FF in a manner which overrides the effect of any instruction coming to FF from lower comparator. This overriding reset is effective when the reset input is less than about 0.4 V. When this reset is not used, it is returned to V_{cc}. The transistor Q_2 serves as a buffer to isolate the reset input from the FF and transistor Q_1. The transistor Q_2 is driven by an internal reference voltage V_{ref} obtained from supply voltage V_{cc}.

8.3 MONOSTABLE OPERATION

Figure 8.3 shows a 555 timer connected for monostable operation and its functional diagram is shown in Fig. 8.4. In the standby state, FF holds transistor Q_1 ***on***, thus clamping the external timing capacitor C to ground. The output remains at ground potential, i.e. LOW. As the trigger passes through $V_{cc}/3$, the FF is set, i.e. $\overline{Q} = 0$. This makes the transistor Q_1 ***off*** and the short circuit across the timing capacitor C is released. As $\overline{Q}$ is LOW, output goes HIGH (= V_{cc}). The timing cycle now begins. Since C is unclamped, voltage across it rises exponentially through R towards V_{cc} with a time constant RC

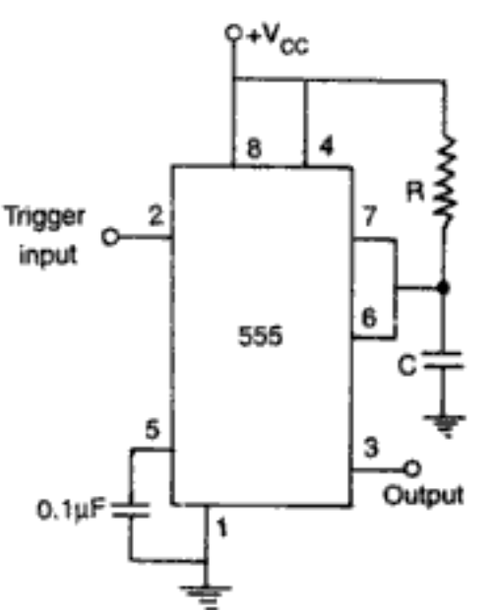

Fig. 8.3 Monostable multivibrator

as in Fig. 8.5(b). After a time period T (calculated later) the capacitor voltage is just greater than (2/3) V_{cc} and the upper comparator resets the FF, that is, $R = 1$, $S = 0$ (assuming very small trigger pulse width). This makes $\overline{Q} = 1$, transistor Q_1 goes ***on*** (i.e. saturates), thereby

discharging the capacitor C rapidly to ground potential. The output returns to the standby state or ground potential as shown in Fig. 8.5 (c).

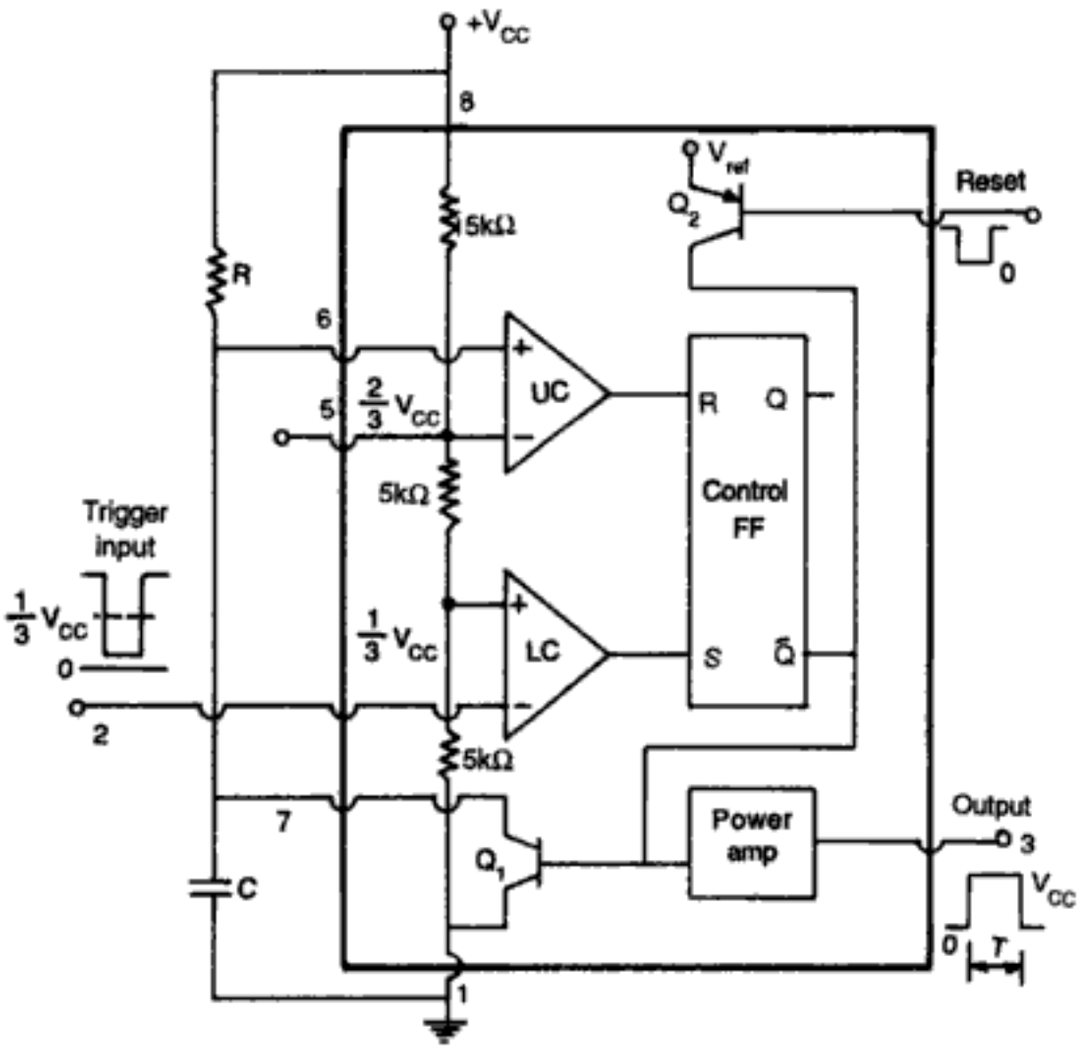

Fig. 8.4 Timer in monostable operation with functional diagram

The voltage across the capacitor as in Fig. 8.5(b) is given by

$$v_c = V_{cc}\,(1 - e^{-t/RC}) \tag{8.1}$$

At $t = T$, $\quad v_c = (2/3)\,V_{cc}$

Therefore, $\quad \frac{2}{3}V_{cc} = V_{cc}\,(1 - e^{-T/RC})$

or, $\quad T = RC \ln (1/3)$

or, $\quad T = 1.1\,RC$ (seconds) $\tag{8.2}$

It is evident from Eq. (8.2) that the timing interval is independent of the supply voltage. It may also be noted that once triggered, the output remains in the HIGH state until time T elapses, which depends only upon R and C. Any additional trigger pulse coming during this time will not change the output state. However, if a negative going reset pulse as in Fig. 8.5(d) is applied to the reset terminal (pin-4)

during the timing cycle, transistor Q_2 goes ***off***, Q_1 becomes ***on*** and the external timing capacitor C is immediately discharged. The output now will be as in Fig. 8.5 (e). It may be seen that the output of Q_2 is connected directly to the input of Q_1 so as to turn ***on*** Q_1 immediately and thereby avoid the propagation delay through the FF. Now, even

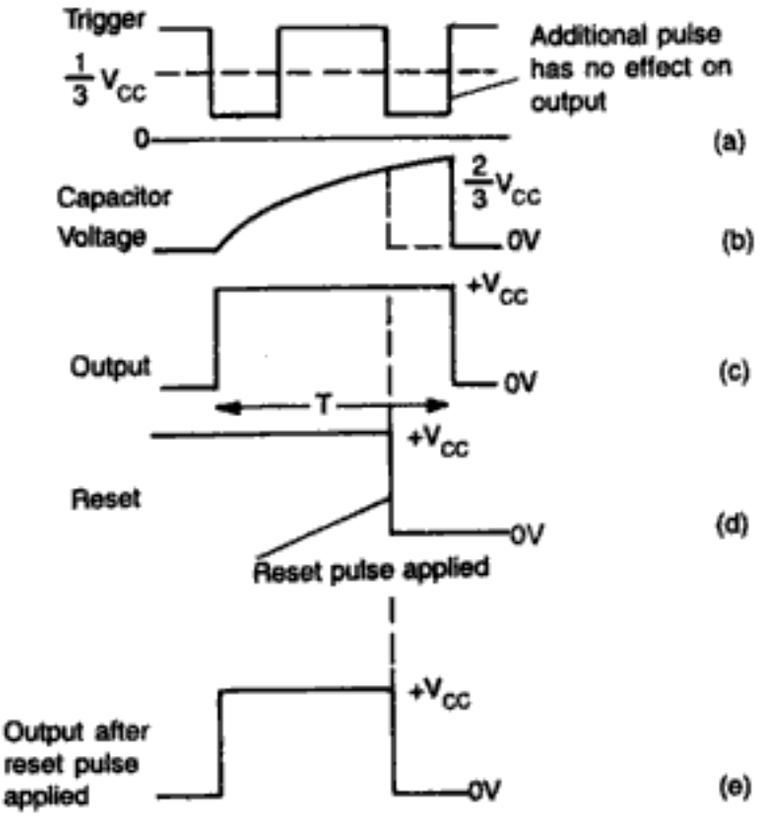

Fig. 8.5 Timing pulses

if the reset is released, the output will still remain LOW until a negative going trigger pulse is again applied at pin 2. Figure 8.6 shows a graph of the various combinations of R and C necessary to produce a given time delay.

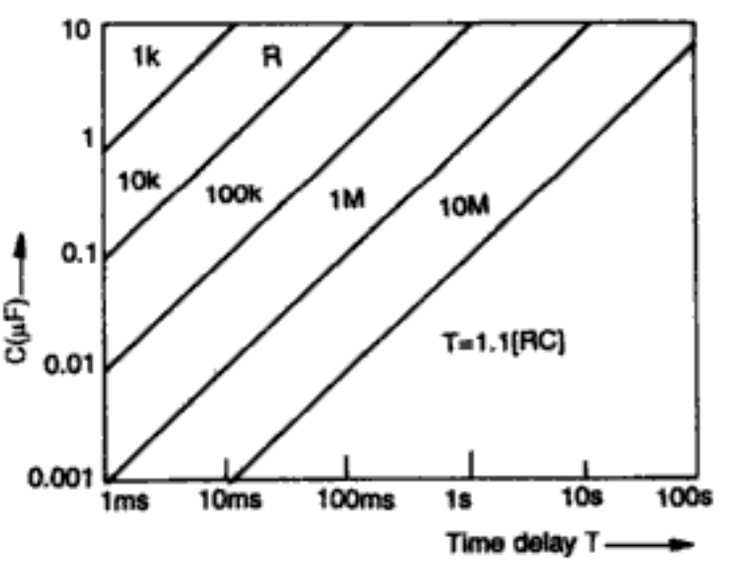

Fig. 8.6 Graph of *RC* combinations for different time delays

Sometimes the monostable circuit of Fig. 8.3 mistriggers on positive pulse edges, even with the control pin bypass capacitor. To prevent this, a modified circuit as shown in Fig. 8.7 is used. Here the resistor and capacitor combination of 10 kΩ and 0.001 μF at the input forms a differentiator. During the positive going edge of the trigger, diode *D* becomes forward biased, thereby limiting the amplitude of the positive spike to 0.7V.

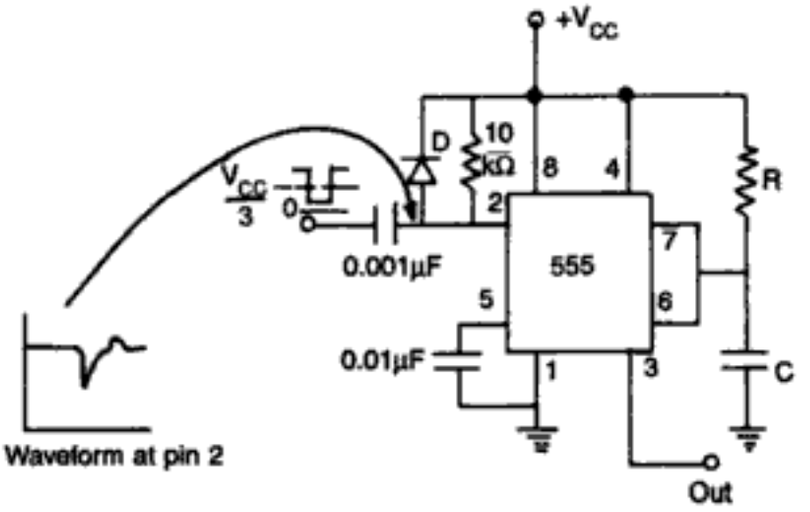

Fig. 8.7 Modified monostable circuit

Example 8.1

In the monostable multivibrator of Fig. 8.3, $R = 100$ kΩ and the time delay $T = 100$ mS. Calculate the value of C. Verify the value of C obtained from the graphs of Fig. 8.6.

Solution

From Eq. (8.2)., we get

$$C = T/1.1\ R = 100 \times 10^{-3}/1.1 \times 100 \times 10^{3} = 0.9\ \mu F$$

From the graph of Fig. 8.6, the value of C is found to be 0.9 μF also.

8.3.1 Applications in Monostable Mode

Missing Pulse Detector

Missing pulse detector circuit using 555 timer is shown in Fig. 8.8. Whenever, input trigger is low, the emitter diode of the transistor Q is forward biased. The capacitor C gets clamped to few tenths of a volt (~ 0.7V). The output of the timer goes HIGH. The circuit is designed so that the time period of the monostable circuit is slightly greater (1/3 longer) than that of the triggering pulses. So long the trigger pulse train keeps coming at pin 2, the output remains HIGH. However, if a pulse misses, the trigger input is high and transistor Q is cut off. The 555 timer enters into normal state of monostable operation. The output goes LOW after time T of the mono-shot. Thus this type of circuit can be used to detect missing heartbeat. It can also be used for

speed control and measurement. If input trigger pulses are generated from a rotating wheel, the circuit tells when the wheel speed drops below a predetermined value.

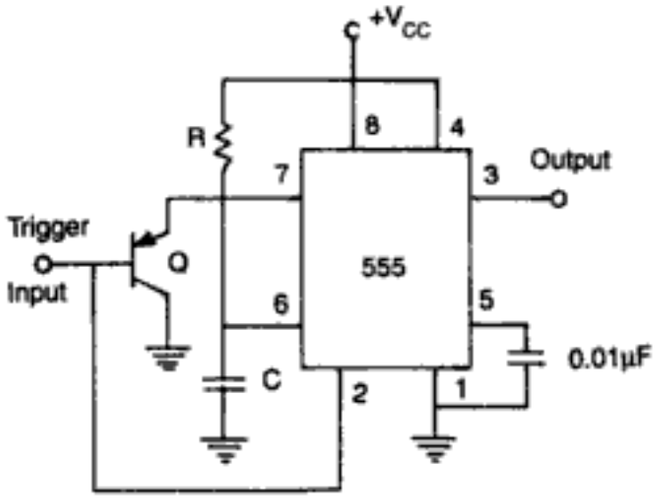

Fig. 8.8 A missing pulse detector monostable circuit

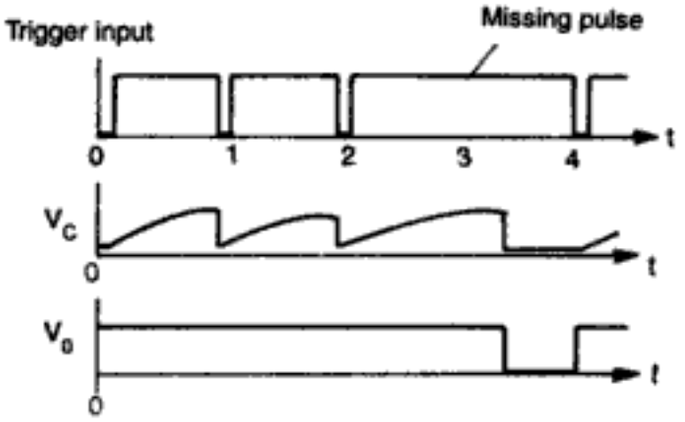

Fig. 8.9 Output of missing pulse detector

Linear Ramp Generator

Linear ramp can be generated by the circuit shown in Fig. 8.10. The resistor R of the monostable circuit is replaced by a constant current source. The capacitor is charged linearly by the constant current source formed by the transistor Q_3. The capacitor voltage v_c can be written as

$$v_c = \frac{1}{C}\int_0^t i\,dt \tag{8.3}$$

where i is the current supplied by the constant current source. Further, the KVL equation can be written as

$$\frac{R_1}{R_1 + R_2} V_{cc} - V_{BE} = (\beta + 1) I_B R_E \approx \beta I_B R_E = I_C R_E = i R_E \tag{8.4}$$

where I_B, I_C are the base current and collector current respectively, β is the current amplification factor in CE-mode and is very high. Therefore,

$$i = \frac{R_1 V_{cc} - V_{BE}(R_1 + R_2)}{R_E (R_1 + R_2)} \tag{8.5}$$

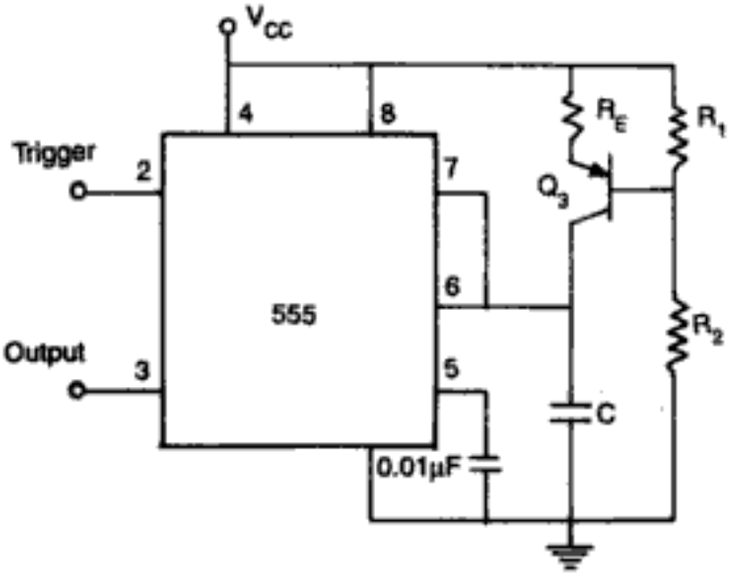

Fig. 8.10 Linear ramp generator

Now putting the value of the current i in Eq. (8.3), we get

$$v_c = \frac{R_1 V_{cc} - V_{BE}(R_1 + R_2)}{C\, R_E (R_1 + R_2)} \times t \tag{8.6}$$

At time $t = T$, the capacitor voltage v_c becomes (2/3) V_{cc}. Then we get

$$\frac{2}{3} V_{cc} = \frac{R_1 V_{cc} - V_{BE}(R_1 + R_2)}{R_E (R_1 + R_2) C} \times T \tag{8.7}$$

which gives the time period of the linear ramp generator as

$$T = \frac{(2/3)\, V_{cc} R_E (R_1 + R_2) C}{R_1 V_{cc} - V_{BE}(R_1 + R_2)} \tag{8.8}$$

The capacitor discharges as soon as its voltage reaches (2/3) V_{cc} which is the threshold of the upper comparator in the monostable circuit functional diagram. The capacitor voltage remains zero till another trigger is applied. The various waveforms are shown in Fig. 8.11.

The practical values can be noted as
R_1 = 47 kΩ; R_2 = 100 kΩ; R_E = 2.7 kΩ; C = 0.1 μF.
V_{cc} = 5 V (any value between 5 to 18V can be chosen)

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Pulse Width Modulation

The circuit is shown in Fig. 8.13. This is basically a monostable multivibrator with a modulating input signal applied at pin-5. By the application of continuous trigger at pin-2, a series of output pulses are obtained, the duration of which depends on the modulating input at pin-5. The modulating signal applied at pin-5 gets superimposed upon the already existing voltage (2/3) V_{cc} at the inverting input terminal of UC. This in turn changes the threshold level of UC and the output pulse width modulation takes place. The modulating signal and the output waveform are shown in Fig. 8.14. It may be noted from the output waveform that the pulse duration, that is, the duty cycle only varies, keeping the frequency same as that of the continuous input pulse train trigger.

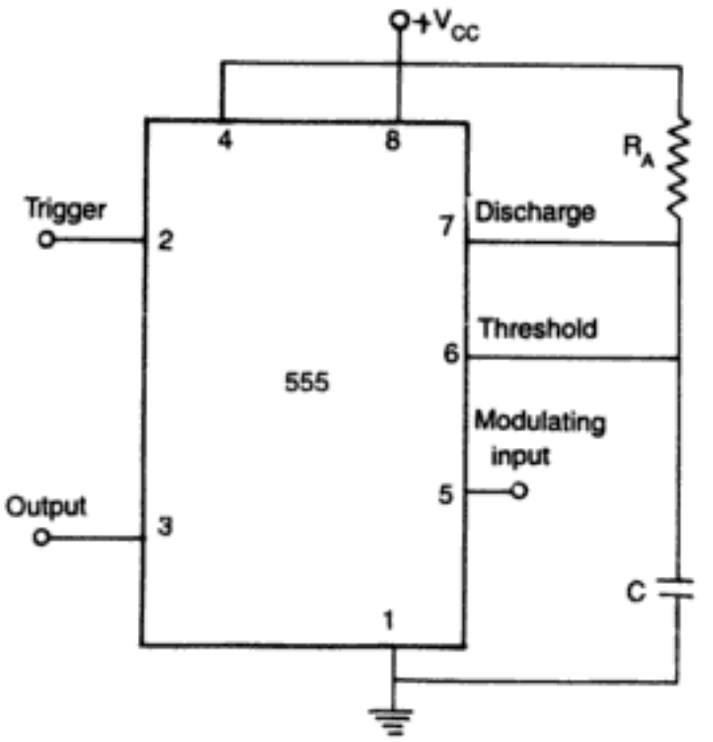

Fig. 8.13 Pulse width modulator

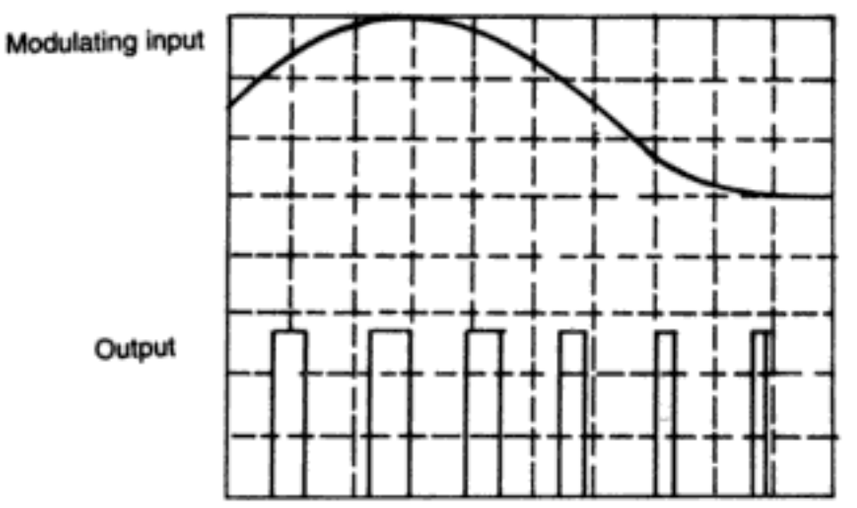

Fig. 8.14 Pulse width modulator waveforms

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$(R_A + R_B)C$. During this time, output (pin 3) is high (equals V_{cc}) as Reset $R = 0$, Set $S = 1$ and this combination makes $\overline{Q} = 0$ which has unclamped the timing capacitor C.

When the capacitor voltage equals (to be precise is just greater than), (2/3) V_{cc} the upper comparator triggers the control flip-flop so that $\overline{Q} = 1$. This, in turn, makes transistor Q_1 ***on*** and capacitor C starts discharging towards ground through R_B and transistor Q_1 with a time constant R_BC (neglecting the forward resistance of Q_1). Current also flows into transistor Q_1 through R_A. Resistors R_A and R_B must be large enough to limit this current and prevent damage to the discharge transistor Q_1. The minimum value of R_A is approximately equal to $V_{cc}/0.2$ where 0.2 A is the maximum current through the ***on*** transistor Q_1.

During the discharge of the timing capacitor C, as it reaches (to be precise, is just less than) $V_{cc}/3$, the lower comparator is triggered and at this stage $S = 1$, $R = 0$, which turns $\overline{Q} = 0$. Now $\overline{Q} = 0$ unclamps the external timing capacitor C. The capacitor C is thus periodically charged and discharged between (2/3) V_{cc} and (1/3) V_{cc} respectively. Figure 8.17 shows the timing sequence and capacitor voltage wave form. The length of time that the output remains HIGH is the time for the capacitor to charge from (1/3) V_{cc} to (2/3) V_{cc}. It may be calculated as follows:

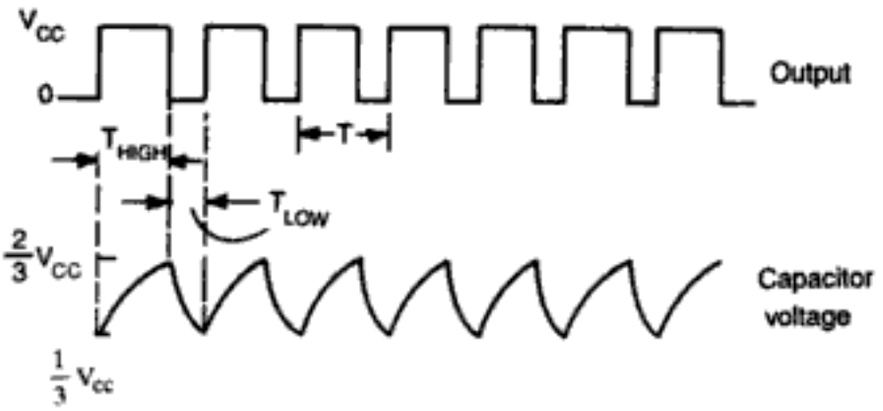

Fig. 8.17 Timing sequence of astable multivibrator

The capacitor voltage for a low pass RC circuit subjected to a step input of V_{cc} volts is given by

$$v_c = V_{cc}(1 - e^{-t/RC})$$

The time t_1 taken by the circuit to charge from 0 to (2/3) V_{cc} is,

$$(2/3)\, V_{cc} = V_{cc}(1 - e^{-t_1/RC}) \tag{8.9}$$

or, $$t_1 = 1.09\ RC$$

and the time t_2 to charge from 0 to (1/3) V_{cc} is,

$$(1/3)\, V_{cc} = V_{cc}(1 - e^{-t_2/RC}) \tag{8.10}$$

or, $$t_2 = 0.405\, RC$$

So the time to charge from (1/3) V_{cc} to (2/3) V_{cc} is

$$t_{HIGH} = t_1 - t_2$$

$$t_{HIGH} = 1.09\, RC - 0.405\, RC = 0.69\, RC$$

So, for the given circuit,

$$t_{HIGH} = 0.69\,(R_A + R_B)C \tag{8.11}$$

The output is low while the capacitor discharges from (2/3) V_{cc} to (1/3) V_{cc} and the voltage across the capacitor is given by

$$(1/3)\, V_{cc} = (2/3) V_{cc}\, e^{-t/RC}$$

solving, we get $$t = 0.69\, RC$$

So, for the given circuit, $t_{LOW} = 0.69\, R_B C$ (8.12)

Notice that both R_A and R_B are in the charge path, but only R_B is in the discharge path. Therefore, total time,

$$T = t_{HIGH} + t_{LOW}$$

or, $$T = 0.69\,(R_A + 2R_B)\, C$$

So, $$f = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C} \tag{8.13}$$

Figure 8.18 shows a graph of the various combinations of $(R_A + 2R_B)$ and C necessary to produce a given stable output frequency. The duty cycle D of a circuit is defined as the ratio of ON time to the total time period $T = (t_{ON} + t_{OFF})$. In this circuit, when the transistor Q_1 is ***on***, the output goes low. Hence,

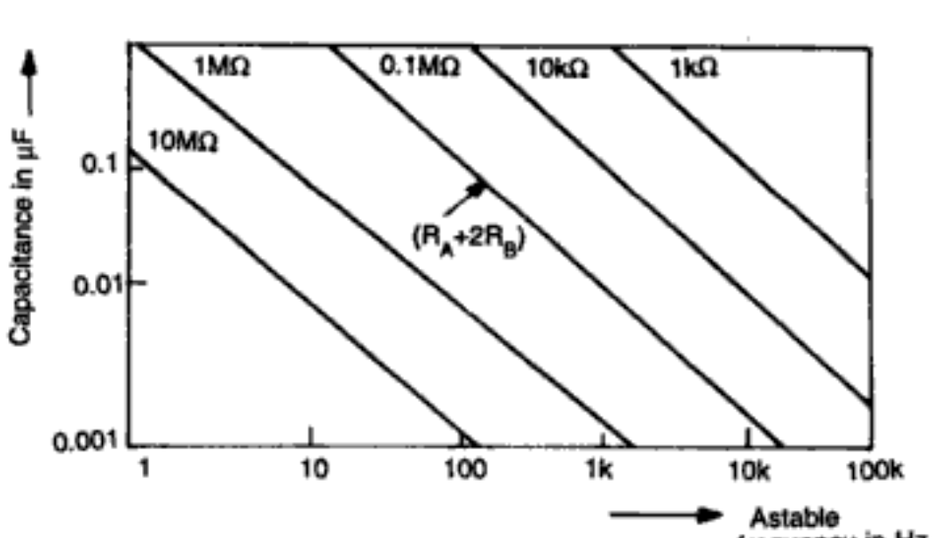

Fig. 8.18 Frequency dependence of R_A, R_B and C

$$D\% = \frac{t_{LOW}}{T} \times 100$$

$$= \frac{R_B}{R_A + 2R_B} \times 100 \tag{8.14}$$

With the circuit configuration of Fig. 8.15 it is not possible to have a duty cycle more than 50% since $t_{HIGH} = 0.69\ (R_A + R_B)\ C$ will always be greater than $t_{LOW} = 0.69\ R_B\ C$. In order to obtain a symmetrical square wave i.e. $D = 50\%$, the resistance R_A must be reduced to zero. However, now pin 7 is connected directly to V_{cc} and extra current will flow through Q_1 when it is ***on***. This may damage Q_1 and hence the timer.

An alternative circuit which will allow duty cycle to be set at practically any level is shown in Fig. 8.19. During the charging portion of the cycle, diode D_1 is forward biased effectively short circuiting R_B so that

$$t_{HIGH} = 0.69\ R_A C$$

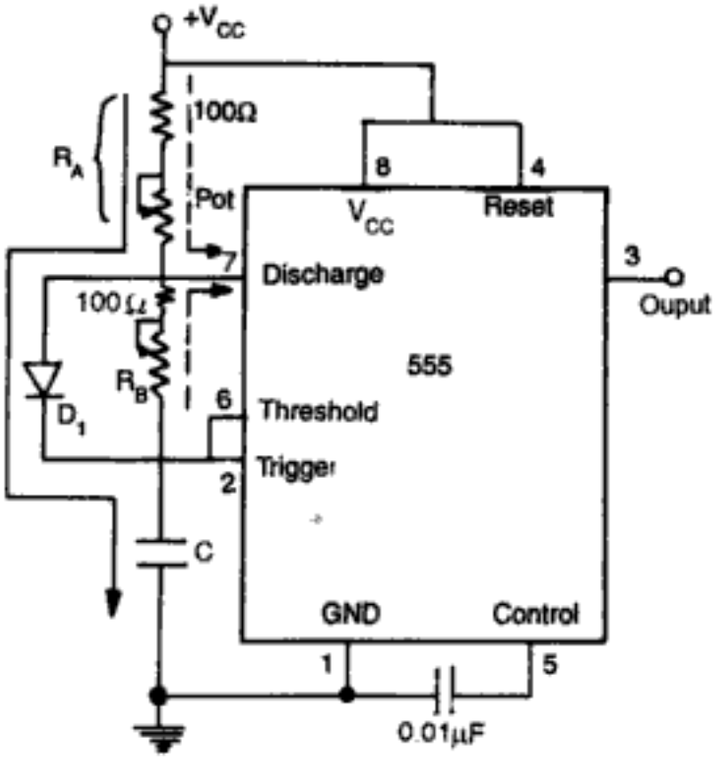

Fig. 8.19 Adjustable duty cycle rectangular wave generator

However, during the discharging portion of the cycle, transistor Q_1 becomes ON, thereby grounding pin 7 and hence the diode D_1 is reverse biased.

So $$t_{LOW} = 0.69\ R_B\ C \tag{8.15}$$

$$T = t_{HIGH} + t_{LOW} = 0.69\ (R_A + R_B)\ C \tag{8.16}$$

or, $$f = \frac{1.45}{(R_A + R_B)C} \tag{8.17}$$

and duty cycle $D = \dfrac{R_B}{R_A + R_B}$

Resistors R_A and R_B could be made variable to allow adjustment of frequency and pulse width. However, a series resistor of atleast 100 Ω (fixed) should be added to each R_A and R_B. This will limit peak current to the discharge transistor Q_1 when the variable resistors are at minimum value. And, if R_A is made equal to R_B, then 50% duty cycle is achieved.

Symmetrical square wave generator by adding a clocked JK flip-flop to the output of the nonsymmetrical square wave generator is shown in Fig. 8.20. The clocked flip-flop acts as binary divider to the timer output. The output frequency in this case will be one half that of the timer. The advantage of this circuit is of having output of 50% duty cycle without any restriction on the choice of R_A and R_B.

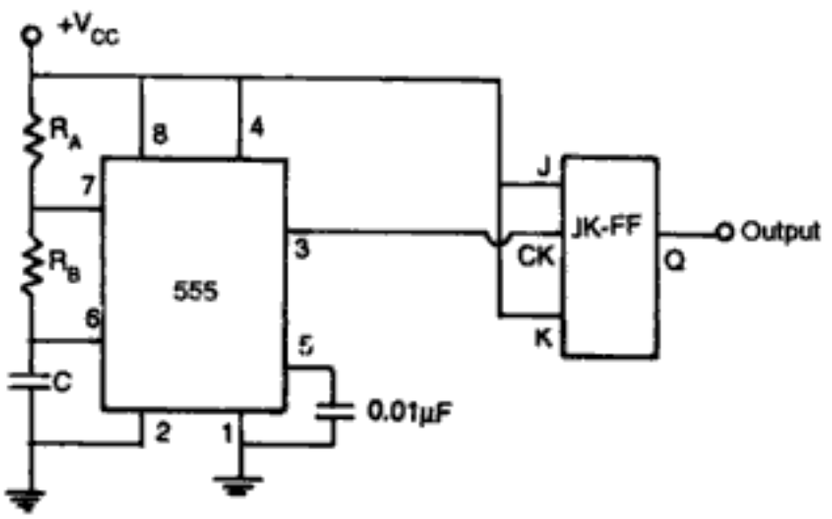

Fig. 8.20 Symmetrical waveform generator

Example 8.2

Refer Fig. 8.15. For $R_A = 6.8\ k\Omega$, $R_B = 3.3\ k\Omega$ and $C = 0.1\ \mu F$, calculate (a) t_{HIGH} (b) t_{LOW} (c) free running frequency (d) duty cycle, D.

Solution

(a) By Eq. (8.11)
$t_{HIGH} = 0.69\,(6.8\ k\Omega + 3.3\ k\Omega)\,(0.1\ \mu F) = 0.7\ ms$

(b) By Eq. (8.12)
$t_{LOW} = 0.69\,(3.3\ k\Omega)\,(0.1\ \mu F) = 0.23\ ms$

(c) $f = \dfrac{1.45}{[(6.8\ k\Omega) + (2)\,(3.3\ k\Omega)]\,(0.1\ \mu F)} = 1.07\ kHz$

(d) $D = \dfrac{t_{LOW}}{T} = \dfrac{R_B}{R_A + 2R_B}$

$$= \frac{3.3\ \text{k}\Omega}{6.8\ \text{k}\Omega + 2(3.3\ \text{k}\Omega)} = 0.25 \text{ or, } 25\%$$

8.4.1 Applications in Astable Mode

FSK Generator

In digital data communication, binary code is transmitted by shifting a carrier frequency between two preset frequencies. This type of transmission is called frequency shift keying (FSK) technique. A 555 timer in astable mode can be used to generate FSK signal. The circuit is as shown in Fig. 8.21. The standard digital data input frequency is 150 Hz. When input is HIGH, transistor Q is ***off*** and 555 timer works in the normal astable mode of operation. The frequency of the output waveform given by Eq. (8.1) can be rewritten as

$$f_o = \frac{1.45}{(R_A + 2R_B)C} \tag{8.18}$$

In a tele-typewriter using a modulator-demodulator (MODEM), a frequency between 1070 Hz to 1270 Hz is used as one of the standard FSK signals. The components R_A and R_B and the capacitor C can be selected so that f_o is 1070 Hz.

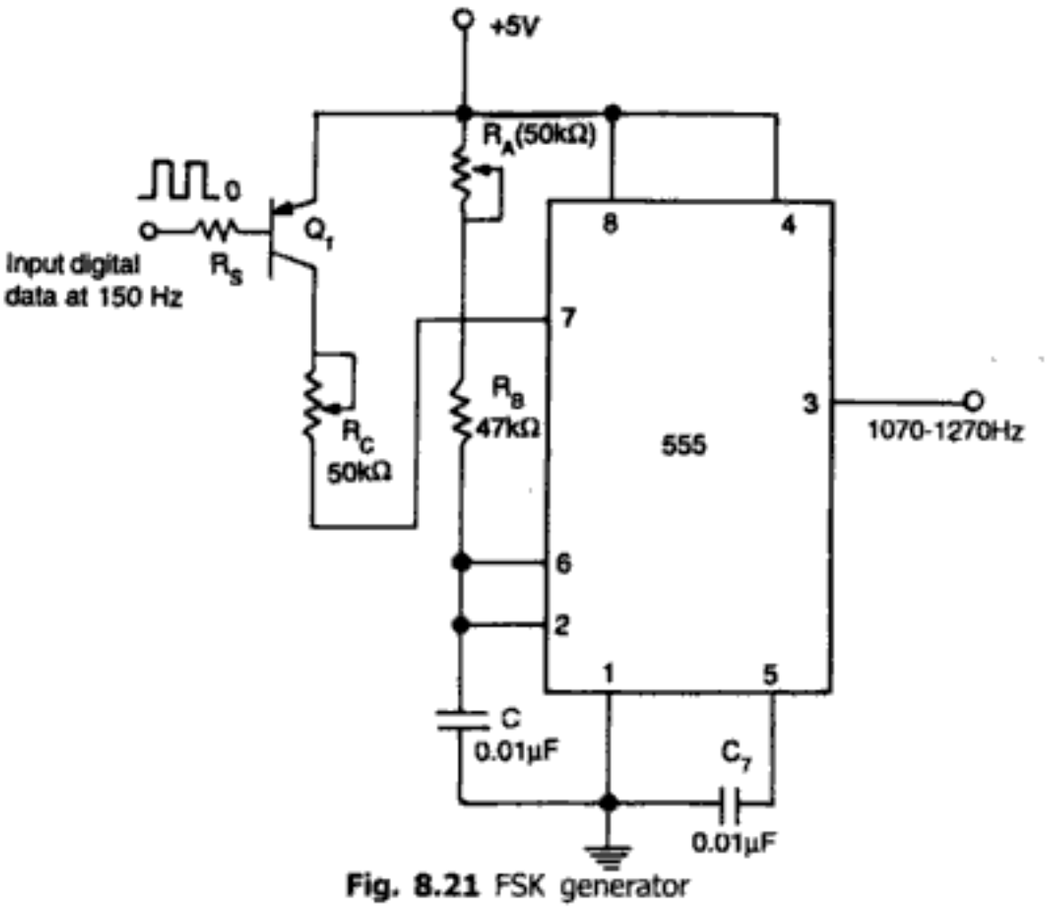

Fig. 8.21 FSK generator

When the input is LOW, Q goes ***on*** and connects the resistance R_c across R_A. The output frequency is now given by

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8.5 SCHMITT TRIGGER

The use of 555 timer as a Schmitt Trigger is shown in Fig. 8.24. Here the two internal comparators are tied together and externally biased at $V_{cc}/2$ through R_1 and R_2. Since the upper comparator will trip at (2/3) V_{cc} and lower comparator at (1/3) V_{cc}, the bias provided by R_1 and R_2 is centered within these two thresholds.

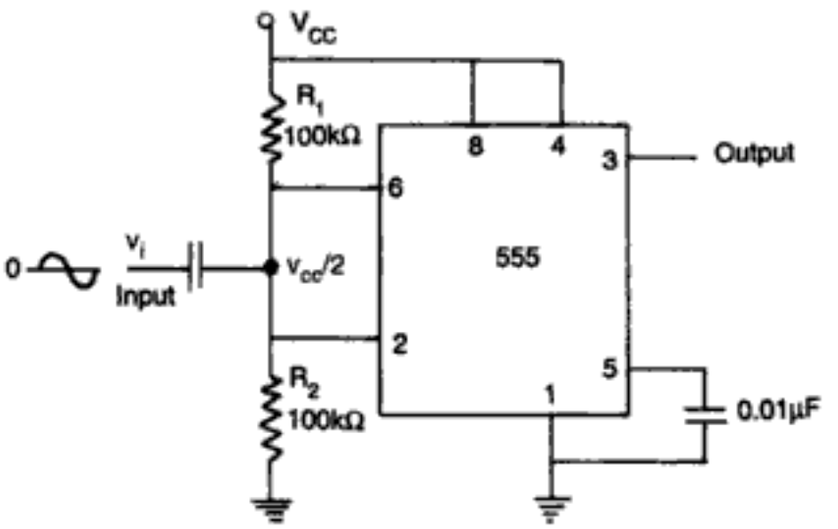

Fig. 8.24 Timer in Schmitt Trigger Operation

Thus, a sine wave of sufficient amplitude ($> V_{cc}/6 = 2/3\ V_{cc} - V_{cc}/2$) to exceed the reference levels causes the internal flip-flop to alternately set and reset, providing a square wave output as shown in Fig. 8.25.

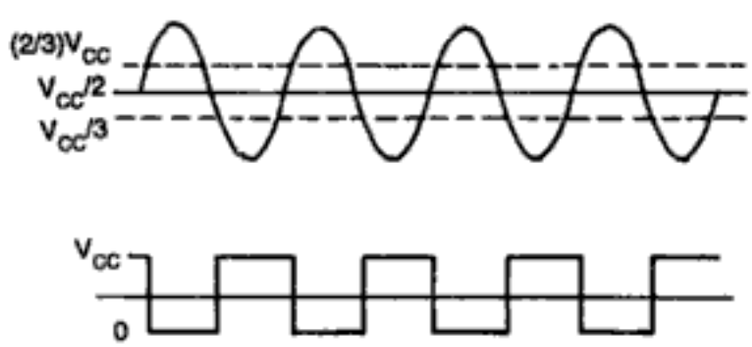

Fig. 8.25 Input output waveforms of Schmitt Trigger

It may be noted that unlike conventional multivibrator, no frequency division is taking place and frequency of square wave remains the same as that of input signal.

Summary

1. 555 IC Timer can produce very accurate and stable time delays, from microseconds to hours.
2. Timer is available in two packages, circular can and DIP.
3. It can be used with supply voltage varying from 5 to 18V and thus is compatible with TTL and CMOS circuits.

4. Timer can be used in monostable or astable mode of operation. Its various applications include waveform generator, missing pulse detector, frequency divider, pulse width modulator, burglar alarm, FSK generator, ramp generator, pulse position modulator etc.

Review Questions

8.1. Draw and explain the functional diagram of a 555 Timer.
8.2. Explain the function of reset.
8.3. What are the modes of operation of a timer?
8.4. Derive the expression of time delay of a monostable multivibrator.
8.5. Discuss some applications of timer in monostable mode.
8.6. Define duty cycle D.
8.7. Give methods for obtaining symmetrical square wave.
8.8. Discuss the operation of a FSK generator using 555 timer.
8.9. How is an astable multivibrator connected into a pulse position modulator?
8.10. Draw the circuit of a Schmitt trigger using 555 timer and explain its operation.

PROBLEMS

8.1. Design a monostable multivibrator using 555 timer to produce a pulse width of 100 ms. Verify the values of R and C obtained from the graph of Fig. 8.6.
8.2. The monostable multivibrator of Fig. 8.3 is used as a divide-by-3 network. The frequency of the input trigger is 15 kHz. If the value of $C = 0.01$ μF, calculate, the value of resistance R.
8.3. In the astable multivibrator of Fig. 8.15, $R_A = 2.2$ kΩ, $R_B = 6.8$ kΩ and $C = .01$ μF. Calculate (i) t_{HIGH} (ii) t_{LOW}, (iii) free running frequency, and (iv) duty cycle D.
8.4. Design a square waveform generator of frequency 100 Hz and duty cycle of 75%.
8.5. Design a symmetrical square waveform generator of 10 kHz.

Experiment

To construct and observe the waveforms of a 1 kHz square waveform generator using 555 timer for duty cycle, (a) $D = 0.25$; (b) $D = 0.50$.

Design aspects:

(a) Unsymmetrical square waveform generator

$$f = 1 \text{ kHz and } D = 0.25$$

In Fig. 8.15, $$f = \frac{1.45}{(R_A + 2R_B)C}$$

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9

Phase-Locked Loops

9.1 INTRODUCTION

The phase-locked loop (PLL) is an important building block of linear systems. Electronic phase-locked loop (PLL) came into vogue in the 1930s when it was used for radar synchronisation and communication applications. The high cost of realizing PLL in discrete form limited its use earlier. Now with the advanced IC technology, PLLs are available as inexpensive monolithic ICs. This technique for electronic frequency control is used today in satellite communication systems, air borne navigational systems, FM communication systems, computers etc. The basic principle of PLL, different ICs and important applications are discussed.

9.2 BASIC PRINCIPLES

The basic block schematic of the PLL is shown in Fig. 9.1. This feedback system consists of:

1. Phase detector/comparator
2. A low pass filter
3. An error amplifier
4. A Voltage Controlled Oscillator (VCO)

The VCO is a free running multivibrator and operates at a set frequency f_o called free running frequency. This frequency is determined by an external timing capacitor and an external resistor. It can also be shifted to either side by applying a dc control voltage v_c to an appropriate terminal of the IC. The frequency deviation is directly proportional to the dc control voltage and hence it is called a "Voltage Controlled Oscillator" or, in short, VCO.

If an input signal v_s of frequency f_s is applied to the PLL, the phase detector compares the phase and frequency of the incoming signal to that of the output v_o of the VCO. If the two signals differ in frequency

and/or phase, an error voltage v_e is generated. The phase detector is basically a multiplier and produces the sum $(f_s + f_o)$ and difference $(f_s - f_o)$ components at its output. The high frequency component $(f_s + f_0)$ is removed by the low pass filter and the difference frequency

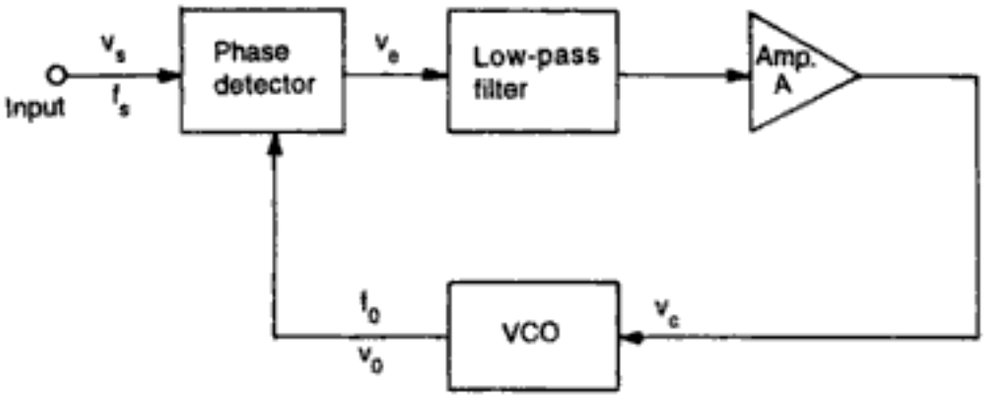

Fig. 9.1 Block schematic of the PLL

component is amplified and then applied as control voltage v_c to VCO. The signal v_c shifts the VCO frequency in a direction to reduce the frequency difference between f_s and f_o. Once this action starts, we say that the signal is in the capture range. The VCO continues to change frequency till its output frequency is exactly the same as the input signal frequency. The circuit is then said to be locked. Once locked, the output frequency f_o of VCO is identical to f_s except for a finite phase difference ϕ. This phase difference ϕ generates a corrective control voltage v_c to shift the VCO frequency from f_o to f_s and thereby maintain the lock. Once locked, PLL tracks the frequency changes of the input signal. Thus, a PLL goes through three stages (i) free running, (ii) capture and (iii) locked or tracking.

Figure 9.2 shows the capture transient. As capture starts, a small sine wave appears. This is due to the difference frequency between the VCO and the input signal. The dc component of the beat drives the VCO towards the lock. Each successive cycle causes the VCO frequency to move closer to the input signal frequency. The difference in frequency becomes smaller and a large dc component is passed by the filter, shifting the VCO frequency further. The process continues until the VCO locks on to the signal and the difference frequency is dc.

The low pass filter controls the capture range. If VCO frequency is far away, the beat frequency will be too high to pass through the filter and the PLL will not respond. We say that the signal is out of the capture band. However, once locked, the filter no longer restricts the PLL. The VCO can track the signal well beyond the capture band. Thus tracking range is always larger than the capture range.

Some of the important definitions in relation to PLL are:

Lock-in Range: Once the PLL is locked, it can track frequency changes in the incoming signals. The range of frequencies over which

the PLL can maintain lock with the incoming signal is called the lock-in range or tracking range. The lock range is usually expressed as a percentage of f_0, the VCO frequency.

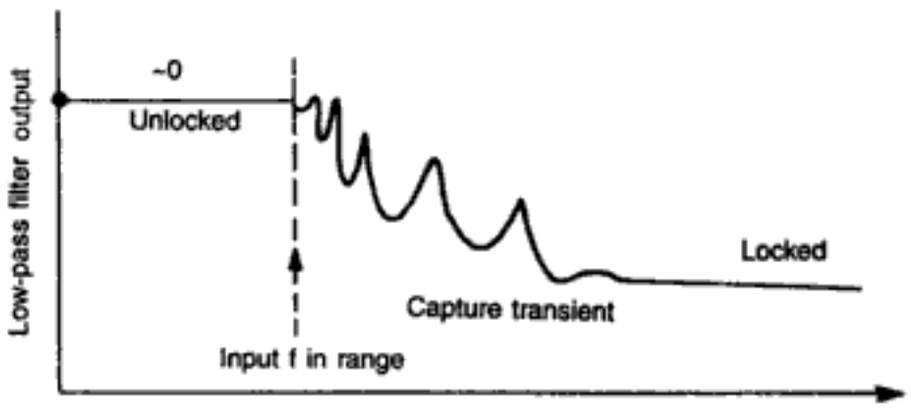

Fig. 9.2 The capture transient

Capture Range: The range of frequencies over which the PLL can acquire lock with an input signal is called the capture range. This parameter is also expressed as percentage of f_0.

Pull-in time: The total time taken by the PLL to establish lock is called pull-in time. This depends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics.

9.3 PHASE DETECTOR/COMPARATOR

The phase detection is the most important part of the PLL system. There are two types of phase detectors used, analog and digital.

9.3.1 Analog Phase Detector

The principle of analog phase detection using switch type phase detector is shown in Fig. 9.3(a). An electronic switch S is opened and closed by signal coming from VCO (normally a square wave) as shown in Fig. 9.3(b). The input signal is, therefore, chopped at a repetition rate determined by VCO frequency. Figure 9.3(c) shows the input signal v_s assumed to be in phase ($\phi = 0°$) with VCO output v_0. Since the switch S is closed only when VCO output is positive, the output waveform v_e will be half sinusoids (shown hatched). Similarly, the output waveform for $\phi = 90°$ and $\phi = 180°$ is shown in Fig. 9.3(d, e). This type of phase detector is called a half wave detector, since the phase information for only one-half of the input waveform is detected and averaged. The output of the phase comparator when filtered through a low pass filter gives an error signal which is the average value of the output waveform shown by dotted line in Fig. 9.3(c, d, e).

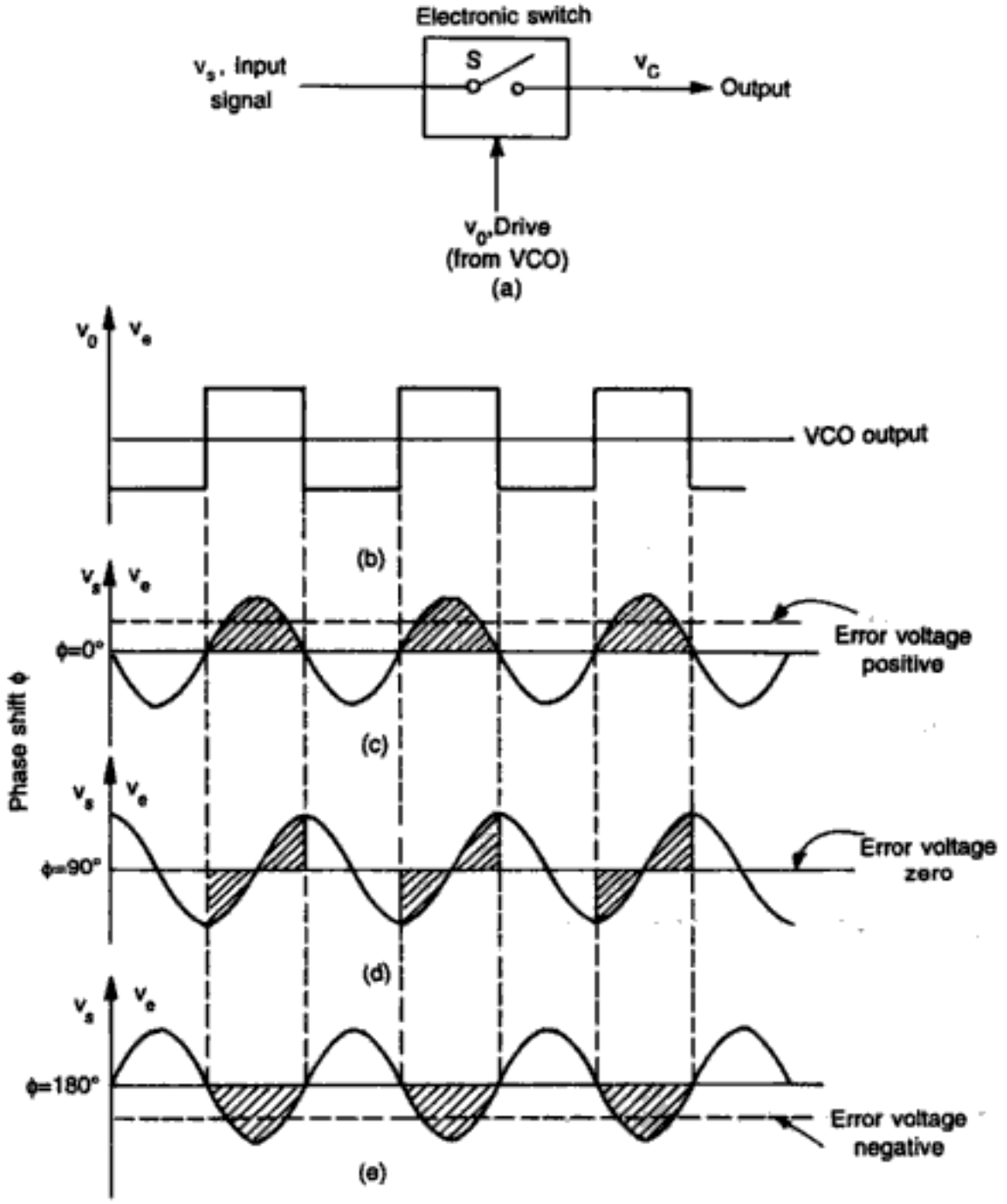

Fig. 9.3 Phase detector for PLL (a) Basic scheme (b) VCO output waveform. Input and output waveform (hatched) of phase detector for (c) $\phi = 0$ (d) $\phi = 90°$ (e) $\phi = 180°$

It may be seen that the error voltage is zero when the phase shift between the two inputs is 90°. So, for perfect lock, the VCO output should be 90° out of phase with respect to the input signal.

Analysis

A phase comparator is basically a multiplier which multiplies the input signal ($v_s = V_s \sin 2\pi f_s t$) by the VCO signal ($v_o = V_o \sin (2\pi f_o t + \phi)$. Thus the phase comparator output is,

$$v_e = KV_sV_o \sin (2\pi f_s t) \sin (2\pi f_o t + \phi) \qquad (9.1)$$

where K is the phase comparator gain (or attenuation constant) and ϕ is the phase shift between the input signal and the VCO output. Equation (9.1) can be simplified as,

$$v_e = \frac{KV_s V_o}{2}\left[\cos(2\pi f_s t - 2\pi f_o t - \phi) - \cos(2\pi f_s t + 2\pi f_o t + \phi)\right] \quad (9.2)$$

when at lock, that is, $f_s = f_o$,

$$\text{Then } v_e = \frac{KV_s V_o}{2}\left[\cos(-\phi) - \cos(2\pi \times 2 f_o t + \phi)\right]$$

This shows that the phase comparator output contains a double frequency term and a dc term $(KV_s V_o/2)\cos\phi$ which varies as a function of phase ϕ, that is, $\cos\phi$ between the two signals. The double frequency term is eliminated by the low pass filter and the dc signal is applied to the modulating input terminal of a VCO. It can be seen that in the perfect locked state ($f_s = f_o$), the phase shift should be 90° ($\cos 90° = 0$), in order to get zero error signal, that is, $v_e = 0$.

There are two problems associated with the switch type phase detector:

1. The output voltage v_e is proportional to the input signal amplitude V_s. This is undesirable since it makes phase detector gain and the loop gain dependent on the input signal amplitude.
2. The output is proportional to $\cos\phi$ and not proportional to ϕ making it non-linear.

Both these problems can be eliminated by limiting the amplitude of the input signal, that is, converting the input to a constant amplitude square wave. A circuit which performs phase comparison with square wave input is shown in Fig. 9.4(a). This is a balanced modulator used as full-wave switching phase detector. Here the input signal is applied to the differential pair Q_1Q_2. Transistors Q_3–Q_4 and Q_5–Q_6 are two sets of SPDT switches activated by the VCO output. The input signal v_s and the VCO output v_o are assumed to be high enough to switch the transistors in Fig. 9.4 (a) fully ***on*** or ***off***. In Fig. 9.4(b) when v_s and v_o both are high during the time 0 to $(\pi-\phi)$, transistors Q_1 and Q_3 are driven ***on*** and current I_E flows through Q_1 and Q_3. This gives an output voltage

$$v_e = -I_E R_L \quad (9.4)$$

Next for the period $(\pi - \theta)$ for π, when v_s is high and v_o is low, transistors Q_1 and Q_4 are driven ***on*** resulting in an output voltage

$$v_e = I_E R_L \quad (9.5)$$

In this way, the output voltage waveform v_e in Fig. 9.4(b) is obtained.

The average value of the phase detector output v_e can be calculated as,

$$(v_e)_{av} = \frac{1}{\pi}\left[(\text{area } A_1) + (\text{area } A_2)\right]$$

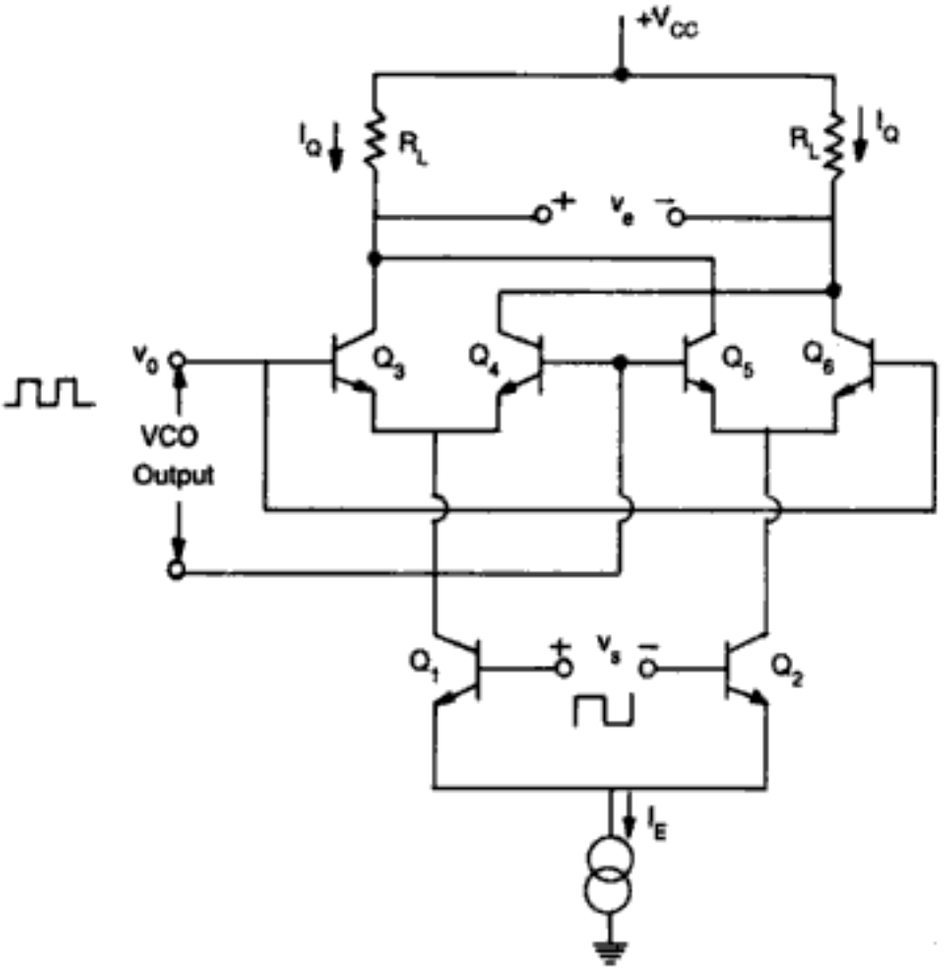

Fig. 9.4 (a) Phase detector for IC PLL

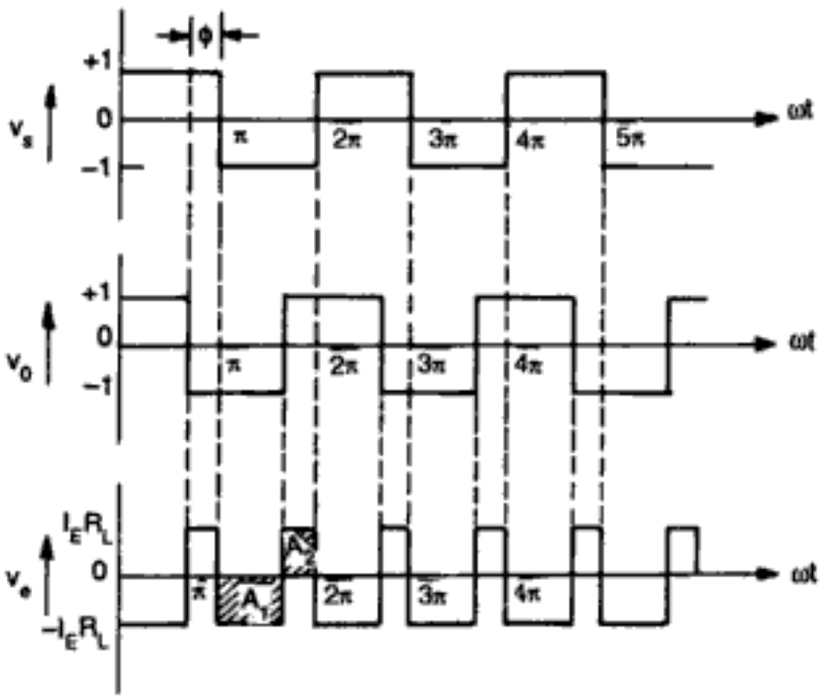

Fig. 9.4 (b) Timing diagram of input and output waveforms for balanced modulator circuit of Fig. 9.4 (a)

$$= \frac{1}{\pi}\left[I_E R_L \phi + (-I_E R_L) \times (\pi - \phi)\right]$$

$$= I_E R_L \left(\frac{2\phi}{\pi} - 1\right)$$

$$= 4\frac{I_Q R_L}{\pi}\left(\phi - \frac{\pi}{2}\right) \qquad [\text{Since } I_E = 2I_Q]$$

$$= K_\phi(\phi - \pi/2) \tag{9.6}$$

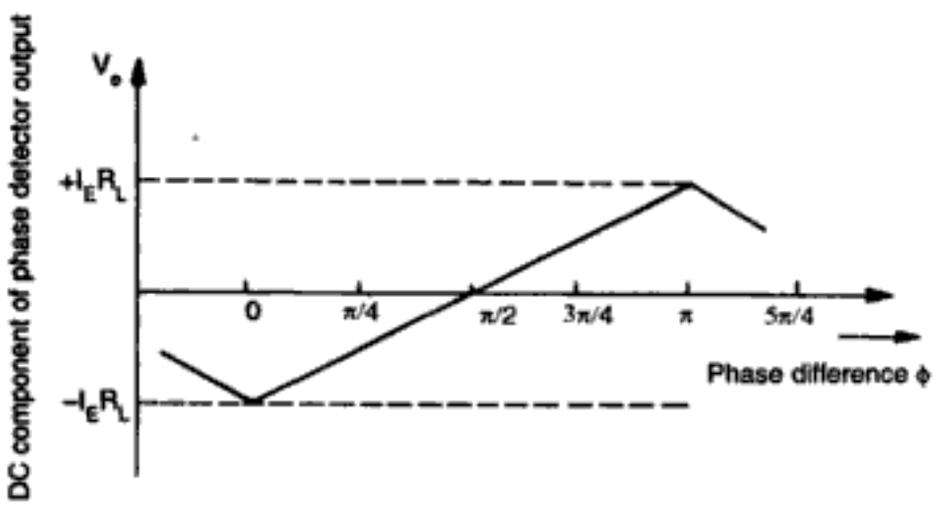

Fig. 9.4 (c) Output dc voltage versus input phase difference of balanced modulator full wave switching phase detector

where K_ϕ is the phase angle-to-voltage transfer coefficient or, the conversion ratio of the phase detector. This linear relationship between v_e and ϕ is depicted in Fig. 9.4 (c).

9.3.2 Digital Phase Detector

Figure 9.5(a) shows the digital type XOR (Exclusive–OR) phase detector. It uses CMOS type 4070 Quad 2-input XOR gate. The output of the XOR gate is high when only one of the inputs signals f_s or f_o is high. This type of detector is used when both the input signals are square waves. The input and output waveforms for $f_s = f_o$ are shown in Fig. 9.5(b). In this figure, f_s is leading f_o by ϕ degrees. The variation of dc output voltage with phase difference ϕ is shown in Fig. 9.5(c). It can be seen that the maximum dc output voltage occurs when the phase difference is π because the output of the gate remains high throughout. The slope of the curve gives the conversion ratio k_ϕ of the phase detector. So, the conversion ration K_ϕ for a supply voltage V_{cc} = 5V is,

$$K_\phi = \frac{5}{\pi} = 1.59 \ V/\text{rad} \tag{9.7}$$

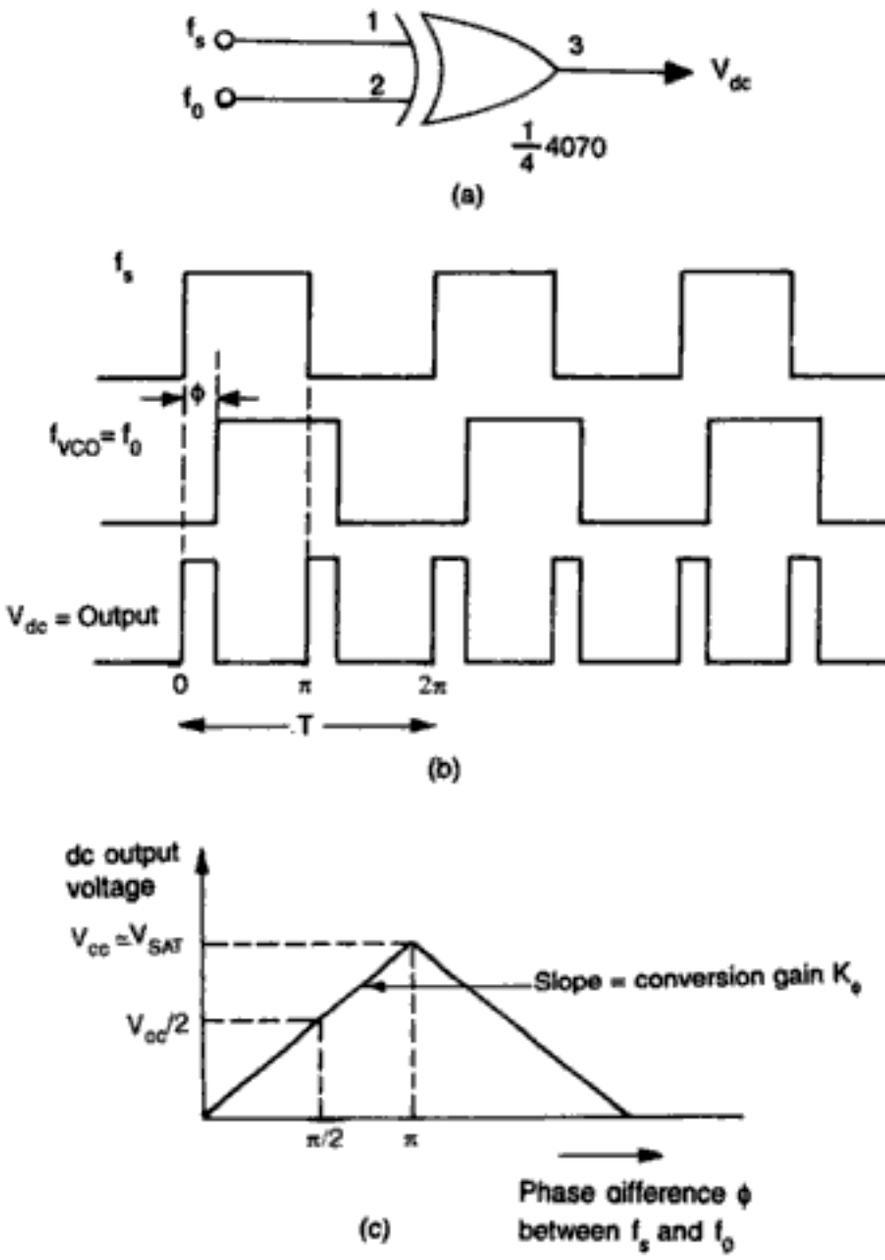

Fig. 9.5 (a) Exclusive-OR phase detector (b) Input and output waveforms (c) DC output voltage versus phase difference ϕ curve

Another type of digital phase detector is an edge-triggered phase detector as shown in Fig. 9.6(a). The circuit is an R-S flip-flop made by NOR gates, such as CD 4001. This circuit is useful when f_s (incoming signal) and f_0 (VCO output) are both pulse waveforms with duty cycle less than 50 percent. The output of the R-S flip-flop changes its state on the leading edge of f_s and f_0 as shown in Fig. 9.6(b). The variation of dc output voltage vs phase difference between f_s and f_0 is shown in Fig. 9.6(c). This type of detector has better capture tracking and locking characteristics as the dc output voltage is linear upto 360° compared to 180° in the case of Exclusive-OR detector.

Digital phase detector is also available in independent monolithic IC form. A typical example is MC4344/4044. This IC gives input/output transfer characteristics which is linear upto 4π radians or 720°.

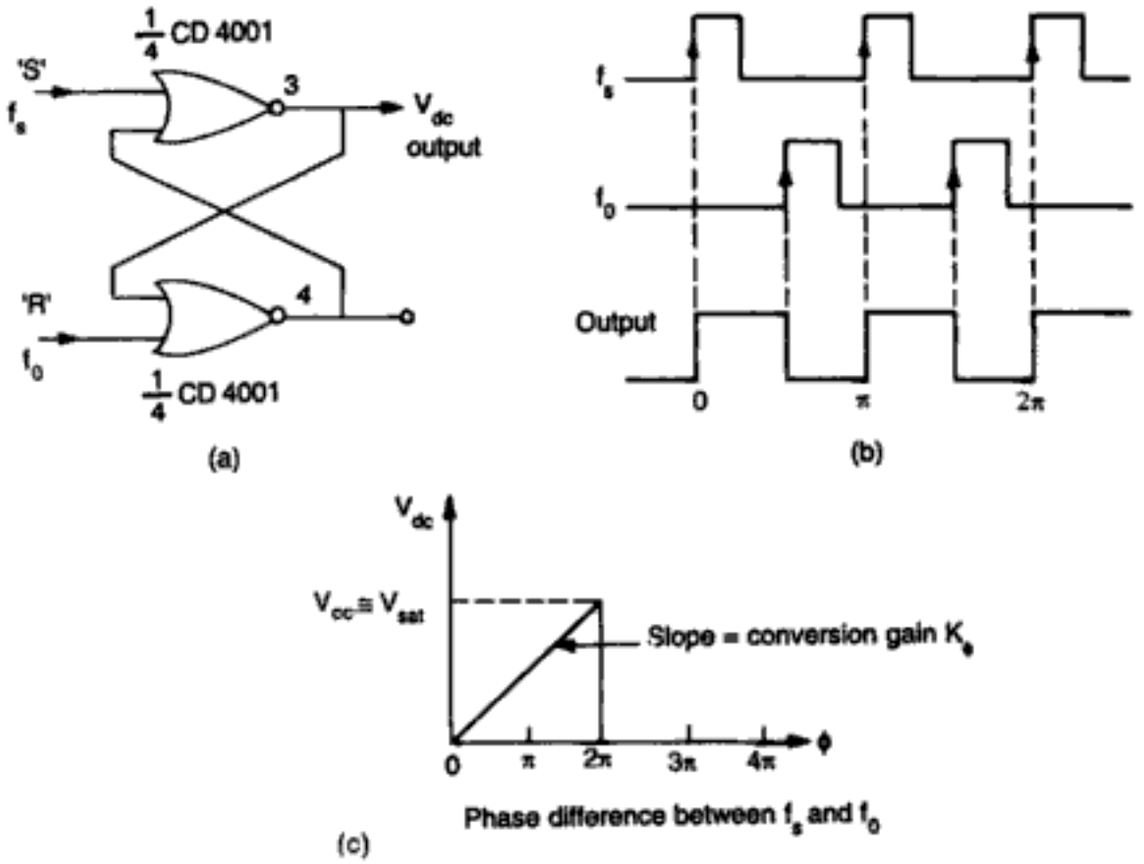

Fig. 9.6 (a) Edge-triggered phase detector using CD4001, Quad 2-input NOR gate (b) Input and output waveforms (c) dc output voltage vs phase difference ϕ

9.4 VOLTAGE CONTROLLED OSCILLATOR (VCO)

A common type of VCO available in IC form is Signetics NE/SE566. The pin configuration and basic block diagram of 566 VCO are shown in Fig. 9.7(a, b). Referring to Fig. 9.7(b), a timing capacitor C_T is linearly charged or discharged by a constant current source/sink. The amount of current can be controlled by changing the voltage v_c applied at the modulating input (pin 5) or by changing the timing resistor R_T external to IC chip. The voltage at pin 6 is held at the same voltage as pin 5. Thus, if the modulating voltage at pin 5 is increased, the voltage at pin 6 also increases, resulting in less voltage across R_T and thereby decreasing the charging current.

The voltage across the capacitor C_T is applied to the inverting input terminal of Schmitt trigger A_2 via buffer amplifier A_1. The output voltage swing of the Schmitt trigger is designed to V_{cc} and 0.5 V_{cc}. If $R_a = R_b$ in the positive feedback loop, the voltage at the non-inverting input terminal of A_2 swings from 0.5 V_{cc} to 0.25 V_{cc}. In Fig. 9.7(c), when the voltage on the capacitor C_T exceeds 0.5 V_{cc} during charging, the output of the Schmitt trigger goes LOW (0.5 V_{cc}). The capacitor now discharges and when it is at 0.25 V_{cc}, the output of Schmitt

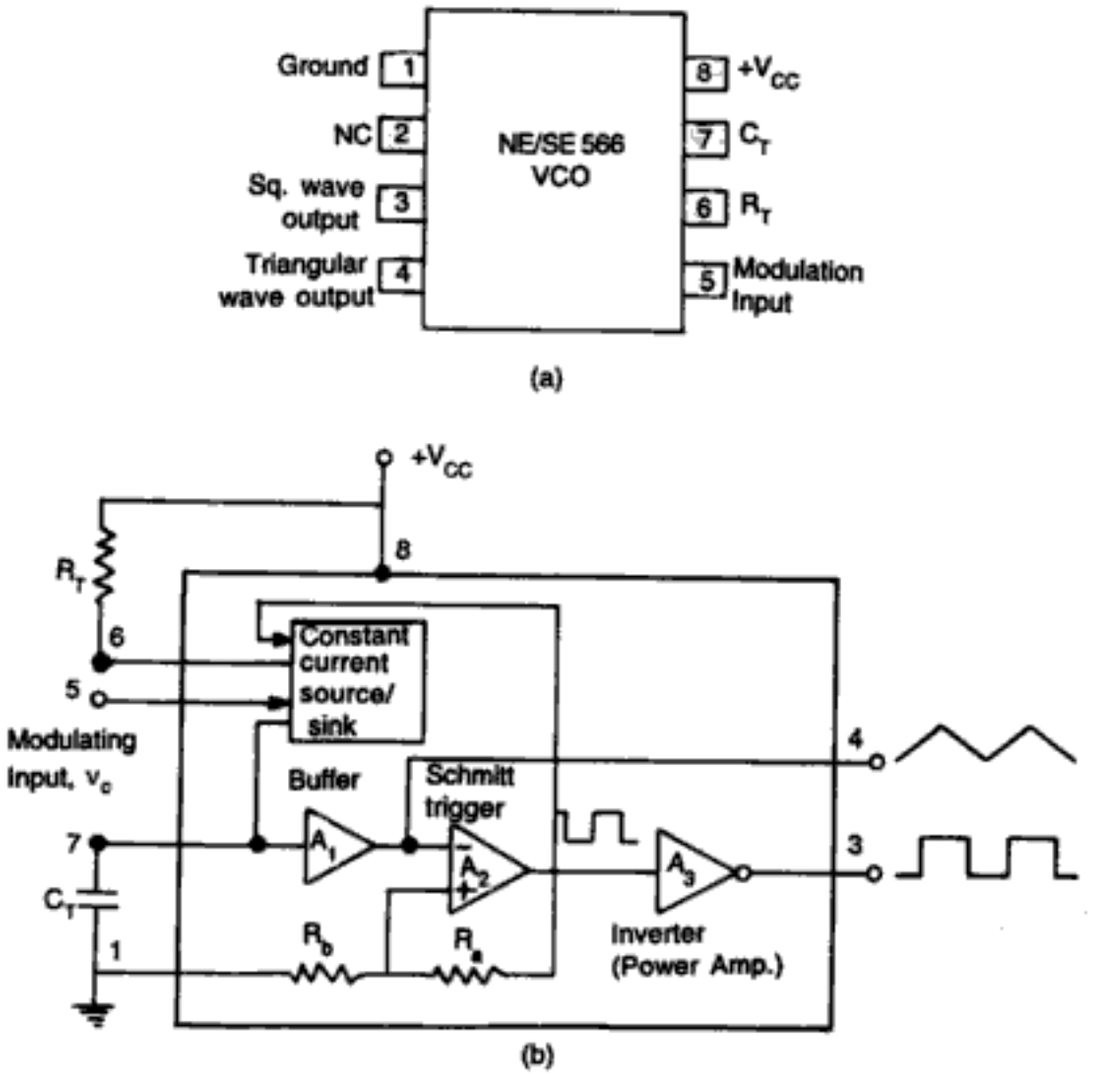

Fig. 9.7 Voltage controlled oscillator (a) Pin configuration (b) Block diagram

trigger goes HIGH (V_{cc}). Since the source and sink currents are equal, capacitor charges and discharges for the same amount of time. This gives a triangular voltage waveform across C_T which is also available at pin 4. The square wave output of the Schmitt trigger is inverted* by inverter A_3 and is available at pin 3. The output waveforms are shown in Fig. 9.7(c).

The output frequency of the VCO can be calculated as follows:

The total voltage on the capacitor changes from 0.25 V_{cc} to 0.5 V_{cc}. Thus $\Delta v = 0.25\ V_{cc}$. The capacitor chargers with a constant current source.

So
$$\frac{\Delta v}{\Delta t} = \frac{i}{C_T}$$

or,
$$\frac{0.25\,V_{cc}}{\Delta t} = \frac{i}{C_T}$$

or,
$$\Delta t = \frac{0.25\,V_{cc}C_T}{i} \qquad (9.8)$$

* An inverter is basically a current amplifier to drive the load.

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$$f_o = \frac{2(V_{cc} - (7/8)V_{cc})}{C_T R_T V_{cc}} = \frac{1}{4R_T C_T} = \frac{0.25}{R_T C_T} \tag{9.11}$$

Voltage to Frequency Conversion Factor

A parameter of importance for VCO is voltage to frequency conversion factor K_v and is defined as

$$K_v = \frac{\Delta f_0}{\Delta v_c}$$

Here Δv_c is the modulation voltage required to produce the frequency shift Δf_o for a VCO. If we assume that the original frequency is f_o and the new frequency is f_1, then

$$\Delta f_o = f_1 - f_o$$

$$= \frac{2(V_{cc} - v_c + \Delta v_c)}{C_T R_T V_{cc}} - \frac{2(V_{cc} - v_c)}{C_T R_T V_{cc}}$$

$$= \frac{2\Delta v_c}{C_T R_T V_{cc}} \tag{9.12}$$

or, $$\Delta v_c = \frac{\Delta f_o C_T R_T V_{cc}}{2} \tag{9.13}$$

Putting the value of $C_T R_T$ from Eq. (9.11)

$$\Delta v_c = \Delta f_o \, V_{cc}/8 f_o \tag{9.14}$$

or, $$K_v = \frac{\Delta f_o}{\Delta v_c} = \frac{8 f_o}{V_{cc}} \tag{9.15}$$

9.5 LOW PASS FILTER

The filter used in a PLL may be either passive type as shown in Fig. 9.8(a, b) or active type as in Fig. 9.8(c).

The low pass filter not only removes the high frequency components and noise, but also controls the dynamic characteristics of the PLL. These characteristics include capture and lock range, band-width and transient response. If filter band-width is reduced, the response time increases. However, reducing the band-width of the filter also reduces the capture range of the PLL. The filter serves one more important purpose. The charge on the filter capacitor gives a short time 'memory' to the PLL. Thus, even if the signal becomes less than the noise for a few cycles, the dc voltage on the capacitor continues to shift the frequency of the VCO till it picks up signal again. This produces a high noise immunity and locking stability.

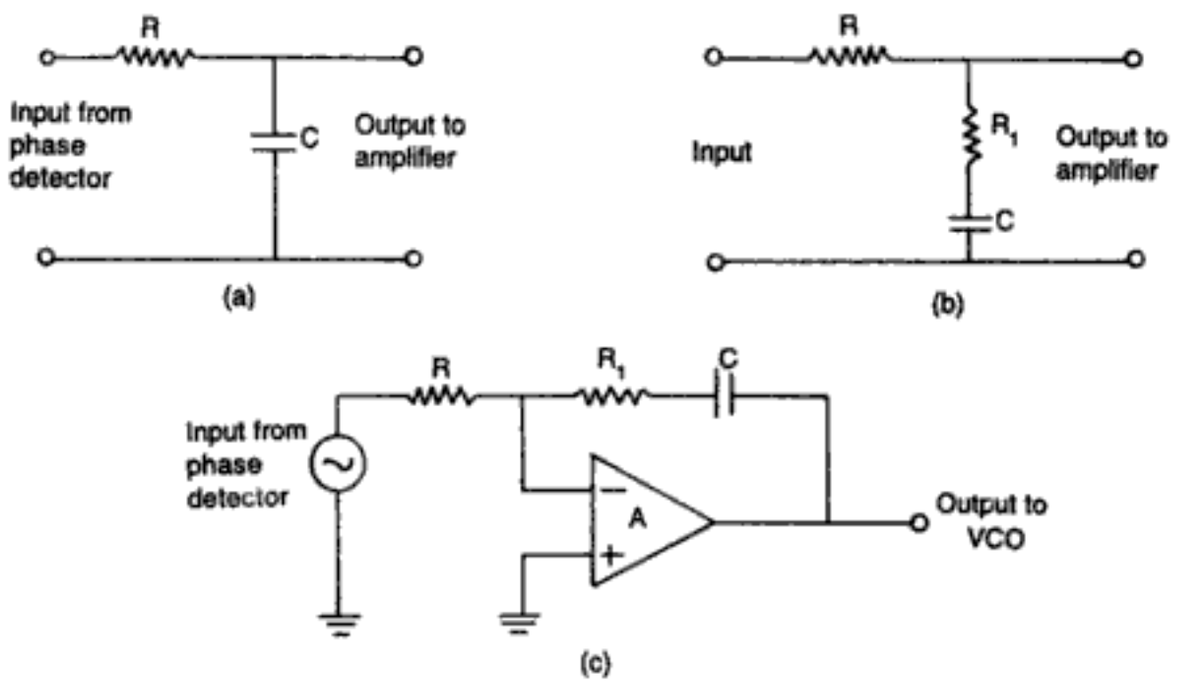

Fig. 9.8 Low pass filter (a, b) Passive filter (c) Active filter

9.6 MONOLITHIC PHASE-LOCKED LOOP

All the different building blocks of PLL are available as independent IC packages and can be externally interconnected to make a PLL. However, a number of manufacturers have introduced monolithic PLLs too. Some of the important monolithic PLLs are SE/NE560 series introduced by Signetics and LM560 series by National Semiconductor. The SE/NE 560, 561, 562, 564, 565 and 567 mainly differ in operating frequency range, power supply requirement, frequency and bandwidth adjustment ranges. Since 565 is the most commonly used PLL, we will discuss some of the important features of this IC chip.

IC PLL 565

565 is available as a 14-pin DIP package and as 10-pin metal can package. The pin configuration and the block diagram are shown in Fig. 9.9(a, b). The output frequency of the VCO (both inputs 2, 3 grounded) as given by Eq. (9.11) can be rewritten as,

$$f_o = \frac{0.25}{R_T C_T} \text{ Hz} \tag{9.16}$$

where R_T and C_T are the external resistor and capacitor connected to pin 8 and pin 9. A value between 2 kΩ and 20 kΩ is recommended for R_T. The VCO free running frequency is adjusted with R_T and C_T to be at the centre of the input frequency range. It may be seen that phase locked loop is internally broken between the VCO output and the

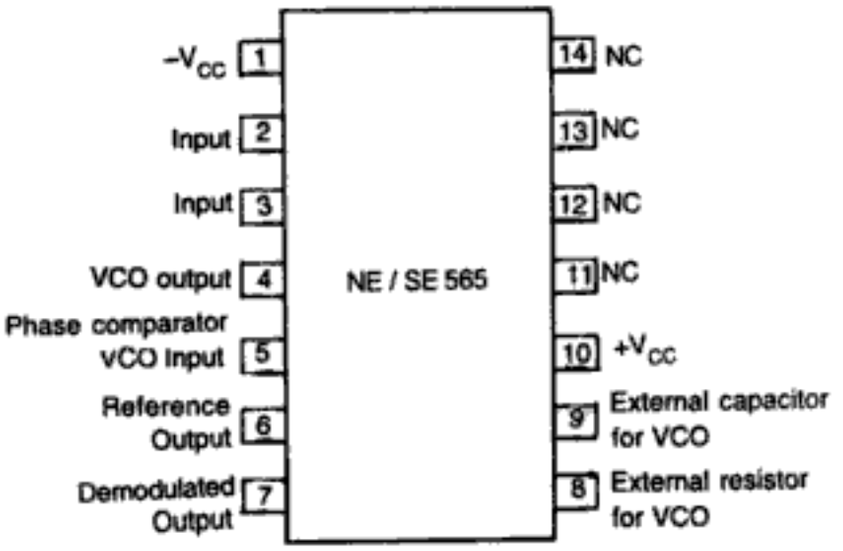

Fig. 9.9 (a) Pin diagram

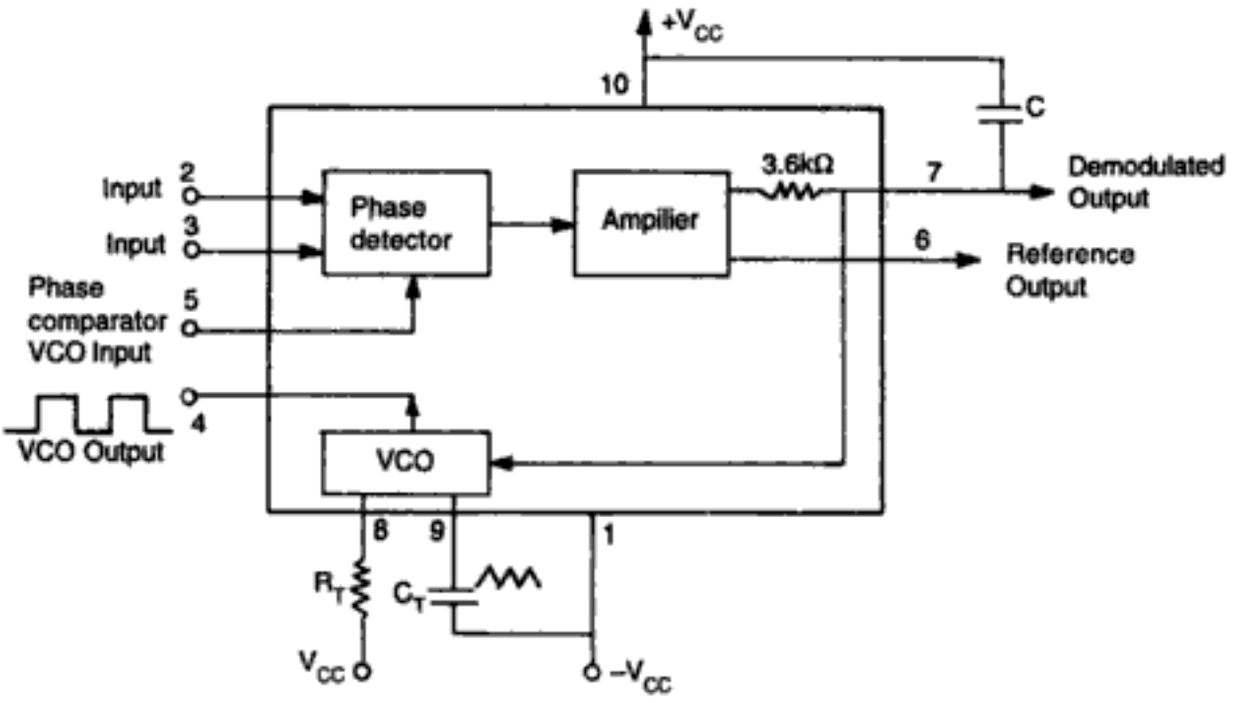

Fig. 9.9 (b) NE/SE565 PLL block diagram

phase comparator input. A short circuit between pins 4 and 5 connects the VCO output to the phase comparator so as to compare f_o with input signal f_s. A capacitor C is connected between pin 7 and pin 10 (supply terminal) to make a low pass filter with the internal resistance of 3.6 kΩ.

In Fig. 9.10, a complete diagram of LM565 (National Semiconductor) IC PLL is presented. The analog phase detector is comprised of the Q_1–Q_2, Q_3–Q_4 and Q_5–Q_6 differential amplifier pairs with Q_{37} together with R_3 (200 Ω) serving as a current sink bias source. Resistors R_1 and R_2 (each 7.2 kΩ) serve as the load for the phase detector. The output voltage of the phase detector is limited by the diode-connected transistors Q_7 and Q_8 to a maximum of ± 0.7 V which minimizes the

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$$v_c = AK_\phi(\phi - \pi/2) \tag{9.19}$$

where A is the voltage gain of the amplifier. This v_c shifts VCO frequency from its free running frequency f_o to a frequency f given by,

$$f = f_o + K_v v_c \tag{9.20}$$

where K_v is the voltage to frequency transfer coefficient of the VCO. When PLL is locked-in to signal frequency f_s, then we have

$$f = f_s = f_o + K_v v_c \tag{9.21}$$

since, $$v_c = (f_s - f_o)/K_v = A K_\phi (\phi - \pi/2) \tag{9.22}$$

Thus, $$\phi = \pi/2 + (f_s - f_o)/K_v K_\phi A \tag{9.23}$$

The maximum output voltage magnitude available from the phase detector occurs for $\phi = \pi$ and 0 radian (see in Fig. 9.4(c) and v_e (max) $= \pm K_\phi \pi/2$ from Eq. (9.6). The corresponding value of the maximum control voltage available to drive the VCO will be,

$$v_{c(max)} = \pm (\pi/2)\ K_\phi A \tag{9.24}$$

The maximum VCO frequency swing that can be obtained is given by,

$$(f - f_o)_{max} = K_v v_{c(max)} = K_v K_\phi A\ (\pi/2) \tag{9.25}$$

Therefore, the maximum range of signal frequencies over which the PLL can remain locked will be,

$$\begin{aligned} f_s &= f_o \pm (f - f_o)_{max} \\ &= f_o \pm K_v K_\phi\ (\pi/2) A = f_o \pm \Delta f_L \end{aligned} \tag{9.26}$$

where $2\ \Delta f_L$ will be the lock-in frequency range and is given by,

lock-in range = $$2\ \Delta f_L = K_v K_\phi A\ \pi \tag{9.27}$$

or, $$\Delta f_L = \pm\ K_v K_\phi A\ (\pi/2) \tag{9.28}$$

The lock-in range is symmetrically located with respect to VCO free running frequency f_o. For IC PLL 565,

$$K_v = \frac{8 f_o}{V} \quad \text{(from Eq. (9.15))}$$

where $$V = +V_{cc} - (-V_{cc})$$

Again, $$K_\phi = \frac{1.4}{\pi} \quad \text{(from Eq. (9.17))}$$

and $$A = 1.4$$

Hence the lock-in range from Eq. (9.28) becomes,

$$\Delta f_L = \pm\ 7.8\ f_o/V \tag{9.29}$$

Derivation of Capture Range

When PLL is not initially locked to the signal, the frequency of the VCO will be free running frequency f_o. The phase angle difference between the signal and the VCO output voltage will be,

$$\phi = (\omega_s t + \theta_s) - (\omega_o t + \theta_o) = (\omega_s - \omega_o)t + \Delta\theta \tag{9.30}$$

thus the phase angle difference does not remain constant but will change with time at a rate given by

$$\frac{d\phi}{dt} = \omega_s - \omega_o \tag{9.31}$$

The phase detector output voltage will therefore not have a dc component but will produce an ac voltage with a triangular waveform of peak amplitude $K_\phi(\pi/2)$ and a fundamental frequency $(f_s - f_o) = \Delta_f$.

The low pass filter (LPF) is a simple RC network having transfer function

$$T(jf) = \frac{1}{1 + j(f/f_1)} \tag{9.32}$$

where $f_1 = 1/2\,\pi\,RC$ is the 3-dB point of LPF. In the slope portion of LPF where $(f/f_1)^2 >> 1$, then

$$T(f) \simeq \frac{f_1}{jf} \tag{9.33}$$

The fundamental frequency term supplied to the LPF by the phase detector will be the difference frequency $\Delta f = f_s - f_o$. If $\Delta f > 3f_1$, the LPF transfer function will be approximately,

$$T(\Delta f) \simeq f_1/\Delta f = f_1/(f_s - f_o) \tag{9.34}$$

The voltage v_c to drive the VCO is,

$$v_c = v_e \times T(f) \times A \tag{9.35}$$

or,
$$v_{c(max)} = v_{e(max)} \times T(f) \times A$$
$$= \pm K_\phi(\pi/2)A\,(f_1/\Delta f). \text{ (from Eq. (9.24))} \tag{9.36}$$

Then the corresponding value of the maximum VCO frequency shift is,

$$(f - f_o)_{max} = K_v\, v_{c(max)} = \pm K_v K_\phi(\pi/2)A\,(f_1/\Delta f) \tag{9.37}$$

For the acquisition of signal frequency, we should put $f = f_s$ so that the maximum signal frequency range that can be acquired by PLL is,

$$(f_s - f_o)_{max} = \pm K_v K_\phi(\pi/2)A\,(f_1/\Delta f_c) \tag{9.38}$$

Now
$$\Delta f_c = (f_s - f_o)_{max}$$

so,
$$(\Delta f_c)^2 = K_v K_\phi(\pi/2)Af_1 \text{ (from Eq. (9.38))}$$

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The output of VCO which has the same frequency as the carrier, but unmodulated is fed to the multiplier. Since VCO output is always 90° out of phase with the incoming AM signal under the locked condition, the AM input signal is also shifted in phase by 90° before being fed to the multiplier. This makes both the signals applied to the multiplier in same phase. The output of the multiplier contains both the sum and the difference signals, the demodulated output is obtained after filtering high frequency components by the LPF. Since the PLL responds only to the carrier frequencies which are very close to the VCO output, a PLL AM detector exhibits a high degree of selectivity and noise immunity which is not possible with conventional peak detector type AM modulators.

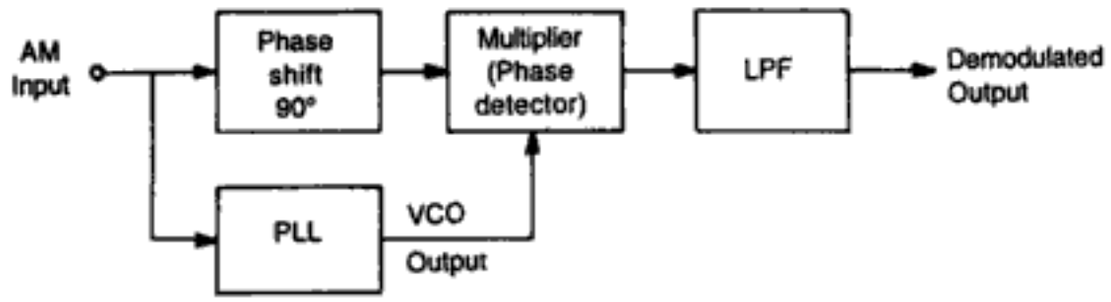

Fig. 9.14 PLL used as AM demodulator

9.7.4 FM Demodulation

If PLL is locked to a FM signal, the VCO tracks the instantaneous frequency of the input signal. The filtered error voltage which controls the VCO and maintains lock with the input signal is the demodulated FM output. The VCO transfer characteristics determine the linearity of the demodulated output. Since, VCO used in IC PLL is highly linear, it is possible to realize highly linear FM demodulators.

9.7.5 Frequency Shift Keying (FSK) Demodulator

In digital data communication and computer peripheral, binary data is transmitted by means of a carrier frequency which is shifted between two preset frequencies. This type of data transmission is called frequency shift keying (FSK) technique. The binary data can be retrieved using a FSK demodulator at the receiving end. The 565 PLL is very useful as a FSK demodulator. Figure 9.15 shows FSK demodulator using PLL for tele-typewriter signals of 1070 Hz and 1270 Hz. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding dc shift at the output. A three stage filter removes the carrier component and the output signal is made logic compatible by a voltage comparator.

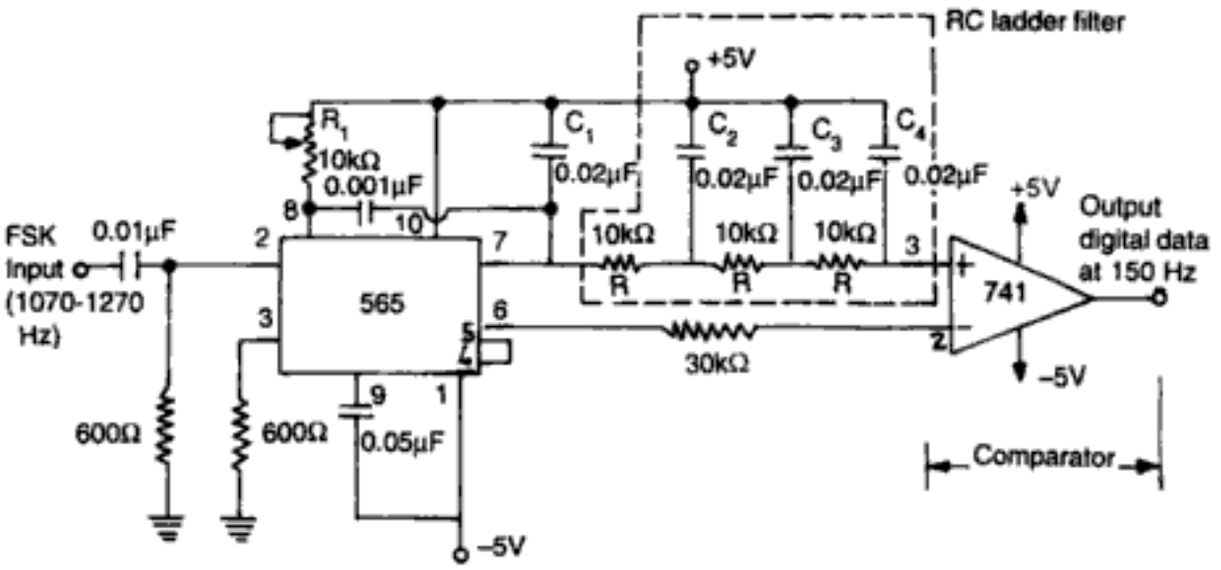

Fig. 9.15 FSK demodulator

Summary

1. A phase locked loop consists of a phase detector, low pass filter, amplifier and a VCO in feedback loop.
2. The important characteristics of a PLL are: lock-in range, capture range and pull-in-time.
3. The lock range is usually greater than the capture range. The capture range depends upon the LPF characteristics.
4. The phase detectors are of two types: analog and digital. The phase detector is basically a multiplier.
5. The frequency of VCO can be set by an external capacitor and resistor. The output frequency f_0 of VCO is compared with the incoming signal f_s. When $f_0 = f_s$ the PLL is said to be locked.
6. The low pass filter may be passive or active type. The LPF controls the capture range and lock range of PLL.
7. Signetics SE/NE 560 series – 560, 561, 562, 564, 565 and 567 are monolithic PLLs. All the blocks of a PLL are also available as independent ICs and can be interconnected to make a PLL.
8. The PLLs are used as frequency multiplier, divider, AM and FM demodulator, FSK demodulator etc.

Review Questions

9.1. List the basic building blocks of a PLL.
9.2. Define capture range, lock range and pull-in-time.
9.3. Which is greater 'Capture range' or 'Lock range'?
9.4. What is the major difference between digital and analog PLLs?
9.5. Give the block diagram of IC 566 VCO and explain its operation.
9.6. What is the range of modulating input voltage applied to a VCO?
9.7. List the applications of PLL.
9.8. Draw the circuit of a PLL AM detector and explain its operation.

PROBLEMS

9.1. In the VCO of Fig. 9.7 calculate the change in output frequency if the supply voltage is varied between 9V and 11V. Assume V_{cc} = 12V, R_T = 6.8 kΩ, C_T = 75 pF, R_1 = 15 kΩ and R_2 = 100 kΩ.

9.2. Determine the dc control voltage v_c at lock if signal frequency f_s = 10 kHz, VCO free running frequency is 10.66 kHz and the voltage to frequency transfer coefficient of VCO is 6600 Hz/V.

9.3. If f_s = 100 kHz, the voltage to frequency transfer coefficient of VCO, K_v = 2 MHz/V, f_o the VCO frequency is 5 MHz and N = 100 in the frequency multiplier of Fig. 9.12, what is the dc control voltage at lock?

9.4. Calculate output frequency f_o, lock range Δf_L and capture range Δf_c of a 565 PLL if R_T = 10 kΩ, C_T = 0.01 μF and C = 10 μF.

9.5. Repeat Problems 9.4 for C_T = 470 pF.

Experiment

(a) To study the operation of NE 565 PLL.
(b) To use NE 565 as a multiplier.

Procedure

1. Make connections of the PLL as shown in Fig. E. 9.1 (a).
2. Measure the free running frequency of VCO at pin 4, with the input signal V_{in} set equal to zero. Compare it with the calculated value = $0.25/R_TC_T$.
3. Now apply the input signal of 1 V_{pp} square wave at a 1 kHz to pin 2. Connect one channel of the scope to pin 2 and display this signal on the scope.

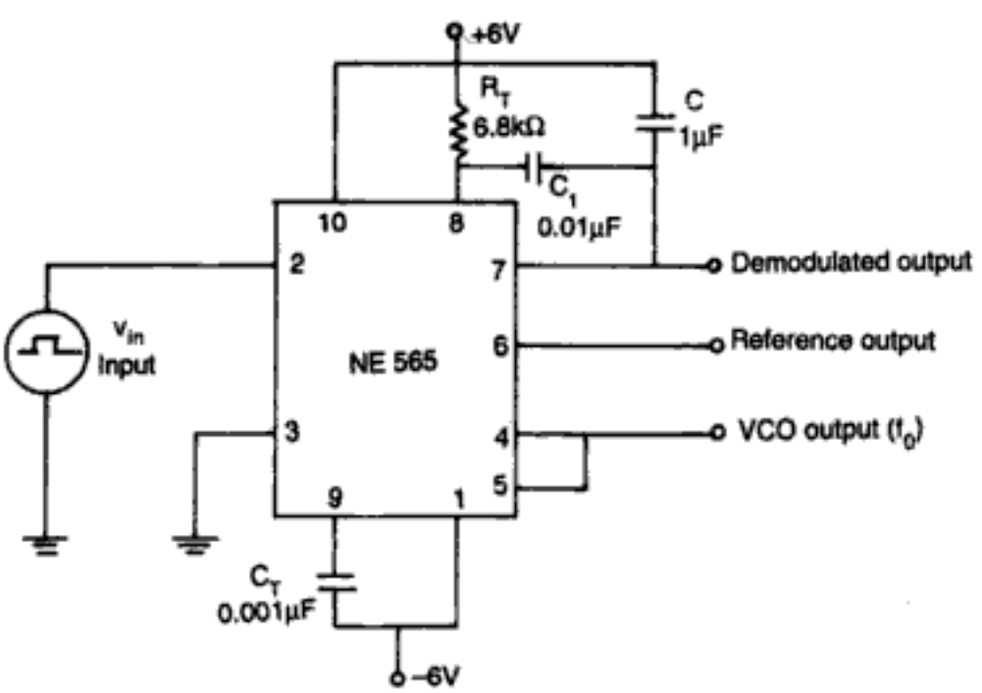

Fig. E. 9.1 (a) NE565 PLL connection diagram

4. Gradually increase the input frequency till the PLL is locked to the input frequency. This frequency f_1 gives the lower end of the capture range. Go on increasing the input frequency, till PLL tracks the input signal, say, to a frequency f_2. This frequency f_2 gives the upper end of the lock range. If input frequency is increased further, the loop will get unlocked.
5. Now gradually decrease the input frequency till the PLL is again locked. This is the frequency f_3, the upper end of the capture range. Keep on decreasing the input frequency until the loop is unlocked. This frequency f_4 gives the lower end of the lock range.
6. The lock range $\Delta f_L = (f_2 - f_4)$. Compare it with the calculated value of $\frac{\pm 7.8 f_0}{12}$. Also the capture range is $\Delta f_c = (f_3 - f_1)$. Compare it with the calculated value of capture range.

$$\Delta f_c = \pm \left[\frac{\Delta f_L}{(2\pi)(3.6)(10^3) \times C} \right]^{\frac{1}{2}}$$

7. To use PLL as a multiplier, make connections as shown in Fig. E. 9.1(b). The circuit uses a 4-bit binary counter 7490 used as a divide-by-5 circuit.

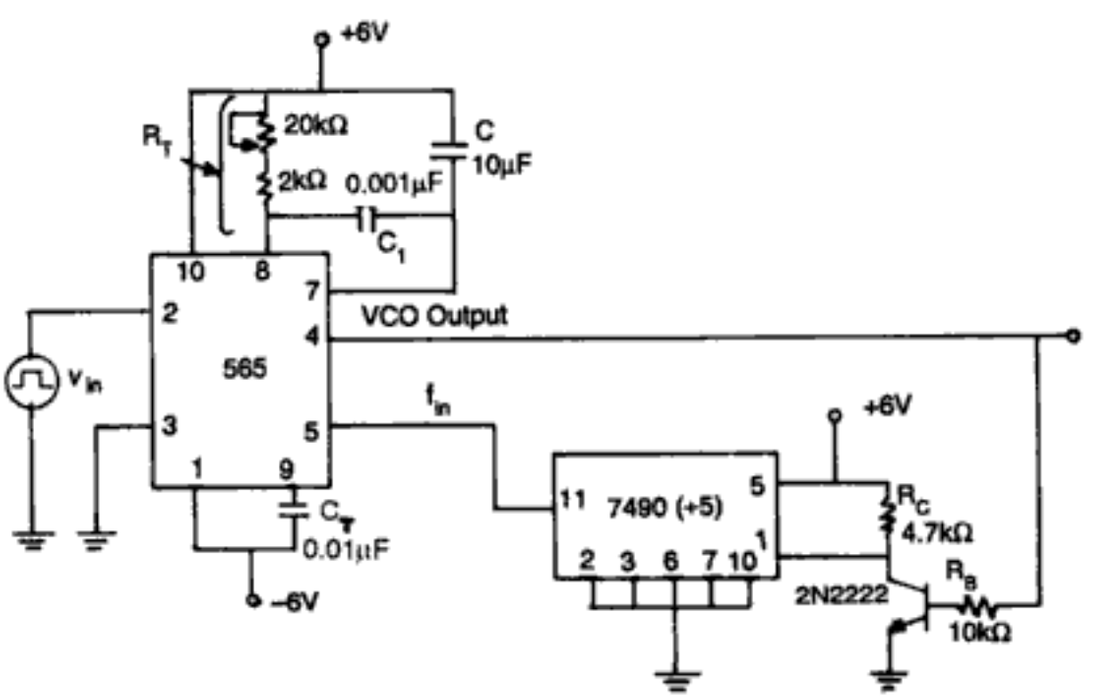

Fig. E. 9.1 (b) NE 565 as a frequency multiplier

8. Set the input signal at 1 V_{pp} square wave at 500 Hz.
9. Vary the VCO frequency by adjusting the 20 kΩ potentiometer till the PLL is locked. Measure the output frequency. It should be 5 times the input frequency.
10. Repeat steps 8, 9 for input frequency of 1 kHz and 1.5 kHz.

10

D-A And A-D Converters

10.1 INTRODUCTION

Most of the real-world physical quantities such as voltage, current, temperature, pressure and time etc. are available in analog form. Even though an analog signal represents a real physical parameter with accuracy, it is difficult to process, store or transmit the analog signal without introducing considerable error because of the superimposition of noise as in the case of amplitude modulation. Therefore, for processing, transmission and storage purposes, it is often convenient to express these variable in digital form. It gives better accuracy and reduces noise. The operation of any digital communication system is based upon analog to digital (A/D) and digital to analog (D/A) conversion.

Figure 10.1 highlights a typical application within which A/D and D/A conversion is used. The analog signal obtained from the transducer is band limited by antialiasing filter. The signal is then sampled at a frequency rate more than twice the maximum frequency of the band limited signal. The sampled signal has to be held constant while conversion is taking place in A/D converter. This requires that ADC should be preceded by a sample and hold (S/H) circuit. The ADC output is a sequence in binary digit. The micro-computer or digital signal processor performs the numerical calculations of the desired control algorithm. The D/A converter is to convert digital signal into analog and hence the function of DAC is exactly opposite to that of ADC. The D/A converter is usually operated at the same frequency as the ADC. The output of a D/A converter is commonly a staircase. This staircase-like digital output is passed through a smoothing filter to reduce the effect of quantization noise.

The scheme given in Fig. 10.1 is used either in full or in part in applications such as digital audio recording and playback, computer, music and video synthesis, pulse code modulation transmission, data

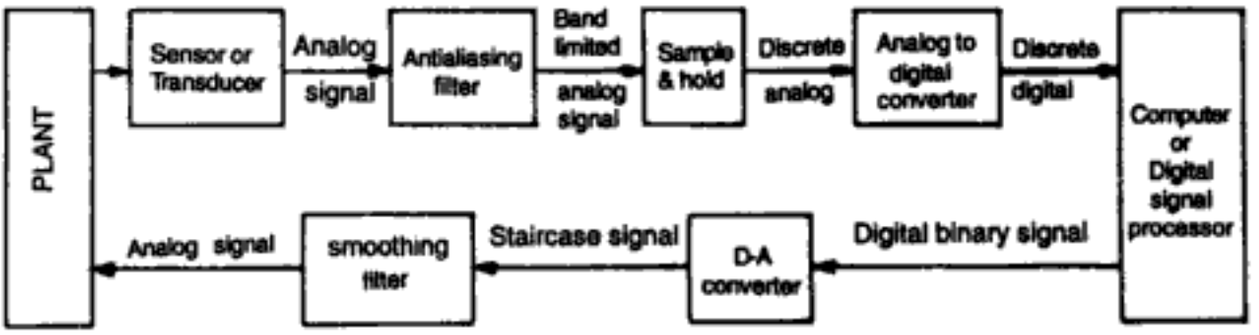

Fig. 10.1 Circuit showing application of A/D and D/A converter

acquisition, digital multimeter, direct digital control, digital signal processing, microprocessor based instrumentation.

Both ADC and DAC are also known as data converters and are available in IC form. It may be mentioned here that for slowly varying signal, sometimes sample and hold circuit may be avoided without considerable error. The A-D conversion usually makes use of a D-A converter so we shall first discuss DAC followed by ADC.

10.2 BASIC DAC TECHNIQUES

The schematic of a DAC is shown in Fig. 10.2. The input is an n-bit binary word D and is combined with a reference voltage V_R to give an analog output signal. The output of a DAC can be either a voltage or current. For a voltage output DAC, the D/A converter is mathematically described as

$$V_o = K\ V_{FS}\ (d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n}) \qquad (10.1)$$

where, V_o = output voltage

V_{FS} = full scale output voltage

K = scaling factor usually adjusted to unity

$d_1 d_2 \ldots d_n$ = n-bit binary fractional word with the decimal point located at the left

d_1 = most significant bit (MSB) with a weight of $V_{FS}/2$

d_n = least significant bit (LSB) with a weight of $V_{FS}/2^n$

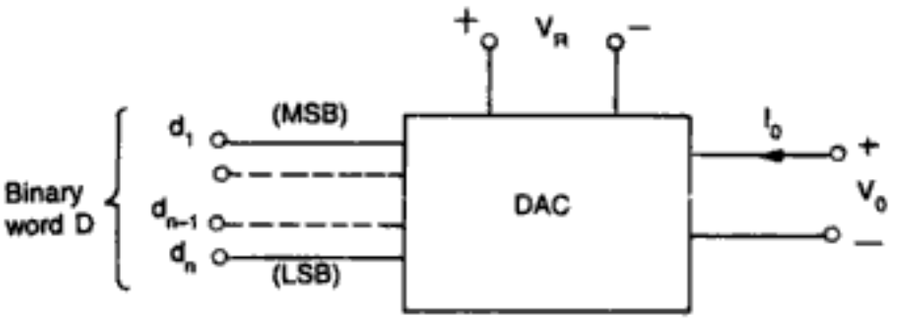

Fig. 10.2 Schematic of a DAC

There are various ways to implement Eq. (10.1) Here we shall discuss the following resistive techniques only:

Weighted resistor DAC
R-2R ladder
Inverted R-2R ladder

10.2.1 Weighted Resistor DAC

One of the simplest circuits shown in Fig. 10.3(a) uses a summing amplifier with a binary weighted resistor network. It has n-electronic switches $d_1, d_2, \ldots, d_n$ controlled by binary input word. These switches are single pole double throw (SPDT) type. If the binary input to a particular switch is 1, it connects the resistance to the reference voltage ($-V_R$). And if the input bit is 0, the switch connects the resistor to the ground. From Fig. 10.3(a), the output current I_o for an ideal op-amp can be written as

$$I_o = I_1 + I_2 + \ldots + I_n$$

$$= \frac{V_R}{2R} d_1 + \frac{V_R}{2^2 R} d_2 + \ldots + \frac{V_R}{2^n R} d_n$$

$$= \frac{V_R}{R} (d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n})$$

The output voltage

$$V_o = I_o R_f = V_R \frac{R_f}{R} (d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n}) \qquad (10.2)$$

Comparing Eq. (10.1) with Eq. (10.2) it can be seen that if $R_f = R$ then $K = 1$ and $V_{FS} = V_R$.

The circuit shown in Fig. 10.3(a) uses a negative reference voltage. The analog output voltage is therefore positive staircase as shown in Fig. 10.3(b) for a 3-bit weighted resistor DAC. It may be noted that

(i) Although the op-amp in Fig. 10.3(a) is connected in inverting mode, it can also be connected in non-inverting mode.
(ii) The op-amp is simply working as a current to voltage converter.
(iii) The polarity of the reference voltage is chosen in accordance with the type of the switch used. For example, for TTL compatible switches, the reference voltage should be + 5 V and the output will be negative.

The accuracy and stability of a DAC depends upon the accuracy of the resistors and the tracking of each other with temperature. There are however a number of problems associated with this type of DAC. One of the disadvantages of binary weighted type DAC is the wide range of resistor values required. It may be observed that for better resolution, the input binary word length has to be increased. Thus, as

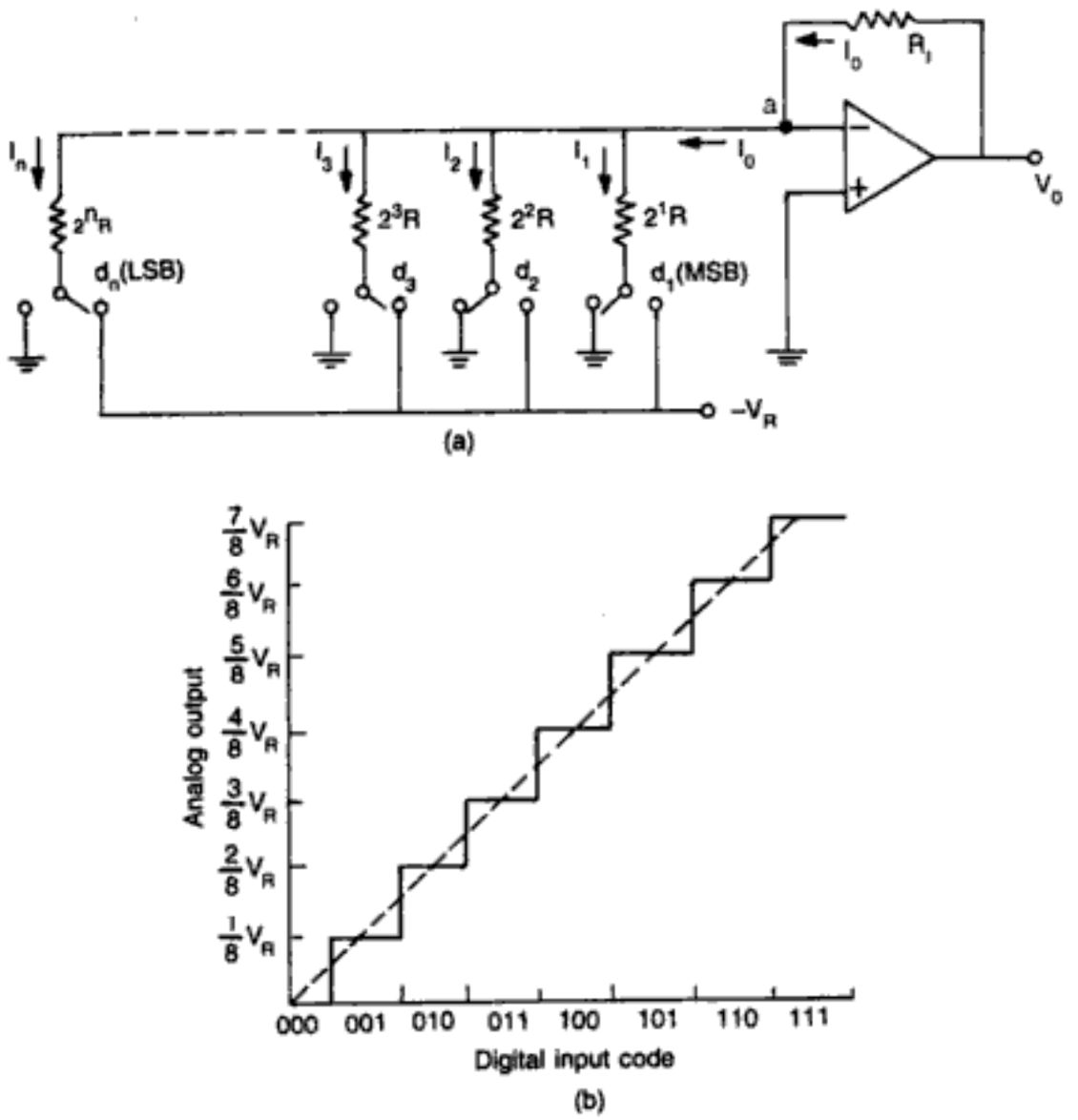

Fig. 10.3 (a) A simple weighted resistor DAC (b) Transfer characteristics of a 3-bit DAC

the number of bit increases, the range of resistance value increases. For 8-bit DAC, the resistors required are 2^0R, 2^1R, 2^2R, ..., 2^7R. The largest resistor is 128 times the smallest one for only 8-bit DAC. For a 12-bit DAC, the largest resistance required is 5.12 MΩ if the smallest is 2.5 kΩ. The fabrication of such a large resistance in IC is not practical. Also the voltage drop across such a large resistor due to the bias current would also affect the accuracy. The choice of smallest resistor value as 2.5 kΩ is reasonable; otherwise loading effect will be there. The difficulty of achieving and maintaining accurate ratios over such a wide range especially in monolithic form restricts the use of weighted resistor DACs to below 8-bits.

The switches in Fig. 10.3 (a) are in series with resistors and therefore, their ***on*** resistance must be very low and they should have zero offset voltage. Bipolar transistors do not perform well as voltage switches, due to the inherent offset voltage when in saturation. However, by using MOSFET, this can be achieved.

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10.2.2 R-2R Ladder DAC

Wide range of resistors are required in binary weighted resistor type DAC. This can be avoided by using R-2R ladder type DAC where only two values of resistors are required. It is well suited for integrated circuit realization. The typical value of R ranges from 2.5 kΩ to 10 kΩ.

For simplicity, consider a 3-bit DAC as shown in Fig. 10.5 (a), where the switch position $d_1\, d_2\, d_3$ corresponds to the binary word 100. The circuit can be simplified to the equivalent form of Fig. 10.5 (b) and finally to Fig. 10.5 (c). Then, voltage at node C can be easily calculated by the set procedure of network analysis as

$$\frac{-V_R\left(\frac{2}{3}R\right)}{2R+\frac{2}{3}R} = -\frac{V_R}{4}$$

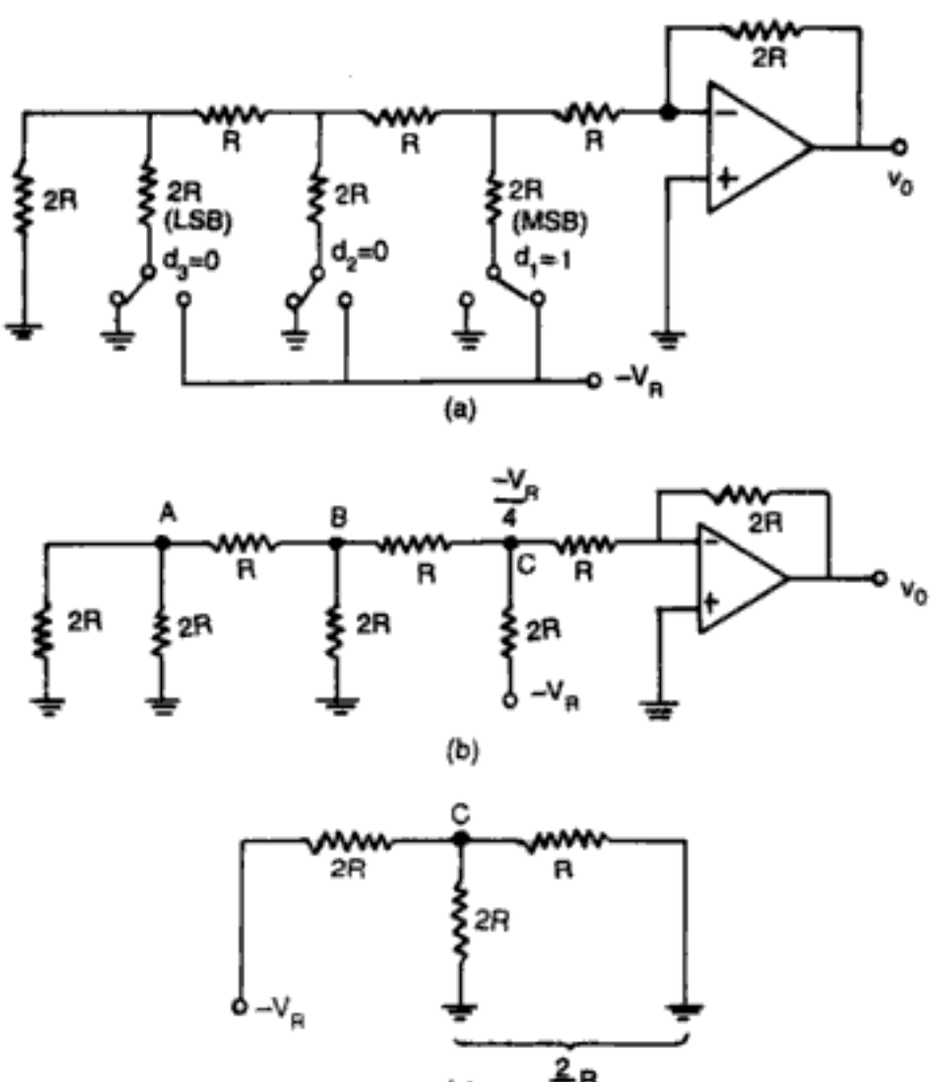

Fig. 10.5 (a) R-2R ladder DAC (b) Equivalent circuit of (a), (c) Equivalent circuit of (b)

The output voltage

$$V_o = \frac{-2R}{R}\left(-\frac{V_R}{4}\right) = \frac{V_R}{2} = \frac{V_{FS}}{2}$$

The switch position corresponding to the binary word 001 in 3 bit DAC is shown in Fig. 10.6 (a). The circuit can be simplified to the equivalent form of Fig. 10.6 (b). The voltages at the nodes (A, B, C) formed by resistor branches are easily calculated in a similar fashion and the output voltage becomes

$$V_o = \left(-\frac{2R}{R}\right)\left(-\frac{V_R}{16}\right) = \frac{V_R}{8} = \frac{V_{FS}}{8}$$

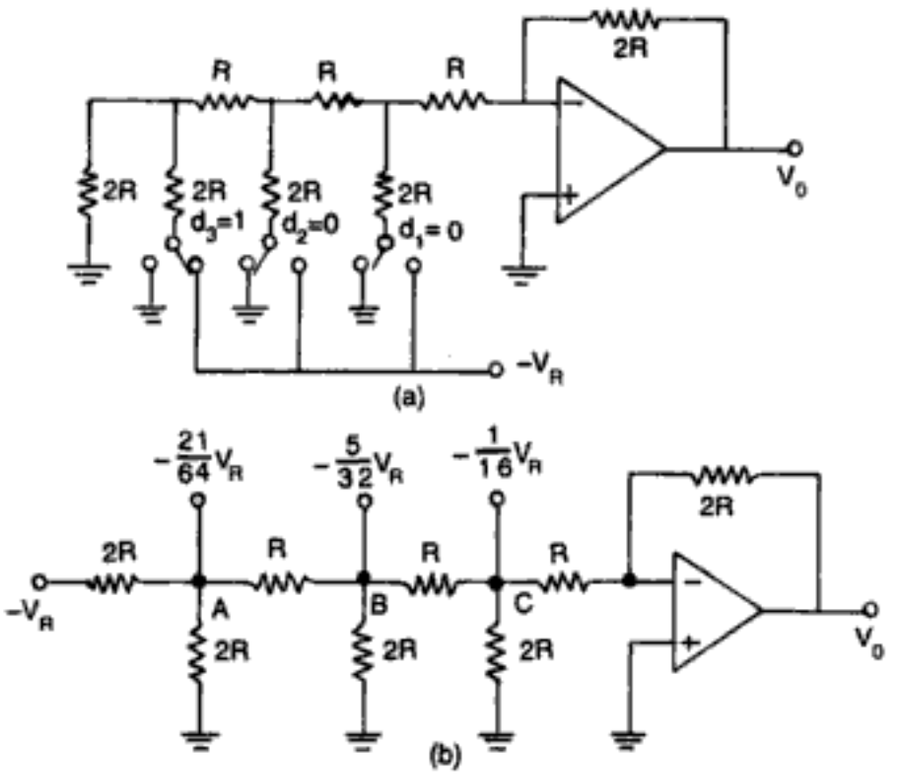

Fig. 10.6 (a) R-2R ladder DAC for switch positions 001 (b) Equivalent circuit

In a similar fashion, the output voltage for R-2R ladder type DAC corresponding to other 3-bit binary words can be calculated.

10.2.3 Inverted R-2R Ladder

In weighted resistor type DAC and R-2R ladder type DAC, current flowing in the resistors changes as the input data changes. More power dissipation causes heating, which in turn, creates non-linearity in DAC. This is a serious problem and can be avoided completely in 'Inverted R-2R ladder type DAC'. A 3-bit Inverted R-2R ladder type DAC is shown in Fig. 10.7 (a) where the position of MSB and LSB is interchanged. Here each input binary word connects the corresponding switch either to ground or to the inverting input terminal of the op-amp which is also at virtual ground. Since both the terminals of

switches d_i are at ground potential, current flowing in the resistances is constant and independent of switch position, i.e. independent of input binary word. In Fig. 10.7 (a), when switch d_i is at logical '0' i.e., to the left, the current through 2R resistor flows to the ground and when the switch d_i is at logical '1' i.e., to the right, the current through 2R sinks to the virtual ground. The circuit has the important property that the currents divides equally at each of the nodes. This is because the equivalent resistance to the right or to the left of any node is exactly 2 R. The division of the current is shown in Fig. 10.7 (b). Consider a reference current of 2 mA. Just to the right of node *A*, the equivalent resistor is 2 R. Thus 2 mA of reference input current divides equally to value 1 mA at node *A*. Similarly to the right of node *B*, the equivalent resistor is 2 R. Thus 1 mA of current further divides to value 0.5 mA at node *B*. Similarly, current divides equally at node *C* to 0.25 mA. The equal division of current in successive nodes remains the same in the 'inverted R-2R ladder' irrespective of the input binary word. Thus the currents remain constant in each branch of the ladder. Since constant current implies constant voltage, the ladder node voltages remain constant at $V_R/2^0$, $V_R/2^1$, $V_R/2^2$. The circuit works on the principle of summing currents and is also said to operate in the current mode. The most important advantage of the current mode or inverted ladder is that since the ladder node voltages remain constant even with changing input binary words (codes), the stray capacitances are not able to produce slow-down effects on the performance of the circuit.

It may be noted that the switches used in Fig. 10.7(a) are the SPDT switches discussed earlier. According to bit d_i, the corresponding switch gets connected either to ground for $d_i = 0$ or to $-V_R$ for $d_i = 1$. The current flows from inverting input terminal to $-V_R$ for $d_i = 1$ and from ground to $-V_R$ for $d_i = 0$. Regardless of the binary input word, the current in the resistive branches of the inverted ladder circuit remains always constant as explained in Fig. 10.7(b). However, the current through the feedback resistor R is the summing current depending upon the input binary word. It may further be mentioned that, Fig. 10.7 (b) shows only the current division for making the analysis simple, though it is a voltage driven DAC.

10.2.4 Multiplying DACs

A digital to analog converter which uses a varying reference voltage V_R is called a multiplying D/A converter (MDAC). Thus if in the Eq. (10.1), the reference voltage v_R is a sine wave given by

$$v_R(t) = V_{im} \cos 2\pi ft$$

Then, $$v_0(t) = V_{om} \cos (2\pi f t + 180°)$$

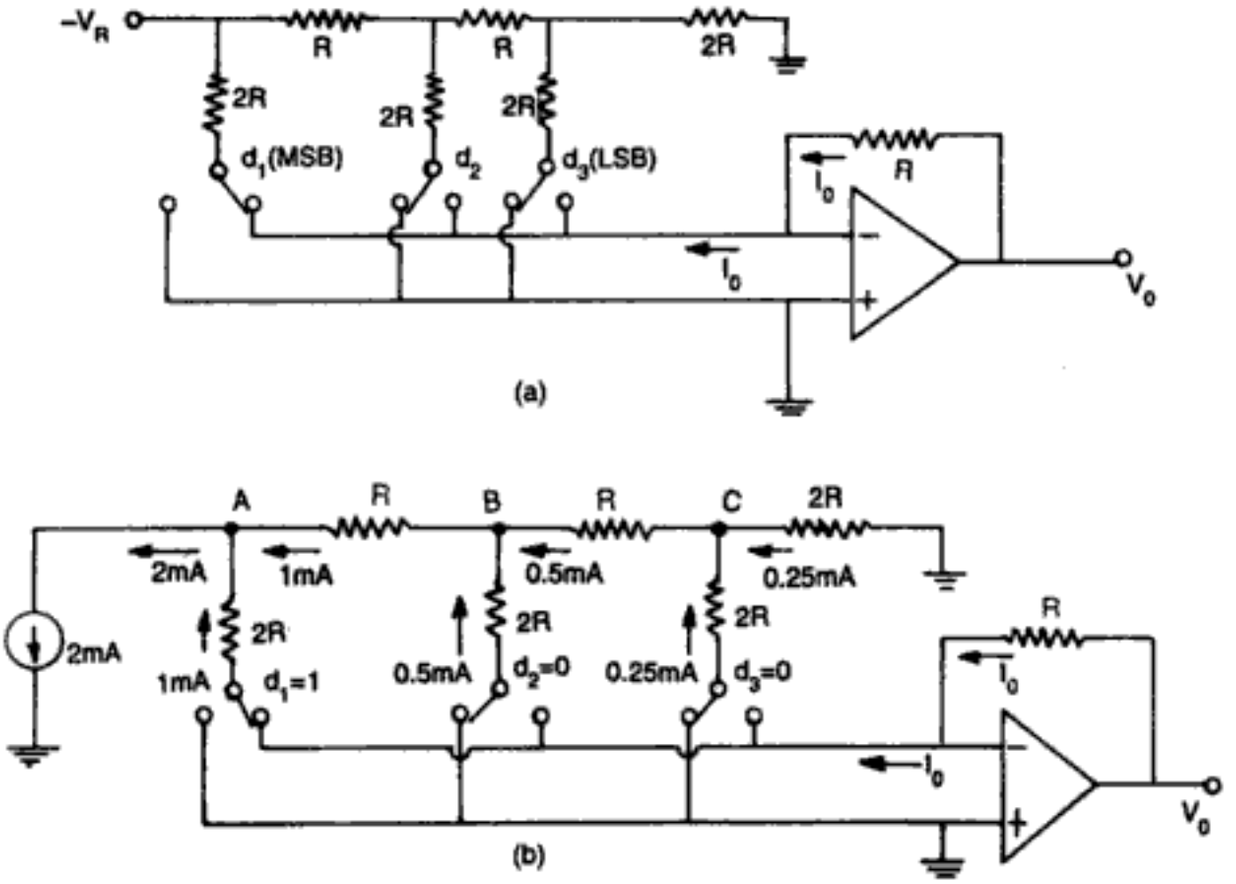

Fig. 10.7 (a) Inverted R-2R ladder DAC (b) Inverted R-2R ladder DAC showing division of current for digital input word 001

where V_{om} will vary from 0V to $(1-2^{-n})\ V_{im}$ depending upon the input code. When used like this, MDAC behaves as a digitally controlled audio attenuator because the output V_0 is a fraction of the voltage representing the input digital code and the attenuator setting can be controlled by digital logic. If followed by an op-amp integrator, the MDAC provides digitally programmable integration which can be used in the design of digitally programmable oscillators, filters.

10.2.5 Monolithic DAC

Monolithic DACs consisting of R-2R ladder, switches and the feedback resistor are available for 8, 10, 12, 14 and 16 bit resolution from various manufacturers. The MC 1408L is a 8-bit DAC with a current output. The SE/NE 5018 is also a 8-bit DAC but with a voltage output. There are hybrid D/A converters available in DATEL DAC-HZ series for current as well as voltage output.

A typical 8-bit DAC 1408 compatible with TTL and CMOS logic with settling time around 300 ns is shown in Fig. 10.8 (a). It has eight input data lines d_1 (MSB) through d_8 (LSB). It requires 2 mA reference current for full scale input and two power supplies V_{cc} = + 5 V and V_{EE} – 5 V (V_{EE} can range from – 5 V to –15 V). The total reference current

source is determined by resistor R_{14} and voltage reference V_R and is equal to $V_R/R_{14} = 5V/2.5\ k\Omega = 2\ mA$. The resistor $R_{15} = R_{14}$ match the input impedance of the reference source. The output current I_o is calculated as

$$I_o = \frac{V_R}{R_{14}} \left(\sum_{i=1}^{8} d_i\, 2^{-i} \right); d_i = 0 \text{ or } 1$$

For full scale input (i.e. d_8 through $d_1 = 1$)

$$I_o = \frac{5\,V}{2.5\ k\Omega} \left(\sum_{i=1}^{8} 1 \times 2^{-i} \right) = 2\ mA\ (255/256) = 1.992\ mA$$

The output is 1 LSB less than the full scale reference current of 2 mA. So, the output voltage V_o for the full scale input is

$$V_o = 2\ mA\ (255/256) \times 5\ k\Omega = 9.961\ V$$

In general the output voltage V_o is given by

$$V_o = \frac{V_R}{R_{14}} R_f \left[\frac{d_1}{2} + \frac{d_2}{4} + \frac{d_3}{8} + \ldots + \frac{d_8}{256} \right]$$

The 1408 DAC can be calibrated for bipolar range from $-5\,V$ to $+5\,V$ by adding resistor R_B (5 kΩ) between V_R and output pin 4 as shown in Fig. 10.8 (b). The resistor R_B supplies 1 mA ($= V_R/R_B$) current to the output in the opposite direction of the current generated by the input signal. Therefore the output current for the bipolar operation I_o' is

$$I_o' = I_o - (V_R/R_B) = (V_R/R_{14}) \left(\sum_{i=1}^{8} d_i 2^{-i} \right) - (V_R/R_B)$$

For binary input word = 00000000, i.e. zero input, the output becomes,

$$V_o = I_o' R_f = (I_o - V_R/R_B) R_f = (0 - 5\ V/5\ k\Omega) \times 5\ k\Omega = -5\,V$$

For binary input word = 10000000 output V_o becomes

$$\begin{aligned} V_o &= (I_o - V_R/R_B) R_f = [V_R/R_{14})\ (d_1/2) - (V_R/R_B)] R_f \\ &= [(5\ V/2.5\ k\Omega)\ (1/2) - (5\ V/5\ k\Omega)]\ 5\ k\Omega \\ &= (1\ mA - 1\ mA) \times 5\ k\Omega = 0V \end{aligned}$$

For binary input word = 11111111 output V_o becomes

$$\begin{aligned} V_o &= [(V_R/R_{14})\ (255/256) - (V_R/R_B)] R_f = (1.992\ mA - 1\ mA) \times 5\ k\Omega \\ &= 0.992\ mA \times 5\ k\Omega = +4.960\ V \end{aligned}$$

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Example 10.2

Calculate the values of the LSB, MSB and full scale output for an 8-bit DAC for the 0 to 10 V range.

Solution

$$\text{LSB} = \frac{1}{2^8} = \frac{1}{256}$$

For 10 V range, $\quad \text{LSB} = \dfrac{10\text{ V}}{256} = 39\text{ mV}$

and $\quad \text{MSB} = \left(\dfrac{1}{2}\right)\text{ full scale} = 5\text{ V}$

Full scale output = (Full scale voltage – 1 LSB)

= 10 V – 0.039 V = 9.961 V

Example 10.3

What output voltage would be produced by a D/A converter whose output range is 0 to 10 V and whose input binary number is

(i) 10 (for a 2-bit D/A converter)
(ii) 0110 (for a 4-bit DAC)
(iii) 10111100 (for a 8-bit DAC)

Solution

(i) $V_0 = 10\text{ V}\left(1 \times \dfrac{1}{2} + 0 \times \dfrac{1}{4}\right) = 5\text{ V}$

(ii) $V_0 = 10\text{ V}\left(0 \times \dfrac{1}{2} + 1 \times \dfrac{1}{2^2} + 1 \times \dfrac{1}{2^3} + 0 \times \dfrac{1}{2^4}\right)$

$= 10\left(\dfrac{1}{4} + \dfrac{1}{8}\right) = 3.75\text{ V}$

(iii) $V_0 = 10\text{ V}\,(1 \times 1/2 + 0 \times 1/2^2 + 1 \times 1/2^3 + 1 \times 1/2^4 + 1 \times 1/2^5 + 1 \times 1/2^6 + 0 \times 1/2^7 + 0 \times 1/2^8)$

$= 10\text{ V}\,(1/2 + 1/8 + 1/16 + 1/32 + 1/64) = 7.34\text{ V}$

10.3 A-D CONVERTERS

The block schematic of ADC shown in Fig. 10.9 provides the function just opposite to that of a DAC. It accepts an analog input voltage V_a and produces an output binary word $d_1 d_2 \ldots d_n$ of functional value D, so that

$$D = d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n} \qquad (10.3)$$

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DIRECT TYPE ADCs

10.3.1 The Parallel Comparator (Flash) A/D converter

This is the simplest possible A/D converter. It is at the same time, the fastest and most expensive technique. Figure, 10.10 (a) shows a 3-bit A/D converter. The circuit consists of a resistive divider network, 8 op-amp comparators and a 8-line to 3-line encoder (3-bit priority encoder). The comparator and its truth table is shown in Fig. 10.10 (b). A small amount of hysteresis is built into the comparator to resolve

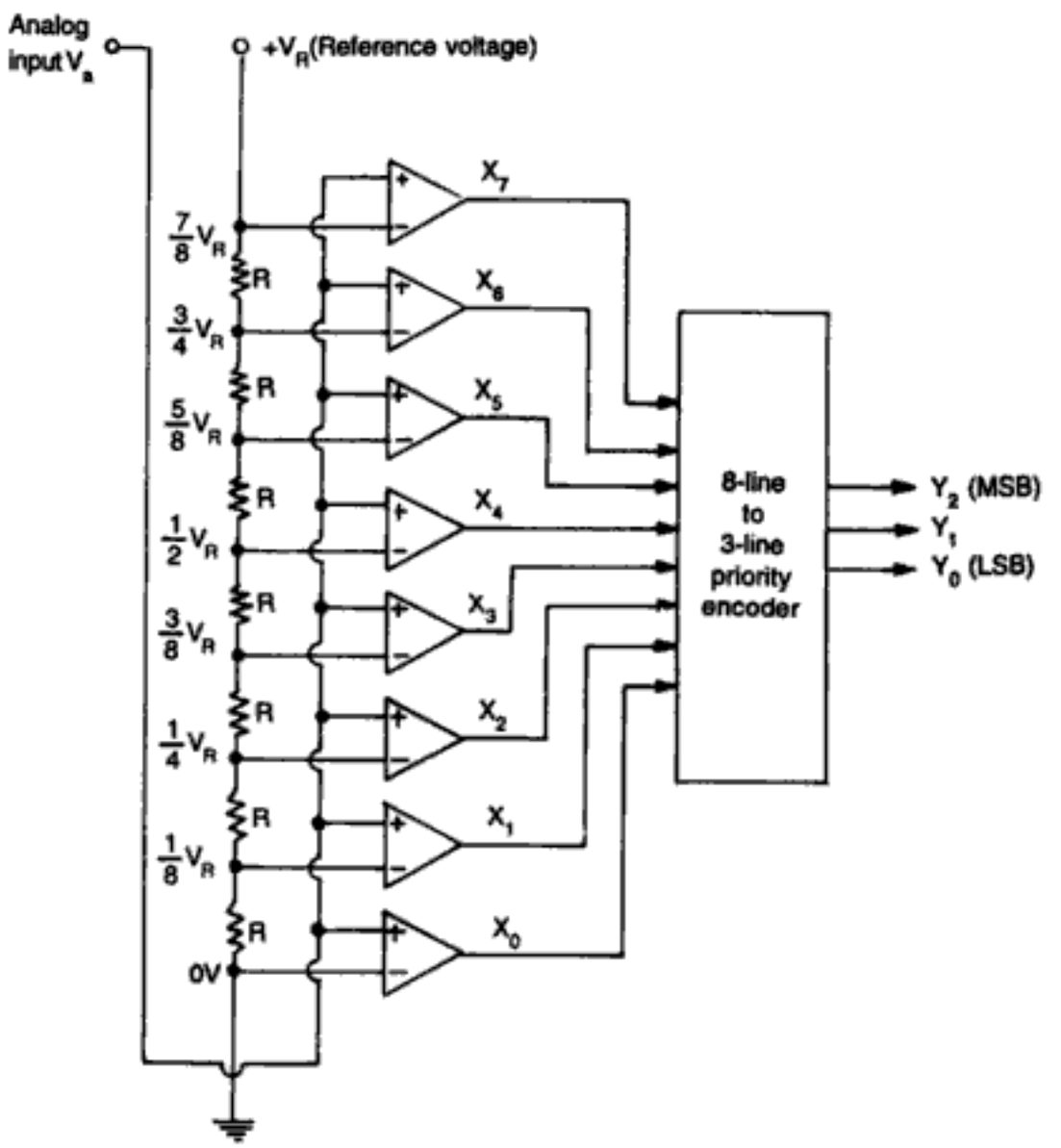

Fig. 10.10 (a) Basic circuit of a flash type A/D converter

any problems that might occur if both inputs were of equal voltage as shown in the truth table. Coming back to Fig. 10.10 (a), at each node of the resistive divider, a comparison voltage is available. Since all the resistors are of equal value, the voltage levels available at the nodes are equally divided between the reference voltage V_R and the ground. The purpose of the circuit is to compare the analog input voltage V_a

with each of the node voltages. The truth table for the flash type AD converter is shown in Fig. 10.10 (c). The circuit has the advantage of high speed as the conversion take place simultaneously rather than sequentially. Typical conversion time is 100 ns or less. Conversion time is limited only by the speed of the comparator and of the priority encoder. By using an Advanced Micro Devices AMD 686A comparator and a T1147 priority encoder, conversion delays of the order of 20 ns can be obtained.

Voltage input	Logic output X
$V_a > V_d$	$X = 1$
$V_a < V_d$	$X = 0$
$V_a = V_d$	Previous value

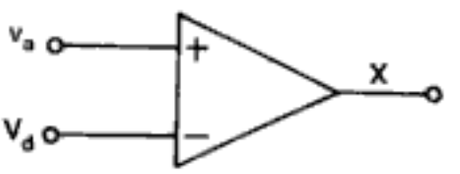

Fig. 10.10 (b) Comparator and its truth table

Input voltage V_a	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
0 to $V_R/8$	0	0	0	0	0	0	0	1	0	0	0
$V_R/8$ to $V_R/4$	0	0	0	0	0	0	1	1	0	0	1
$V_R/4$ to 3 $V_R/8$	0	0	0	0	0	1	1	1	0	1	0
3 $V_R/8$ to $V_R/2$	0	0	0	0	1	1	1	1	0	1	1
$V_R/2$ to 5 $V_R/8$	0	0	0	1	1	1	1	1	1	0	0
5 $V_R/8$ to 3 $V_R/4$	0	0	1	1	1	1	1	1	1	0	1
3 $V_R/4$ to 7 $V_R/8$	0	1	1	1	1	1	1	1	1	1	0
7 $V_R/8$ to V_R	1	1	1	1	1	1	1	1	1	1	1

Fig. 10.10 (c) Truth table for a flash type A/D converter

This type of ADC has the disadvantage that the number of comparators required almost doubles for each added bit. A 2-bit ADC requires 3 comparators, 3-bit ADC needs 7, whereas 4-bit requires 15 comparators. In general, the number of comparators required are $2^n - 1$ where n is the desired number of bits. Hence the number of comparators approximately doubles for each added bit. Also the larger the value of n, the more complex is the priority encoder.

10.3.2 The Counter Type A/D Converter

The D to A converter can easily be turned around to provide the inverse function A to D conversion. The principle is to adjust the DAC's input code until the DAC's output comes within ± (1/2) LSB to the analog input V_a which is to be converted to binary digital form. Thus in addition to the DAC, we need suitable logic circuitry to perform the code search and a comparator of adequate quality to announce when the DAC output has come within ± (1/2) LSB to V_a.

A 3-bit counting ADC based upon the above principle is shown in Fig. 10.11 (a). The counter is reset to zero count by the reset pulse. Upon the release of RESET, the clock pulses are counted by the binary

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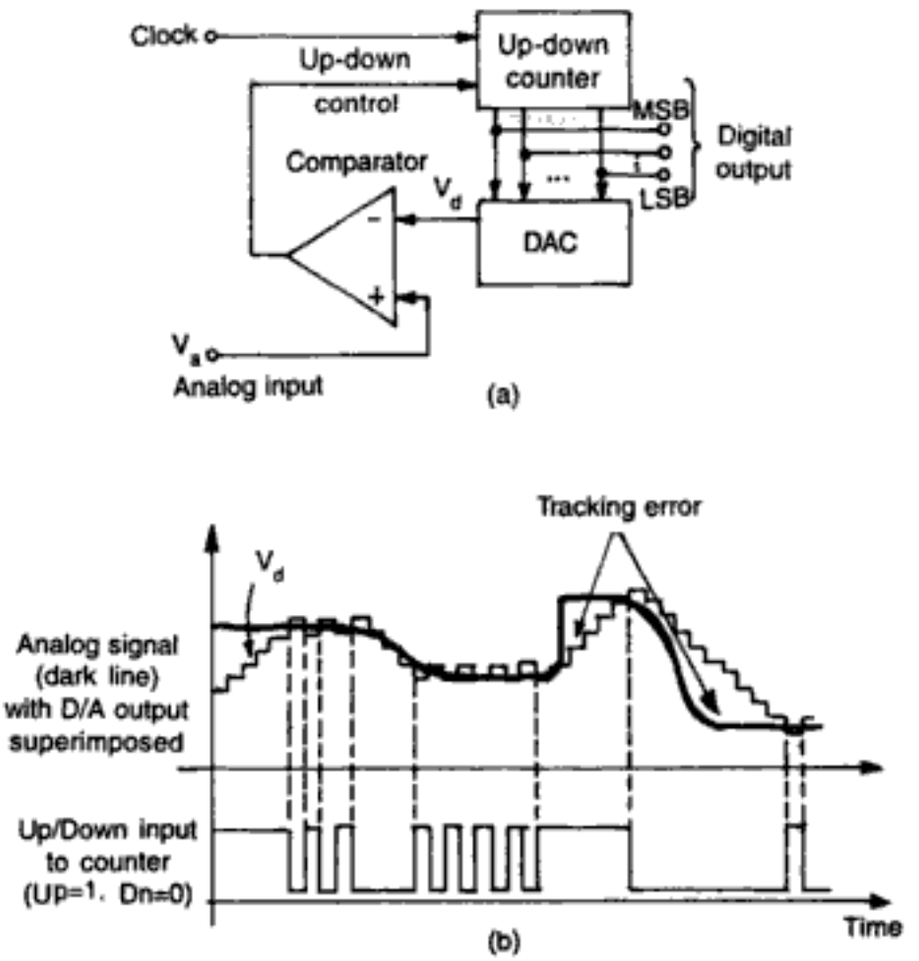

Fig. 10.12(a) A tracking A/D converter (b) Waveforms associated with a tracking A/D converter

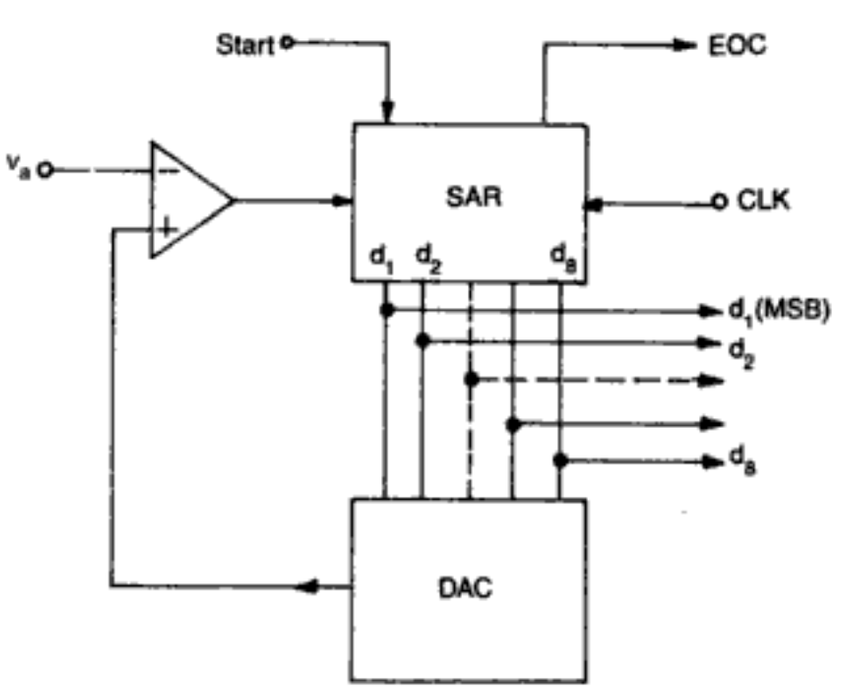

Fig. 10.13 Functional diagram of the successive approximation ADC

state and this can be taken as the end of conversion (EOC) command. Figure 10.14 (a) shows a typical conversion sequence and Fig. 10.14 (b) shows the associated wave forms. It can be seen that the D/A output voltage becomes successively closer to the actual analog input voltage. It requires eight pulses to establish the accurate output regardless of the value of the analog input. However, one additional clock pulse is used to load the output register and reinitialize the circuit.

Correct digital representation	*Successive approximation register output V_d at different stages in the conversion*	*Comparator output*
11010100	10000000	1 (initial output)
	11000000	1
	11100000	0
	11010000	1
	11011000	0
	11010100	1
	11010110	0
	11010101	0
	11010100	

Fig. 10.14 (a) Successive approximation conversion sequence for a typical analog input

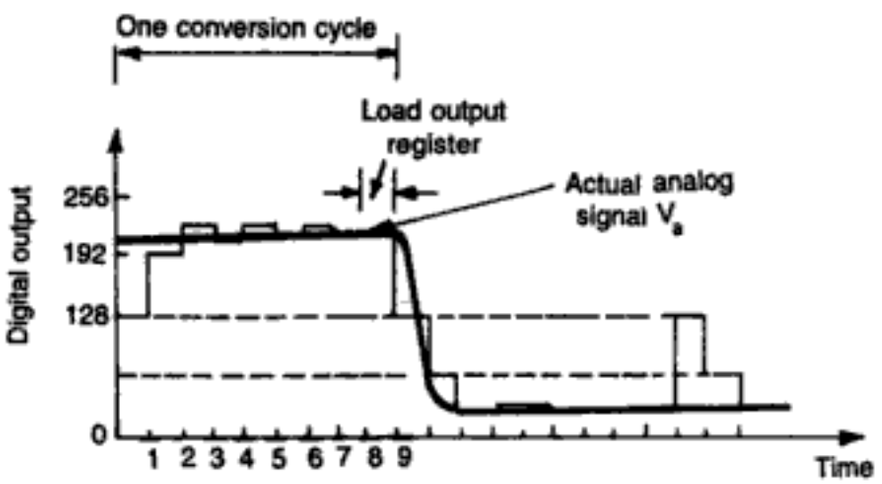

Fig. 10.14 (b) The D/A output voltage is seen to become successively closer to the actual analog input voltage

A comparison of the speed of an eight bit tracking ADC and an eight bit successive approximation ADC is made in Fig. 10.15. Given the same clock frequency, we see that the tracking circuit is faster only for small changes in the input. In general, the successive approximation technique is more versatile and superior to all other circuits discussed so far.

Successive approximation ADCs are available as self contained ICs. The AD7592 (Analog Devices Co.) a 28-pin dual-in-line CMOS package is a 12-bit A/D converter using successive approximation technique.

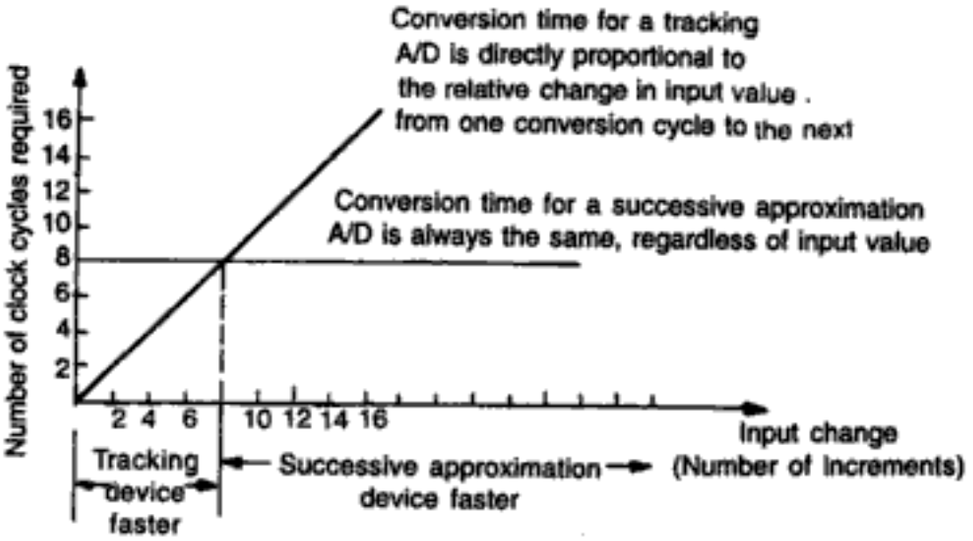

Fig. 10.15 Comparison of conversion times for tracking and successive approximation A/D devices

Integrating Type of ADCs

The integrating type of ADCs do not require a S/H circuit at the input. If the input changes during conversion, the ADC output code will be proportional to the value of the input averaged over the integration period.

10.3.5 Charge Balancing ADC

The principle of charge balancing ADC is to first convert the input signal to a frequency using a voltage to frequency (V/F) converter. This frequency is then measured by a counter and converted to an output code proportional to the analog input. The main advantage of these converters is that it is possible to transmit frequency even in noisy environment or in isolated form. However, the limitation of the circuit is that the output of V/F converter depends upon an *RC* product whose value cannot be easily maintained with temperature and time. The drawback of the charge balancing ADC is eliminated by the dual slope conversion.

10.3.6 Dual-Slope ADC

Figure 10.16 (a) shows the functional diagram of the dual-slope or dual-ramp converter. The analog part of the circuit consists of a high input impedance buffer A_1, precision integrator A_2 and a voltage comparator. The converter first integrates the analog input signal V_a for a fixed duration of 2^n clock periods as shown in Fig. 10.16 (b). Then it integrates an internal reference voltage V_R of opposite polarity until the integrator output is zero. The number N of clock cycles required to return the integrator to zero is proportional to the value of V_a averaged over the integration period. Hence N represents the desired output code. The circuit operates as follows:

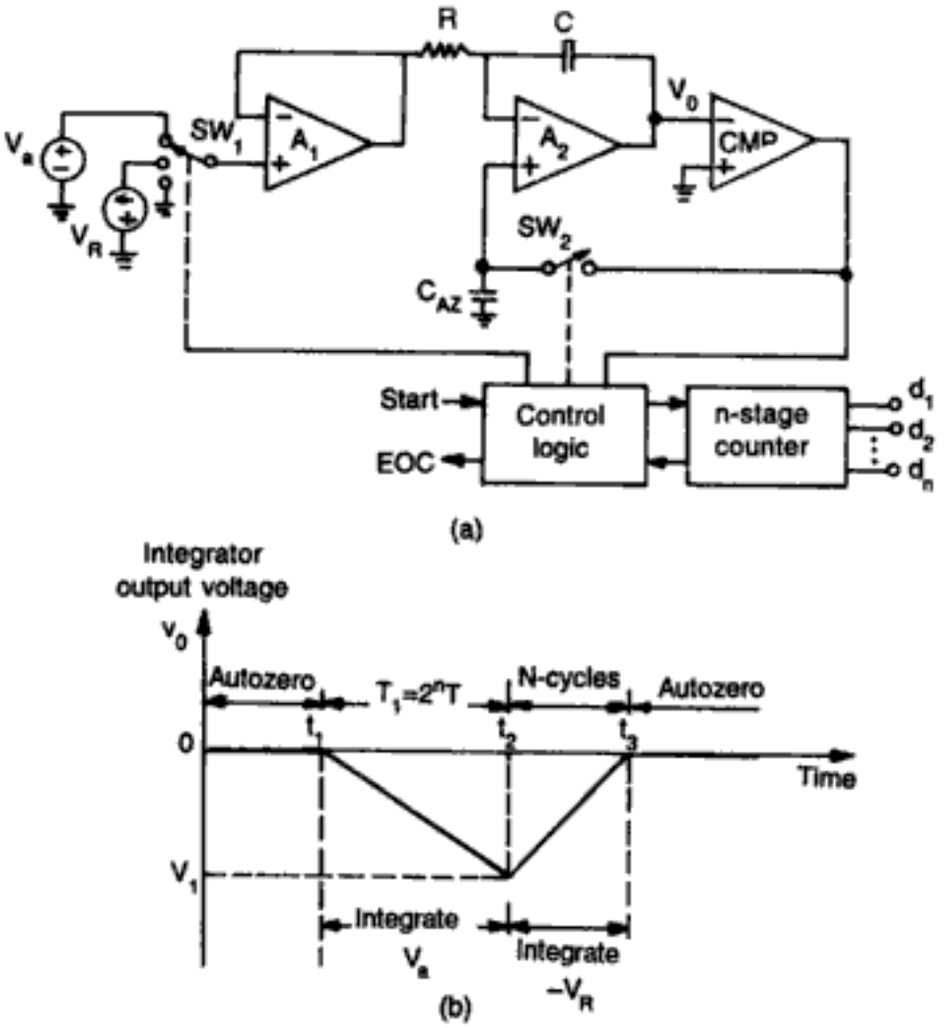

Fig. 10.16 (a) Functional diagram of the dual slope ADC (b) Integrated output waveform for the dual slop ADC

Before the START command arrives, the switch SW_1 is connected to ground and SW_2 is closed. Any offset voltage present in the A_1, A_2, comparator loop after integration, appears across the capacitor C_{AZ} till the threshold of the comparator is achieved. The capacitor C_{AZ} thus provides automatic compensation for the input-offset voltages of all the three amplifiers. Later, when SW_2 opens, C_{AZ} acts as a memory to hold the voltage required to keep the offset nulled. At the arrival of the START command at $t = t_1$, the control logic opens SW_2 and connects SW_1 to V_a and enables the counter starting from zero. The circuit uses an n-stage ripple counter and therefore the counter resets to zero after counting 2^n pulses. The analog voltage V_a is integrated for a fixed number 2^n counts of clock pulses after which the counter resets to zero. If the clock period is T, the integration takes place for a time $T_1 = 2^n \times T$ and the output is a ramp going downwards as shown in Fig. 10.16 (b).

The counter resets itself to zero at the end of the interval T_1 and the switch SW_1 is connected to the reference voltage ($-V_R$). The output voltage v_0 will now have a positive slope. As long as v_0 is negative, the output of the comparator is positive and the control logic allows the

clock pulse to be counted. However, when v_0 becomes just zero at time $t = t_3$, the control logic issues an end of conversion (EOC) command and no further clock pulses enter the counter. It can be shown that the reading of the counter at t_3 is proportional to the analog input voltage V_a.

In Fig. 10.16(b)

$$T_1 = t_2 - t_1 = \frac{2^n \text{ counts}}{\text{clock rate}} \tag{10.4}$$

and

$$t_3 - t_2 = \frac{\text{digital count } N}{\text{clock rate}} \tag{10.5}$$

For an integrator,

$$\Delta v_0 = (-1/RC)\ V(\Delta t) \tag{10.6}$$

The voltage v_0 will be equal to v_1 at the instant t_2 and can be written as

$$v_1 = (-1/RC)\ V_a(t_2 - t_1)$$

The voltage v_1 is also given by

$$v_1 = (-1/RC)\ (-V_R)\ (t_2 - t_3)$$

So,

$$V_a(t_2 - t_1) = V_R(t_3 - t_2)$$

Putting the values of $(t_2 - t_1) = 2^n$ and $(t_3 - t_2) = N$, we get

$$V_a(2^n) = (V_R)N$$

or,

$$V_a = (V_R)\ (N/2^n) \tag{10.7}$$

The following important observations can be made:

1. Since V_R and n are constant, the analog voltage V_a is proportional to the count reading N and is independent of R, C and T.
2. The dual-slope ADC integrates the input signal for a fixed time, hence it provides excellent noise rejection of ac signals whose periods are integral multiples of the integration time T_1. Thus ac noise superimposed on the input signal such as 50 Hz power line pick-up will be averaged during the input integration time. So choose clock period T, so that 2^nT is an exact integral multiple of the line period (1/50) second = 20 ms.
3. The main disadvantage of the dual-slope ADC is the long conversion time. For instance, if $2^n - T = 1/50$ is used to reject line pick-up, the conversion time will be 20 ms.

Dual-slope converters are particularly suitable for accurate measurement of slowly varying signals, such as thermocouples and weighing scales. Dual-slope ADCs also form the basis of digital panel meters and multimeters.

Dual-slope converters are available in monolithic form and are available both in microprocessor compatible and in display oriented versions. The former provide the digital code in binary form whereas

the display oriented versions present the output code in a format suitable for the direct drive of LED displays. The Datel Intersil ICL7109 is a monolithic 12-bit dual-slope ADC with microprocessor compatibility.

Example 10.4

A dual slope ADC uses a 16-bit counter and a 4 MHz clock rate. The maximum input voltage is + 10 V. The maximum integrator output voltage should be – 8 V when the counter has cycled through 2^n counts. The capacitor used in the integrator is 0.1 μF. Find the value of the resistor R of the integrator.

Solution

Time period $(t_2 - t_1)$ in Fig. 10.16 (b) $= \dfrac{2^{16}}{4\text{ MHz}} = \dfrac{65536}{4\text{ MHz}} = 16.38$ ms

For the integrator

$$\Delta v_o = (-1/RC)\ V_a (t_2 - t_1)$$

So, $RC = -(10\text{ V}/-8\text{ V})\ 16.3\text{ ms} = 20.47\text{ ms}$

$$R = \frac{20.47\text{ ms}}{0.1\,\mu\text{F}} = 204.7\,\text{k}\Omega = 205\,\text{k}\Omega$$

Example 10.5

If the analog signl V_a is + 4.129 V in the example 10.4, find the equivalent digital number.

Solution

Since, $V_a = V_R(N/2^n)$

So the digital count $N = 2^n\ (V_a/V_R) = 65536\ (4.129\ V/8\text{ V}) = 33825$ for which the binary equivalent is 1000010000100001.

10.4 DAC/ADC SPECIFICATIONS

Both D/A and A/D converters are available with wide range of specifications. The various important specifications of converters generally specified by the manufacturers are analyzed.

Resolution: The resolution of a converter is the smallest change in voltage which may be produced at the output (or input) of the converter. For example, an 8-bit D/A converter has $2^8 - 1 = 255$ equal intervals. Hence the smallest change in output voltage is (1/255) of the full scale output range. In short, the resolution is the value of the LSB.

$$\text{Resolution (in volts)} = \frac{V_{FS}}{2^n - 1} = 1\text{ LSB increment} \qquad (10.8)$$

However, resolution is stated in a number of different ways. An 8-bit DAC is said to have : 8 bit resolution
: a resolution of 0.392 of full-scale
: a resolution of 1 part in 255

Similarly, the resolution of an A/D converter is defined as the smallest change in analog input for a one bit change at the output. As an example, the input range of an 8-bit A/D converter is divided into 255 intervals. So the resolution for a 10 V input range is 39.22 mV (= 10 V/255). Table 10.1 gives the resolution for 6-16 bit DACs.

Table 10.1 Resolution for 6–16 bit DACs

Bits	*Intervals*	*LSB size (% of Full Scale)*	*LSB size (10 V Full Scale)*
6	63	1.588%	158.8 mV
8	256	0.392%	39.2 mV
10	1023	0.0978%	9.78 mV
12	4095	0.0244%	2.44 mV
14	16383	0.0061%	0.61 mV
16	65535	0.0015%	0.15 mV

Linearity: The linearity of an A/D or D/A converter is an important measure of its accuracy and tells us how close the converter output is to its ideal transfer characteristics. In an ideal DAC, equal increment in the digital input should produce equal increment in the analog output and the transfer curve should be linear. However, in an actual DAC, output voltages do not fall on a straight line because of gain and offset errors as shown by the solid line curve in Fig. 10.17. The static performance of a DAC is determined by fitting a straight line through the measured output points. The linearity error measures the deviation of the actual output from the fitted line and is given by ε/Δ as shown in Fig. 10.17. The error is usually expressed as a fraction of LSB increment or percentage of full-scale voltage. A good converter exhibits a linearity error of less than ± (1/2) LSB.

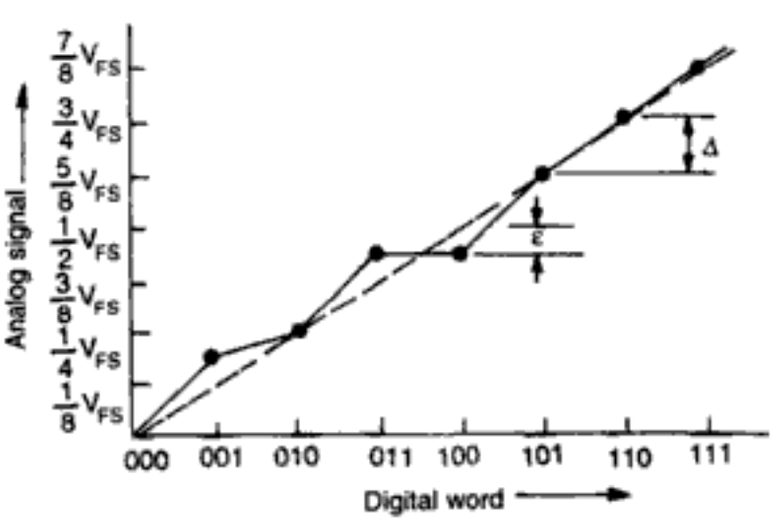

Fig. 10.17 Linearity error for 3-bit DAC

Accuracy: Absolute accuracy is the maximum deviation between the actual converter output and the ideal converter output. Relative accuracy is the maximum deviation after gain and offset errors have

been removed. Data sheets normally specify relative accuracy rather than absolute accuracy. The accuracy of a converter is also specified in terms of LSB increments or percentage of full scale voltage.

Monotonicity: A monotonic DAC is the one whose analog output increases for an increase in digital input. Figure 10.18 represents the transfer curve for a non-monotonic DAC, since the output decreases when input code changes from 001 to 010. A monotonic characteristic is essential in control applications, otherwise oscillations can result. In successive approximation ADCs, a non-monotonic characteristic may lead to missing codes.

If a DAC has to be monotonic, the error should be less than ± (1/2) LSB at each output level. All the commercially available DACs are monotonic because the linearity error never exceeds ± (1/2) LSB at each output level.

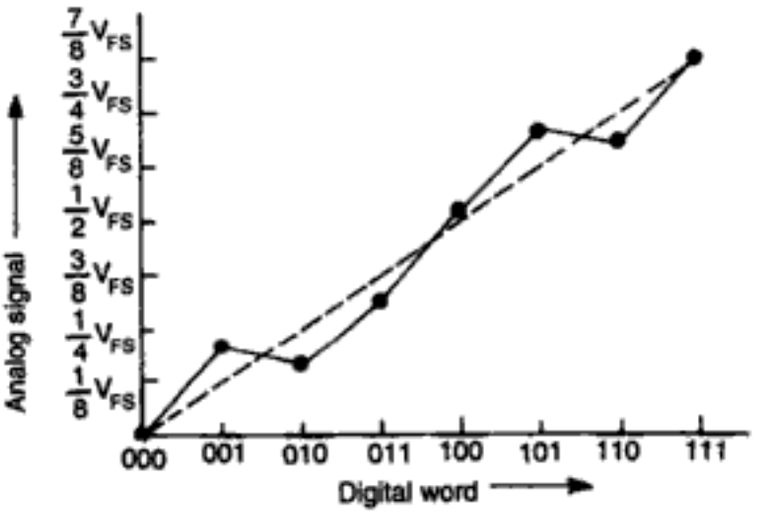

Fig. 10.18 A non-monotonic 3-bit DAC

Settling time: The most important dynamic parameter is the settling time. It represents the time it takes for the output to settle within a specified band ± (1/2) LSB of its final value following a code change at the input (usually a full scale change). It depends upon the switching time of the logic circuitry due to internal parasitic capacitances and inductances. Settling time ranges from 100 ns to 10 μs depending on word length and type of circuit used.

Stability: The performance of converter changes with temperature, age and power supply variations. So all the relevant parameters such as offset, gain, linearity error and monotonicity must be specified over the full temperature and power supply ranges.

A brief overview of ADC and DAC selection guide is given below:

A/D converters:

AD 7520/AD 7530	10-bit binary multiplying type
AD 7521/AD 7531	12-bit binary multiplying type
ADC 0800/0801/0802	8-bit ADC

D/A converters:	
DAC 0800/0801/0802	8-bit DAC
DAC 0830/0831/0832	microprocessor compatible 8-bit DAC
DAC 1200/1201	12-bit DAC
DAC 1208/1209/1210	12-bit microprocessor compatible DAC

Example 10.6

We are familiar with 3½ digit digital voltmeter (DVM) and 4½ digit DVM which are being used regularly in the laboratory. Obviously 3½ digit DVM is less costly as its resolution is poor compared to 4½ digit DVM which is relatively costlier and have better resolution. Let us calculate the resolution of these DVMs.

Solution

In 3½ digit DVM, the MSB can be either 0 or 1 whereas the 3 digit LSBs can be 000 to 999. Hence in 3½ digit DVM, the reading variation can be from 0000 to 1999, that is 2000. The reference voltage is 2V. Hence the resolution is (2/2000) V = 1 mV; that is voltage variation below 1 mV is not detectable. Similarly, in 4½ digit DVM the total variation is from 0 0000 to 1 9999 and reference voltage is 2V. Hence the resolution is (2/20000) V = 0.1 mV. Thus, the resolution of a 4½ digit DVM is ten times better than that of 3½ digit DVM.

Summary

1. The output of a DAC can be either a voltage or current.
2. A multiplying DAC is the one in which the analog signal is allowed to vary.
3. Three resistive techniques for D/A conversion are: weighted resistor DAC, R-2R ladder and inverter R-2R ladder.
4. DAC essentially requires: resistors, electronics switches and an op-amp.
5. Two types of digitally controlled SPDT electronic switches are in use: a totem-pole MOSFET driver, a CMOS inverter.
6. A weighted resistor DAC requires a wide range of resistor values for better resolution whereas a R-2R ladder type DAC requires only two values of resistors.
7. In an inverted R-2R ladder, the current through the resistors remains constant, irrespective of the input data. The constant node voltages therefore eliminate stray capacitance effect and improve circuit performance.
8. Monolithic DACs for 8, 10, 12, 14 and 16 bit resolution are available.
9. A/D converters are either direct type or indirect type. Most direct type ADCs require a D/A converter.
10. The important direct ADC techniques are: Parallel comparator (Flash), Counting type, Tracking type and Successive approximation technique.

11. Integrating type ADCs perform conversion in an indirect manner. The two important converters are: Charge balancing ADC, Dual slope ADC.
12. The parallel comparator ADC is the fastest technique. But it has the disadvantage of using maximum hardware. A counting type A/D converter has low speed with conversion time as long as (2^n-1) clock periods for n-bit ADC. A tracking ADC is simple but gives error when analog signal changes rapidly.
13. Successive approximation type ADC is the most versatile. It completes n-bit conversion in just n-clock periods. Most monolithic ADCs are successive approximation type.
14. Dual slope converters are suitable for precise measurement of slowly varying signals. All digital voltmeters use dual-slope ADC. The disadvantage is of long conversion time.
15. Monolithic dual slope ADCs are available in microprocessor compatible and display-oriented versions.
16. The important converter characteristics are: Resolution, Linearity, Accuracy, Monotonicity, Settling time, Stability etc.

Review Questions

10.1. Classify DACs on the basis of their output.
10.2. Name the essential parts of a DAC.
10.3. Describe the various types of electronic switches used in D/A converter.
10.4. How many resistors are required in a 12-bit weighted resistor DAC?
10.5. Why is an inverted R-2R ladder network DAC better than R-2R ladder DAC?
10.6. List the various A/D conversion techniques.
10.7. Which is the fastest ADC and why?
10.8. Give the conversion time for (i) counting ADC (ii) successive approximation ADC (iii) dual-slope ADC.
10.9. Explain the operation of Dual-slope ADC.
10.10. Explain how Dual-slope ADC provides noise rejection.
10.11. Explain the important specifications of D/A and A/D converters.

PROBLEMS

10.1. How many levels are possible in a two-bit DAC? What is its resolution if the output range is 0 to 3 V.
10.2. A 5-bit D/A converter is available. Assume that '00000' corresponds to an output of + 10 V and that the D/A converter is connected for – 0.1 V per increment, what output voltage will be produced for '11111'?

10.3. If a 10-bit D/A converter spans a range of 0 to 10 V and is always within 1 mV of its ideal output. What is its linearity as a percent of full-scale range?

10.4. Find the voltage at all nodes 0, 1, 2, ... and at the output of a 5-bit R-2R ladder DAC. The least significant bit is 1 and all other bits are equal to 0. Assume $V_R = -10$ V and $R = 10$ kΩ.

10.5. The Fig. P. 10.5 shows a binary weighted resistor D/A converter.

(i) Show that the output resistance is independent of the digital word and that

$$R_0 = \frac{2^{N-1}}{2^N - 1} R$$

(ii) Show that the analog output voltage for the MSB is

$$V_0 = \frac{2^{N-1}}{2^N - 1} V_R$$

(iii) Show that the analog output voltage for the LSB is

$$V_0 = \frac{1}{2^N - 1} V_R$$

10.6. (a) Draw the circuit diagram of a 6-bit inverted R-2R ladder DAC.

(b) For $V(1) = 5$ V, what is the maximum output voltage?

(c) What is the minimum voltage that can be resolved?

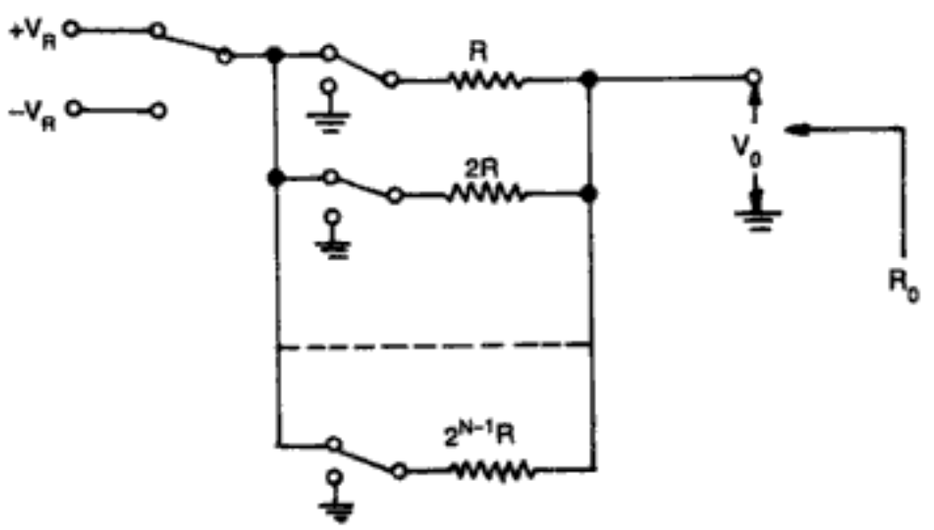

Fig. P. 10.5

10.7. The analog input signal ranges for -5 to $+8$ V in a nine bit A/D converter.

(i) How many quantization levels are available with this A/D converter?

(ii) What is the resolution in volt per increment?

(iii) What binary number will be produced when the analog input is zero volt?

10.8. A counting A/D converter uses a 7-bit DAC. The MSB of DAC output voltage is + 5V.
   (i) If the analog input voltage is + 6.85 V, what will be the R-2R ladder output voltage when the clock stops?
   (ii) What is the number of clock pulses that occur between the release of reset and stopping of the clock?

10.9. The ADC in problem 10.8 uses a 100 kHz clock. How long did it take to digitize 6.85V?

10.10. What is the conversion time of a 10-bit successive approximation A/D converter if its input clock is 5 MHz.

10.11. A dual slope ADC uses a 18-bit counter with a 5 MHz clock. The maximum input voltage is +12 V and the maximum integrator output voltage at 2^N count is – 10 V. If R = 100 kΩ, find the size of the capacitor to be used for integrator.

10.12. The dual slope ADC of problem 10.11 has an input voltage of + 5.237V. Determine the digital number in binary which represents the count in the register.

Experiment 10.1

To construct a 4-bit R-2R ladder type D/A converter. Plot the transfer characteristics, that is, binary input vs output voltage. Calculate the resolution and linearity of the converter from the graph.

(i) Choose R = 10 kΩ, 2R = 20 kΩ of tolerance ± 1% or less.
(ii) For logic '0' short to ground and logic '1' connect to a + 5V supply.

Procedure

1. Set up the circuit shown in Fig. E. 10.1.
2. With all inputs (d_0 to d_3) shorted to ground, adjust the 20 kΩ-pot until the output is 0V. This will nullify any offset voltage at the input of the op-amp.

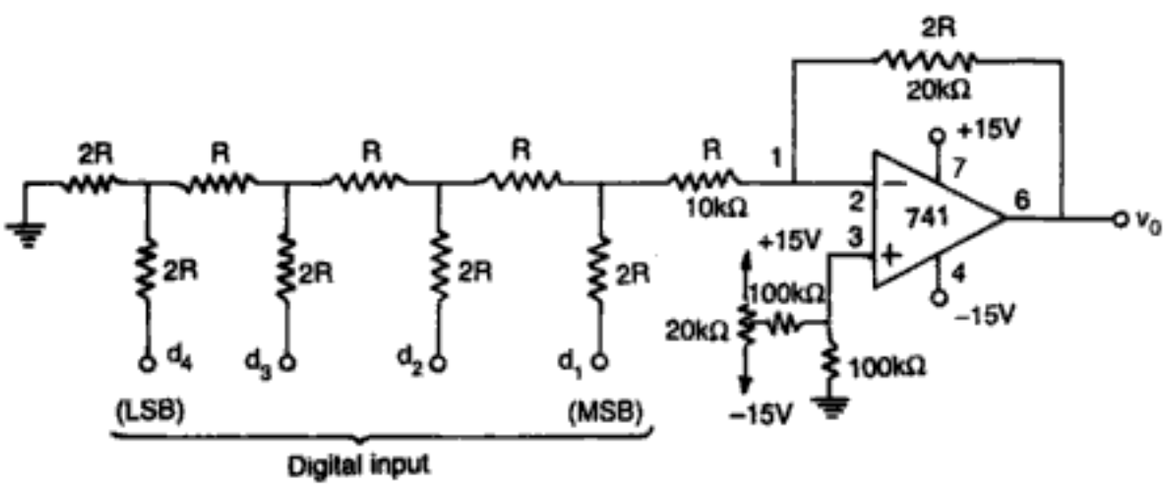

Fig. E. 10.1 A 4-bit R-2R ladder D/A converter

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3. Measure the output voltage for all binary inputs (0000 to 1111) states and plot a graph of binary inputs vs output voltage.
4. Measure the size of each step and hence calculate resolution.
5. Calculate linearity using the definition given in Sec. 10.4.

Experiment 10.2

To set up a 4-bit successive approximation type A/D converter and study its performance.

Procedure

(i) Set up the circuit as shown in Fig. E. 10.2(a). Use the circuit of Fig. E. 10.2(b) for 4-bit weighted resistor D/A converter.
(ii) Connect the Cr terminal to ground momentarily to clear all the flip-flops and the shift resistor IC 7496.
(iii) Connect the Pr terminal momentarily to logic '1' to set the shift register (being used as ring counter) output as $Q_E = 1$, $Q_A = Q_B = Q_C = Q_D = 0$, this will also enable the AND gate for the clock to be transmitted.
(iv) Apply an analog voltage of – 10V. Apply clock pulses, and observe the stable digital output available at the outputs Q_D, Q_C, Q_B, Q_A of the J-K flip-flops.
(v) Vary the input voltage for 0 to –10V and repeat steps (ii), (iii) and (iv).

Appendix-I

PSPICE TUTORIAL

SPICE is a general-purpose circuit program that simulates electronic circuits. SPICE contains models for various circuit elements, active as well as passive and is capable of simulating most of the electronic circuits. SPICE is acronym for *Simulation Program with Integrated Circuit Emphasis* and is used as a popular electrical circuit analysis program. SPICE was originally developed at the University of California, Berkley in the mid-1970s. SPICE has undergone a number of modifications over the years. PSPICE is a very popular version developed by MicroSim Corporation to run on DOS and MacIntosh personal computers.

This appendix includes a summary of the most common default representations for PSPICE circuit models.

PSPICE can be used to simulate and analyze circuits containing resistors, capacitors, inductors, independent and dependent voltage and current sources, and basic semiconductor devices. Separate SPICE models are used for diodes, BJT, JFET, MOSFET, MESFET and Op-Amps.

As a first step, the user must identify each node in the circuit. The location of an element in the circuit is specified by listing the two nodes to which it is connected. Each node is identified by an integer, however, the 0 is reserved for the ground or reference node. The orders in which the two nodes at the terminals of an element are listed are important. The first node is that one at which the +reference for the voltage across the circuit element is located. Thus an element connected between nodes 1 (first named) and 2 (last named) has the voltage V_{12} with the +reference at node 1. The element current I_{12} flows from node 1 (first named) through the element to node 2 (last named).

A resistor is identified by a capital letter R followed by no more than seven additional letters or integers such as RI, ROUTPUT, RINPUT are okay but R1-2, R1/0 are not okay. The value of the resistor can be given in ohms or by use of scale factors as given in Table A-1.

Abbreviation	*Meaning*	*Multiplier*
P	pico	10^{-12}
N	nano	10^{-9}
U	micro	10^{-6}
M	milli	10^{-3}
K	kilo	10^{3}
MEG	mega	10^{6}
G	giga	10^{9}
T	tera	10^{12}

A statement given by

R1 1 2 10K

states that a resistance R1 is connected between nodes 1 and 2 with a value of 10 kΩ.

The independent voltage source is identified by a name beginning with *V* and followed by any combination of not more than seven additional letters or integers. Independent current sources have names beginning with *I*. Thus all the following statements represent dc voltage sources:

VIN 6 0 DC 1.5 → a voltage source VIN is connected between nodes 6 and ground of dc value 1.5 volt.

V2 1 2 DC 10M → a voltage source V2 is connected between nodes 1 and 2 of dc value 10 millivolt.

VCC 4 3 DC 9 → a voltage source VCC is connected between nodes 4 and 3 of dc value 9 volts.

A general sinusoidal input source shown in Fig. 1 has the syntax:

Sin (offset amp freq. delay)

e.g. V1 1 0 sin(0 1V 5 KHz)

means that a sinusoidal input source, V1 of peak amplitude of 1V and frequency 5 KHz is connected between nodes 1 and 0.

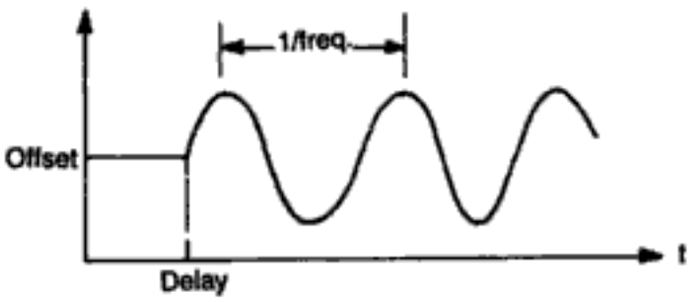

Fig. 1. A general sinusoidal input source

A pulse input source shown in the Fig. 2. has the syntax:

Pulse (V_1 V_2 DELAY T_{RISE} T_{FALL} DUR PERIOD)

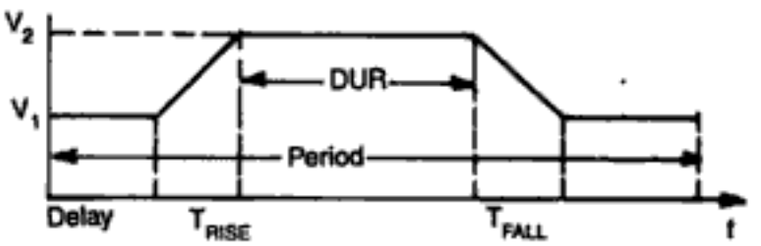

Fig. 2. A pulse input source

If a square wave input has to be applied to the nodes 1 and 0, then the statement will be given as

V1 1 0 pulse(–1V 1V 0MS 0MS 0MS .1MS .2MS)

So the input will be as shown in Fig. 3.

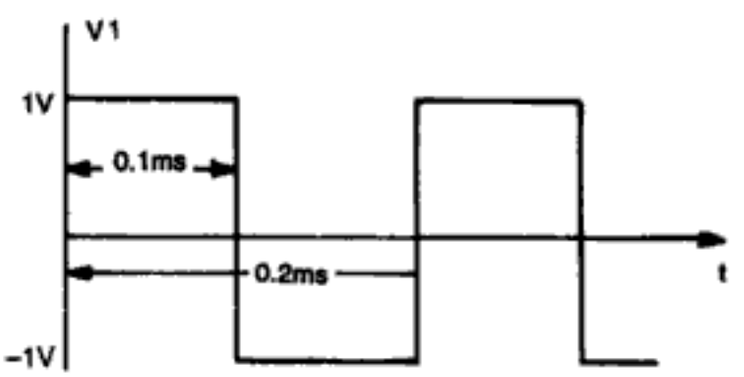

Fig. 3. Square wave input

A step input is given by

V1 1 0 pulse(0V 1V 0MS 0MS 0MS 1MS 1MS)

and is shown in Fig. 4.

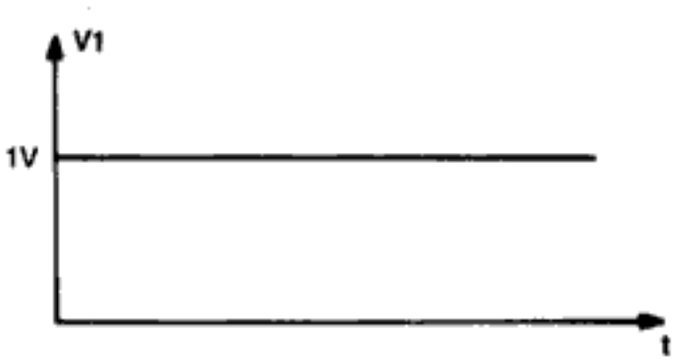

Fig. 4. Step input

Control Commands for Analysis

Note that the SPICE program always interprets the first line of program as **title** of the analysis. Hence always put the title of the circuit for which the analysis is being done. Each program begins with a TITLE statement and ends with an .END statement. For comments, any line beginning with (*) will be printed or displayed but not counted for analysis purpose by the computer.
The control statement

.OP

instructs the computer to calculate the dc voltage between each node and the reference node. The voltages at specific nodes can be obtained from the .PRINT statement. Note that the .PRINT command does not print anything on the paper. The control statement

.PRINT DC V(3) V(1, 3) 1(VX)

instructs the computer to calculate DC value of the node voltage V(3), node-to-node voltage named V (1, 3) between nodes 1 and 3, and the current named I(VX).
Every SPICE program must be ended with the last line as the control statement .END.

Capabilities of PSPICE

Using PSPICE, one can perform the following analysis:

1. DC analysis (large-signal transfer characteristics),
2. AC (small signal) analysis
3. Transient analysis

PSPICE simulation can be performed at different operating temperatures and thermal component noise can also be added. Output can be provided in the tabular form, two dimensional plots, graphs and Bode plots. A special feature of PSPICE is that it includes a graphical output interface called PROBE and a library of devices with pre determined characteristics called parts.

Each analysis is invoked by giving a command statement. The command statements for each of the above analysis are discussed as follows:

DC Analysis

The dc analysis is performed by the statement .DC
The syntax is as follows;

.DC	SOURCE	START	STOP	INCR
.DC	Vin	–5	5	0.1

This means that Vin in the circuit is varied from –5 to +5V in equal steps of 0.1 Volt. All the capacitors in the circuit are treated as open circuit and inductors as short circuit during this analysis.

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Chapter 7

2. 5
3. 1 kHz, 1.74
4. 9
6. 1.6 kΩ, for $R_f = R_i = 10$ kΩ; $C = 0.1$ μF
7. 2050 Hz, 1950 Hz
10. (a) $\frac{1}{RCs+1}$; (b) $\frac{-s}{s^2+2s+1}$

Chapter 8

2. 6.06 kΩ
3. 62.1 μs, 46.92 μs, 9.18 kHz, 43%
4. 0.1 μF, 108.75 kΩ, 72.5 kΩ
5. 0.1 μF, $R_A = R_B = 725\,\Omega$

Chapter 9

1. 653.6 kHz
2. −0.1 V
3. 2.5 V
4. 2500 Hz, ± 812.5 Hz, ± 59.95 Hz
5. ± 275.6 Hz.

Chapter 10

1. 4, 33.33% of full scale
2. 6.9 V
3. 0.102
4. − 3.33 V, − 1.66 V, − 0.82 V, − 0.39 V, − 0.156 V
7. 512, 0.0254 V
10. 2 μs
11. 0.629 μF
12. 1010001000011100001

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Index

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Linear Integrated Circuits

Second Edition

Designed primarily for courses in operational – amplifier and linear integrated circuits for electrical, electronic, instrumentation and computer engineering and applied science students. Includes detailed coverage of fabrication technology of integrated circuits. Basic principle of operational amplifier, internal construction and applications have been discussed. Important linear ICs such as 555 timer, 565 phase-locked loop, linear voltage regulator ICs 78/79 xx and 723 series D-A and A-D converters have been discussed in individual chapters. Each topic is covered in depth. Large number of solved problems, review questions and experiments are given with each chapter for better understanding of text.

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